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ABSTRACT

The large channel length graphene field-effect transistor (GFET) can outperform its competitors due to its larger active area and lower noise. Such long channel length devices have numerous applications, e.g., in photodetectors, biosensors, etc. However, long channel length graphene devices are not common due to their semi-metallic nature. Here, we fabricate large channel length (up to 5.7 mm) GFETs through a simple, cost-effective method that requires thermally evaporated source-drain electrode deposition, which is less cumbersome than the conventional wet-chemistry based photolithography. The semiconducting nature of graphene has been achieved by utilizing the Li^+ ion of the Li_5AlO_4 gate dielectric, which shows current saturation at a low operating voltage (~2 V). The length scaling of these GFETs has been studied with respect to channel length variation within a range from 0.2 mm to 5.7 mm. It is observed that a GFET of 1.65 mm channel length shows optimum device performance with good current saturation. This particular GFET shows a "hole" mobility of 312 $cm^2\ V^{-1}\ s^{-1}$ with an on/off ratio of 3. For comparison, another GFET has been fabricated in the same geometry by using a conventional SiO_2 dielectric that does not show any gate-dependent transport property, which indicates the superior effect of Li^+ of the ionic gate dielectric on current saturation.

I. INTRODUCTION

In the twenty-first century, graphene, a single layer two dimensional (2D) allotrope of carbon atoms, has attracted immense attention in the electronics world due to its unusually high carrier mobility.[1] Along with this, its chemical stability, lightweight, and excellent optoelectronic properties have added more flavor to the exploration of this material in different areas of electronics.[2] However, unlike conventional semiconductors, large-area single-layer graphene (SLG) is semimetal in nature with zero bandgap.[2] The valence and conduction bands of SLG meet to form a cone shape at the K points (named Dirac points) of the Brillouin zone.[3] Because of having zero bandgap, field-effect transistors (FETs) made with a larger channel length cannot be switched off, which makes them unsuitable for logic applications.[2] Large channel length devices can be used in power handling owing to their efficient operation at higher voltages without breaking down the junction and also have low noise, which is very beneficial for analog devices. Long channel length devices are promising in many areas such as for light sensing (photodetector), sensing of bio-analytes (biosensor), etc.[4] Unfortunately, long channel length graphene devices are not common due to their semi-metallic nature, which limits the use of graphene as a semiconductor in FETs, photodetectors, sensors, etc. Hence, the opening of the bandgap in graphene is a crucial step for its realistic application. To date, many efforts have been made to open the bandgap in graphene. Mainly, three types of efforts have

been reported: by confining the electron in quasi one-dimensional graphene nanoribbons,[5] through biasing of bilayer graphene,[6] and by applying strain to graphene through dual-gate biasing.[7] In addition to these three major efforts, ionic or molecular-doping and chemical functionalization have also been reported for opening the bandgap in SLG.[8,9] Particularly, a number of theoretical[10,11] and experimental studies[12,13] suggest that lithium-ion (Li^+) intercalation can open a bandgap of ~0.85 eV in SLG, which is very encouraging for graphene logic circuits in the future. However, the effect of such a kind of Li^+ incorporation on SLG transistors has not been experimentally verified.

Besides the bandgap issue, until now, the fabrication method of graphene field-effect transistors (GFETs) is very expensive and tedious. In most of the earlier reported works on GFETs, different lithography processes had been employed to fabricate the source/drain contact in micrometer or lesser sized channel length (L) FETs, which is a costly and time-consuming process. Cost-effective fabrication like the printing or the physical vapor deposited (PVD) shadow mask process can reach up to several 10 μm channel lengths. However, due to the semimetal nature of graphene, it is practically not possible to fabricate such a large channel length GFET by using these deposition methods.[9] Therefore, despite a large number of reports on GFETs, we hardly found any cost-effective GFET fabrication for large-area applications. Thus, a new technique should be adopted to fabricate devices for 2D systems (e.g., graphene), which is different from the conventional wet-chemistry based photolithography that leads to adverse effects on the novel properties of graphene.

In the present work, we have developed a simple, cost-effective method to fabricate large channel length SLG thin-film transistors that show a good current saturation with low operating voltage. Both the low operation voltage and the current saturation of GFETs have been achieved by utilizing Li^+ of the ion-conducting Li_5AlO_5 gate dielectric. Large area graphene has been grown by the conventional chemical vapor deposition (CVD) method and ion-conducting Li_5AlO_5 by the sol–gel method. A silver electrode (Ag) with a molybdenum oxide (MoO_x) interface has been used as a source and drain electrode, which was deposited by a thermal evaporation process. The distance between the source and the drain was taken as large as in an mm scale that has been varied from 0.2 mm to 5.7 mm. All of these GFETs show typical p-channel transport with the optimum device performance by a GFET of a channel length of 1.65 mm. For comparison, such kinds of mm-scale channel length GFETs have been fabricated using the conventional SiO_2 gate dielectric, and none of them show any significant variation in drain voltage even with a very high variation of gate voltage. This comparison indicates that the mobile Li^+ ion of the Li_5AlO_5 gate dielectric plays a key role in the current saturation of the devices.

II. RESULTS AND DISCUSSION

As mentioned earlier, a single layer of graphene has been was grown on a Cu substrate by the CVD method and has been transferred on the Li_5AlO_5 gate dielectric by the standard graphene transfer method. The details of this deposition and the transfer method of graphene are described in Secs. 1 and 2 of the supplementary material, respectively. The CVD that grew large-area graphene film was characterized by an optical microscope [Fig. S1(a)], scanning electron microscope [SEM, Fig. S1(b)], transmission electron microscope [TEM, Fig. S1(c)], and Raman spectrum [Fig. S1(d)], which are discussed in Sec. 3 of the supplementary material. These studies reveal that this graphene layer is a homogeneous single-layer film with some wrinkles. The precursor solution of Li_5AlO_4 was prepared by the Yoldas process, which is given in Sec. 4 of the supplementary material. Graphene TFTs have been fabricated on a highly doped silicon substrate (p^+-Si) coated with a polycrystalline Li_5AlO_4 dielectric thin film that was deposited on top of this substrate by spin coating and a subsequent annealing process. Source/drain electrodes (Ag/MoO_x) were deposited by a thermal evaporation process with a fixed channel width (W) of 9 mm but with variable channel lengths (L) ranging from 0.2 mm to 5.7 mm. Details of this device fabrication process are given in Sec. 5 of the supplementary material.

All electrical characteristics of GFETs were studied by using a semiconductor parameter analyzer (KEYSIGHT B1500 A, USA) under ambient atmospheric conditions. Electrical contacts of GFETs are made with a manual probe station. As mentioned earlier, single layer GFETs were fabricated with a fixed channel width but with six variable channel lengths, and hence, its W/L ratio varies from 118 to 1.57. During all the electrical characterizations, the drain voltage (V_D) and the gate voltage (V_G) were varied within a range of 2.0 V. Figure S2 of the supplementary material shows the output (drain current vs drain voltage) and transfer characteristics (drain current vs gate voltage) of six GFETs that were fabricated on the p^+-Si/Li_5AlO_4 substrate. These characteristics indicate a p-channel behavior of all individual devices. However, there is a big difference in the device characteristics of different GFETs. Figures S2(a)–S2(f) show the output characteristics (I_D vs V_D) with different channel lengths that point out the gradual improvement in current saturation as the channel length varied from 0.2 mm to 1.65 mm. For this current saturation, the best result was observed for a channel width of 1.65 mm when V_D swept from 0 V to −2.0 V and V_G varied from 0.5 V to −2.0 V [Fig. 1(b)]. However, this current saturation deteriorates as soon as the channel length is increased. During this characterization, the GFET on the p^+-Si/SiO_2 substrate was also tested. However, none of those GFETs show any gate voltage-dependent current; rather, they show a metallic conduction event at very high gate voltage like −40 V (Fig. S3). This observation implies that fabrication of GFETs with such a long channel length is only possible with such a kind of ionic gate dielectric.

Similarly, Figs. S2(g)–S2(l) show the transfer characteristics of the respective GFETs, which show that the on/off ratio and the Dirac point of these devices varied significantly with channel length. Out of these six characteristics, a high on/off ratio of ~3 was observed for the device with a channel length of 1.65 mm [Fig. 1(c)]. In addition to this, the transfer characteristics show that all GFETs have positive Dirac points. This positive shift of the Dirac point originated from the impurity of the graphene film and the dielectric/graphene interface trap state.[14] The least value of the Dirac point is also seen for GFETs with 1.65 mm channel width. Effective carrier mobility (μ) of these GFETs is calculated from the following equation:[15]

$$I_D = \mu \frac{W}{L} C V_{ds} (V_G - V_{th}). \quad (1)$$

Here, I_D, V_G, V_{th} are the drain voltage, gate voltage, and threshold voltage of the GFET, respectively. C is the capacitance per unit

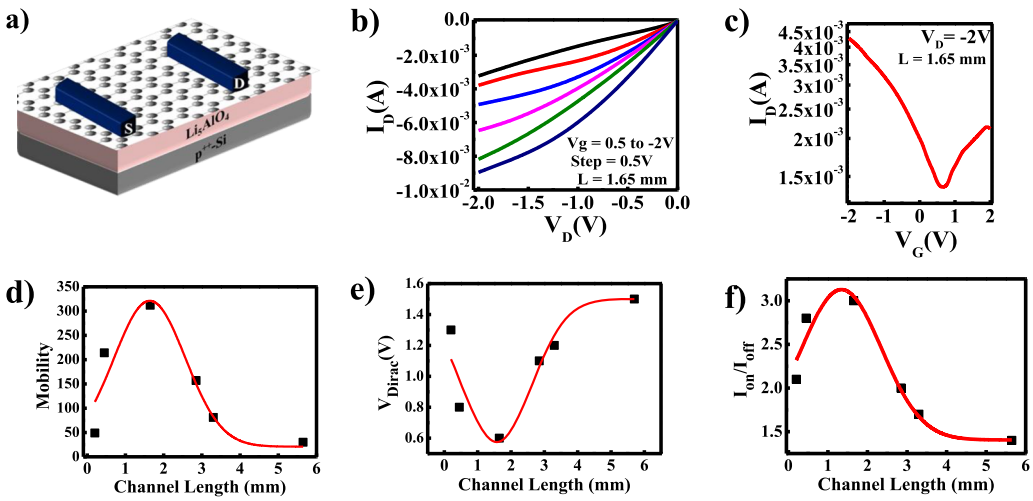

FIG. 1. (a) Schematic illustration of GFETs, (b) output characteristics and (c) transfer characteristics of GFETs with a W/L ratio of ~5.5 (9 mm/1.65 mm), (d) variation in mobility with channel length, (e) variation in a shift in the Dirac point with channel length, and (f) variation in the on/off ratio with channel length.

area of the gate dielectric, and W and L are the channel width and length, respectively. The measured capacitance per unit area of the Li_5AlO_4 dielectric is 350 nF cm^{-2} at 50 Hz frequency (Fig. S4), which is used to calculate charge carrier mobility. The hole mobility for 0.2 mm channel length is 49 cm^2 V^{-1} s^{-1} and increases up to 312 cm^2 V^{-1} s^{-1} for 1.65 mm channel length. However, a further increase in L values decreases the carrier mobility gradually, which reaches 30 cm^2 V^{-1} s^{-1} for 5.7 mm channel length. The variation in the calculated hole mobility with channel length is shown in Fig. 1(d). In addition to mobility, the Dirac point also shifted with the variation in channel length. The variation in the Dirac point and the on/off ratio with channel length are shown in Figs. 1(e) and 1(f), respectively. From this study, it is very clear that the Dirac point gradually decreases when the channel length varies from 0.2 mm to 1.65 mm and then shifts toward a more positive voltage when the channel length varies from 2.85 mm to 5.7 mm.

As mentioned earlier, Li^+ doping is an effective way to open the bandgap of graphene. To check the effect of Li^+ ion on the graphene sheet, we also fabricated the same device with different channel lengths on p-Si^+/SiO_2 substrates, but we did not get any saturation data which is expected because large-area graphene always acts as a semimetal which indicates the conducting nature of graphene (Fig. S3). Therefore, these comparative studies of GFETs on p^+-Si/Li_5AlO_4 and p^+-Si/SiO_2 substrates indicate that the Li^+ of Li_5AlO_4 dielectric plays a key role in the fabrication of larger channel length GFETs. Again, instead of having the ambipolar nature of graphene, the hole likes conduction, i.e., p-GTFT characteristics arise due to oxygen and water adsorption on the graphene surface.[14,16] In these studies, the optimum value of carrier mobility arises due to two combined effects. One of them is the contact resistance of the source and drain electrodes, which decreases with channel length. Therefore, the carrier mobility of GFETs is supposed to increase with channel length. However, increasing the channel length increases the scattering of carriers from ripples, interfaces, and the defect states of graphene. Additionally, the carrier can be trapped in the dielectric/graphene interface. Thus, charge carrier scattering and charge trapping phenomena reduce effective mobility with channel length. Therefore, the combined effects of these two phenomena limit GFETs from reaching their best performance with 1.65 mm channel length.

To realize the opening of the energy bandgap in the graphene layer, which enhances the performance of GFETs devices, we suggest the ion-transport (Li^+) mechanism, as schematically presented in Figs. 2(a) and 2(b). The origin of the graphene bandgap is only possible because of the Li^+ ion, which traps it in the graphene layer. Since the gate dielectric Li_5AlO_4 is polycrystalline in nature, mobile Li^+ ions are not bound in an ordered structure. The atomic radius of the Li^+ ion is also very small, so it has the option of moving anywhere in the crystal lattice. Therefore, after graphene deposition, some lighter Li^+ ions move up and easily trap the voids of graphene, which provide room for the Li^+ ion. Such a kind of intercalation of Li^+ has been reported in a large number of literature studies.[12,17,18] As we increase the channel length from 0.2 mm to 1.65 mm, the Li^+ ion finds a large space to trap the graphene layer, and the energy bandgap of graphene increases simultaneously, resulting in the increase in the current saturation, on/off ratio, and mobility. However, a further increase in channel length degrades the device performance, with a decrease in the mobility, current saturation, and on/off ratio because of dominating charge carrier scattering and trapping phenomena. The variation in the on/off ratio with channel length is shown in Figs. 2(c) and 2(d).

A. Contact resistance of GFETs

Since the contact resistance (R_C) of the source/drain (S/D) electrode of a graphene transistor plays a crucial role in the performance of the device, the transfer length method (TLM) has been used to extract this parameter. According to the TLM method, the total channel resistance R_{tot} of a GFET is related by following equation:[19]

$$\mathbf{R_{tot} = (R_S/W)L + 2R_C/W,} \quad (2)$$

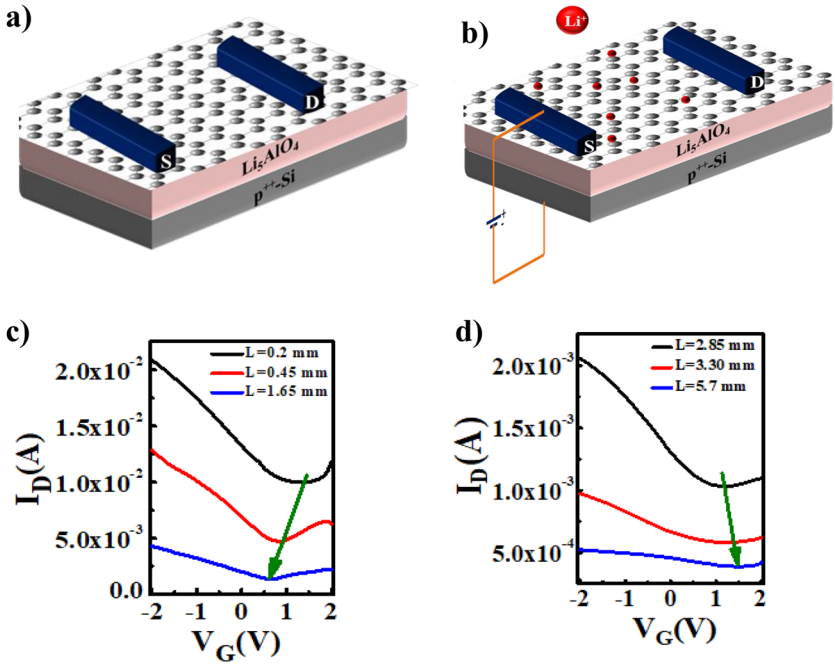

FIG. 2. (a) Schematic illustration of the device structure of back-gated graphene transistors, (b) the channel length-dependent Li^+ ion effect in graphene transistors, and [(c) and (d)] transfer characteristics of back-gated graphene transistors at V_d = −2 V with different channel lengths.

Here, R_S and R_C are the sheet resistance and contact resistance, respectively. R_{tot} of each GFET was determined from the linear part of the I_D–V_D curve at V_G = 0 V. Variation in R_{tot} with different channel lengths is plotted in Fig. 3(a), which indicates that the total channel resistance of a GFET gradually increases from 0.825 KΩ to 2.490 KΩ when the channel length varies from 0.2 mm to 5.7 mm. The sheet resistance (Rs) of single-layer graphene was determined by the four-probe method, which is equal to 0.292 KΩ/sq. By using these sets of R_{tot} and R_S values, R_C values of each GFET were extracted by using Eq. (2), and the variation in R_C with different channel length is plotted in Fig. 3(b). As it was initially observed, R_C decreases from 0.162 KΩ to 0.135 KΩ when the channel length increases from 0.2 mm to 1.56 mm. However, R_C increases rapidly with a further increase in channel length. The variation in R_{tot} and R_C with different channel lengths is summarized in Table I. Again, it is to be noted that our best performance GFET was obtained with this least R_C device of 1.56 mm channel length. Therefore, it can be concluded that the performance of these GFETs strongly depends on the contact resistance of the devices. Besides this contact resistance study, we carried out systematic studies for the variation in transconductance and normalized transconductance with the channel length of the device. When transconductance of the device has been normalized with W/L and source-to-drain bias, the highest value of normalized transconductance is achieved for 1.65 mm channel length (Fig. S5). These data indicate that by optimizing the normalized transconductance value, it becomes possible to achieve the optimum geometry of the device for a better current saturation of a GFET. Details of this study are given in the supplementary material (Sec. 8).

In conclusion, we have demonstrated a new fabrication method of low operating voltage large channel length graphene FETs with current saturation using an ion-conducting oxide gate dielectric (Li_5AlO_4). These GFETs required only 2.0 V to operate with high performance. A systematic study with variable channel length revealed that a high on/off ratio and mobility are achieved with a channel length of 1.65 mm. The Dirac point voltage of the GFETs is

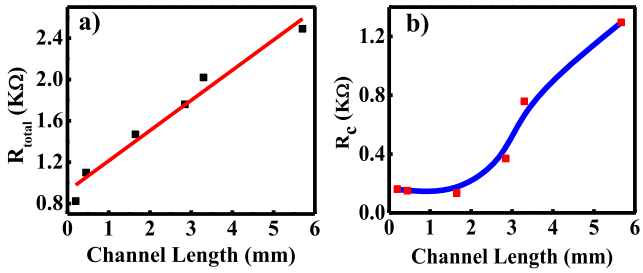

FIG. 3. (a) Variation in total resistance with different channel lengths and (b) variation in contact resistance of the device with different channel lengths.

TABLE I. Summary of R_{tot} and R_C of different channel length GFETs.

Device No.	Channel length L (in mm)	W/L	Total resistance (R_{tot}) in KΩ	Contact resistance (R_C) in KΩ cm
1	0.20	118	0.825	0.162
2	0.45	20	1.142	0.151
3	1.65	5.5	1.471	0.135
4	2.85	3.15	1.760	0.371
5	3.30	2.72	2.020	0.759
6	5.70	1.57	2.490	1.296

also minimized up to 0.6 V with a channel length of 1.65 mm. Interestingly, similar channel length GFETs with conventional p^+-Si/SiO_2 show only a metallic behavior without any gate voltage dependence variation of current. This observation indicates that the Li^+ ion of the Li_5AlO_4 ionic gate dielectric plays an important role and switches the metallic nature of graphene to the semiconducting nature, which was predicted earlier by theoretical studies. Furthermore, we have also demonstrated channel length-dependent normalized transconductance of GFETs, and the highest value of 5.32 mS has been achieved with 1.65 mm channel length, indicating that the current saturation can be adjusted by optimizing the normalized transconductance of the device. Combined with the growth of large-area CVD graphene, this simple sol–gel based ionic gate dielectric could open up a thrilling opportunity for long channel length fabrication of high-performance graphene transistors.

SUPPLEMENTARY MATERIAL

The supplementary material for the synthesis of graphene, graphene characterization, and the GFET with different channel lengths has been provided.

AUTHORS' CONTRIBUTIONS

N.K.C. and V.K.S. contributed equally to this work.

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DATA AVAILABILITY

The data that support the findings of this study are available within the article and its supplementary material.

REFERENCES

[1]X. Du, I. Skachko, A. Barker, and E. Y. Andrei, Nat. Nanotechnol. **3**(8), 491 (2008).
[2]A. K. Geim, Science **324**(5934), 1530 (2009).
[3]F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010).
[4]Y. Yu Wang and P. J. Burke, Appl. Phys. Lett. **103**(5), 052103 (2013).
[5]Q. Yan, B. Huang, J. Yu, F. Zheng, J. Zang, J. Wu, B.-L. Gu, F. Liu, and W. Duan, Nano Lett. **7**(6), 1469–1473 (2007).
[6]K. Tsukagoshi, S.-L. Li, H. Miyazaki, A. Aparecido-Ferreira, and S. Nakaharai, J. Phys. D: Appl. Phys. **47**(9), 094003 (2014).
[7]F. Xia, D. B. Farmer, Y.-m. Lin, and P. Avouris, Nano Lett. **10**(2), 715–718 (2010).
[8]S. Mukherjee and T. Kaloni, J. Nanopart. Res. **14**(8), 1059 (2012).
[9]G. Lu, K. Yu, Z. Wen, and J. Chen, Nanoscale **5**(4), 1353–1368 (2013).
[10]M. Ye, R. Quhe, J. Zheng, Z. Ni, Y. Wang, Y. Yuan, G. Tse, J. Shi, Z. Gao, and J. Lu, Physica E **59**, 60–65 (2014).
[11]M. Farjam and H. Rafii-Tabar, Phys. Rev. B **79**(4), 045417 (2009).
[12]C. Virojanadara, S. Watcharinyanon, A. A. Zakharov, and L. I. Johansson, Phys. Rev. B **82**(20), 205402 (2010).
[13]N. M. Caffrey, L. I. Johansson, C. Xia, R. Armiento, I. A. Abrikosov, and C. Jacobi, Phys. Rev. B **93**(19), 195421 (2016).
[14]Y. Wang, B.-C. Huang, M. Zhang, and J. C. S. Woo, Microelectron. Reliab. **52**(8), 1602–1605 (2012).
[15]B. J. Kim, H. Jang, S.-K. Lee, B. H. Hong, J.-H. Ahn, and J. H. Cho, Nano Lett. **10**(9), 3464–3466 (2010).
[16]W. Xu, T.-S. Lim, H.-K. Seo, S.-Y. Min, H. Cho, M.-H. Park, Y.-H. Kim, and T.-W. Lee, Small **10**(10), 1999–2005 (2014).
[17]R. Mintae, L. Paengro, K. Jingul, P. Heemin, and C. Jinwook, Nanotechnology **27**(31), 31LT03 (2016).
[18]F. Bisti, G. Profeta, H. Vita, M. Donarelli, F. Perrozzi, P. M. Sheverdyaeva, P. Moras, K. Horn, and L. Ottaviano, Phys. Rev. B **91**(24), 245411 (2015).
[19]H. Zhong, Z. Zhang, H. Xu, C. Qiu, and L.-M. Peng, AIP Adv. **5**(5), 057136 (2015).