5

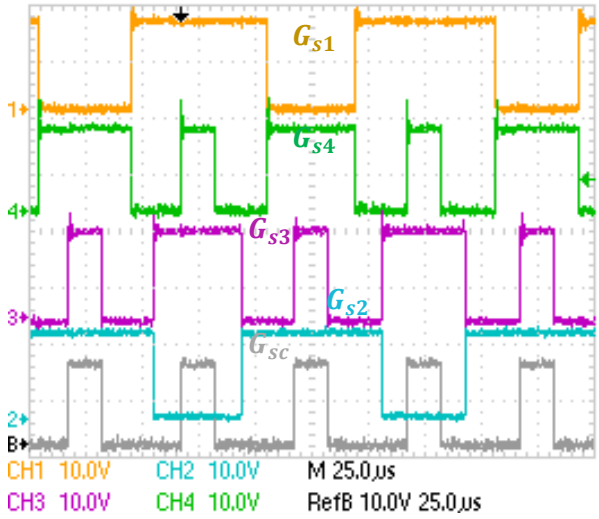
EXPERIMENTAL VERIFICATION

5.1 Introduction

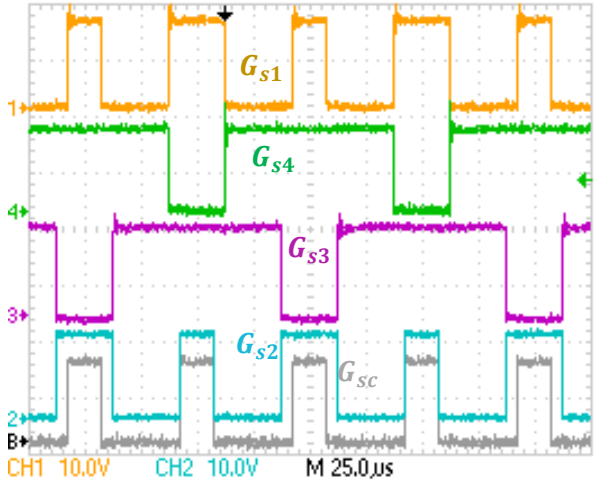
In this chapter, experimental verification of all the proposed converters is carried out. The experimental results of PWM signals generations, steady-state and dynamic operation along with the switch stress are shown presented. The detailed experimental verification of the proposed converters is given in subsequent subsections.

5.2 Verification of Minimum Phase Quadratic Boost Hybrid Inverter

The proposed hybrid inverter is validated through experimental results. The parameters with their attributes are listed in the Table 2.3. For experimental verification the gate pulses are generated through DSP TMS320F28335 kit. The experimental results of the gating signals to switches $G_{s1} - G_{s4}$ and G_{sc} are shown in Fig. 5.1 for $D = 0.4$ and $M = 0.5$. Figs. 5.1 (a) and (b) shows the experimental results of the gating signal given to the switches of the proposed hybrid inverter when $V_{ref} > 0$ and $V_{ref} < 0$, respectively.



(a)

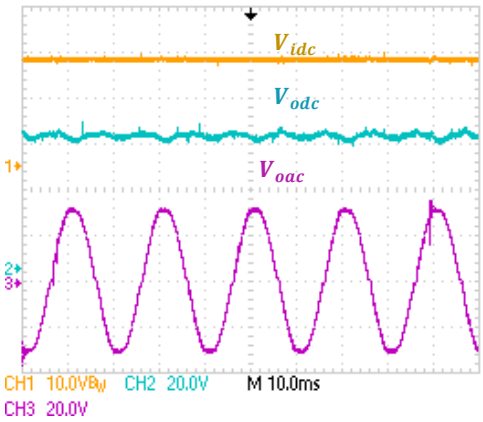


(b)

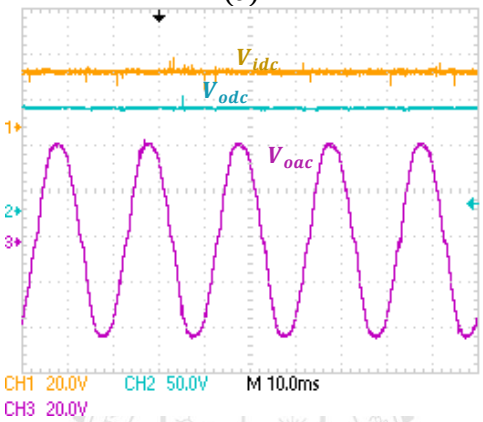
Fig. 5.1 Experimental PWM generation for the proposed hybrid inverter (a) when V_{ref} > 0, (b) when V_{ref} < 0.

5.2.1 Steady-State Operation

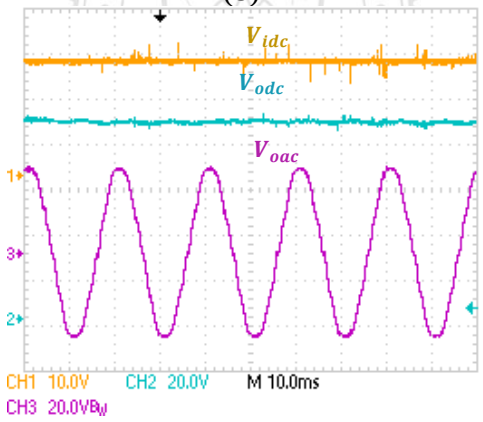
The proposed hybrid inverter is verified experimentally on a 200 W prototype and the results are shown in Figs. 5.2 (a), (b) and (c) for different values of D and M_i. Fig. 5.2 (a) shows the steady state behavior of the proposed hybrid inverter experimentally for D = 0.4 and M = 0.5. It can be observed for Fig. 5.2 (a) that for V_{idc} = 24 V, the hybrid inverter gives dc output voltage V_{odc}= 61.9 V and the AC output voltage V_{oac}= 60.2V (peak-peak). Fig. 5.2 (b) shows the steady state experimental results with for D = 0.6



(a)



(b)



(c)

Fig. 5.2. Experimental steady-state verification (a) operating at D = 0.4 and M = 0.5, (b) D = 0.6 and M = 0.4, (c) D = 0.5 and M = 0.5.

and M = 0.4. It is seen from Fig. 5.2 (b) that for D = 0.6, M = 0.4 and V_{idc} = 24 V, the hybrid inverter gives dc output voltage V_{odc} = 118 V and the AC output voltage V_{oac}= 87.4 V (peak-peak). Fig. 5.2 (c) shows the results for same value of duty and modulation index, i.e., D = M = 0.5. It can be observed from Fig. 5.2(c) that for D = M = 0.5 and V_{idc} = 24 V, the hybrid inverter gives dc output voltage V_{odc} = 86.8 V

and the ac output voltage V_{oac} = 72.1 V (peak-peak). Thus, results in Figs. 5.2 confirm the high voltage step-up property and other steady state behavior of the proposed hybrid inverter for different values of D and M.

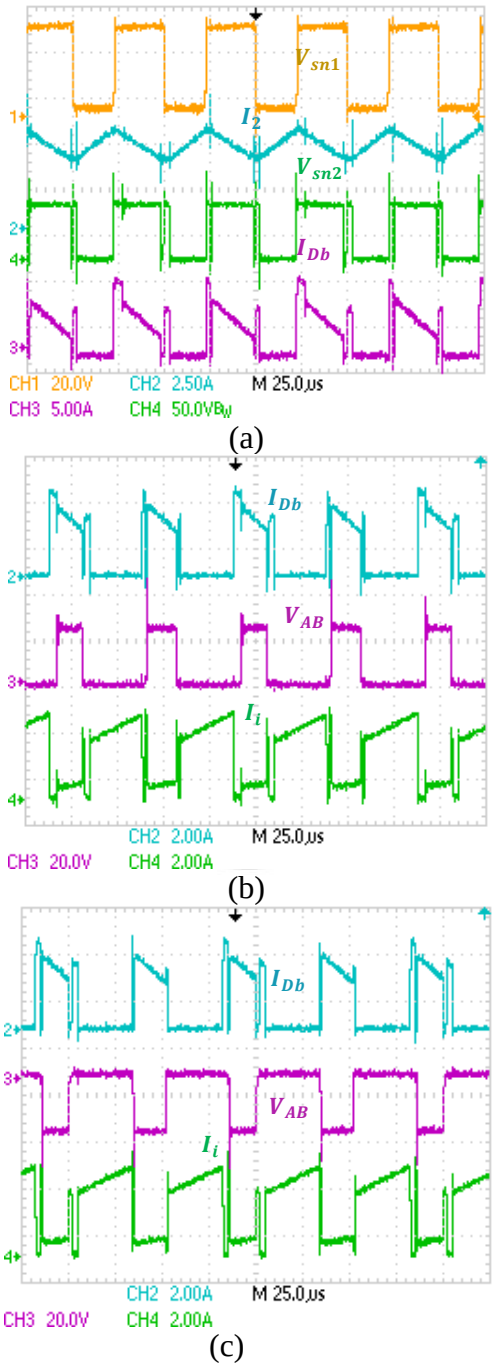


Fig. 5.3. Operational switching waveforms of proposed hybrid inverter (a) switch node voltages, (b) switching waveforms for $V_{AB} > 0$, D = 0.6 and M =0.4, (c) switching waveforms $V_{AB} < 0$ for D = 0.6 and M =0.4.

Fig. 5.3 shows the experimental switching waveforms ($V_{sn1}, V_{sn2}, I_{d2}, I_2$) of the proposed hybrid inverter. The Fig. 5.3(a) verifies the switching waveforms of the proposed hybrid inverter. Verification of inverter bridge voltage V_{AB} is given in Figs. 5.3(b) and (c) for $V_{AB} > 0$ and $V_{AB} < 0$, respectively for D = 0.6 and M = 0.4.

TABLE 5.1
EXPERIMENTAL AND THEORETICAL COMPARISONS

Parameters		Validation Value	
		Theoretical	Experimental
V_{idc}		24	24
V_{sn1}	S_c off	40	37.1
	S_c on	0	0
V_{c1}		40	37.1
V_{sn2}	S_i off	66.67	61.9
	S_i on	0	0
V_{odc}		66.67	61.9
V_{opk}		66.67	60.2

5.2.2 Performance Analysis

The experimental and theoretical results for the proposed hybrid inverter are tabulated in the Table 5.1. The small differences between the experimental and theoretical results are due to non-idealities such as inductor dc resistance, capacitor equivalent series resistance, on state resistance of switches and forward voltage drops of the diodes. Table 5.1 gives a complete comparative analysis between the proposed hybrid inverter and the classical inverters discussed in [18], [29], [83], [86-87] to distinguish the property of the proposed inverter.

TABLE 5.2
COMPARISON OF PROPOSED HYBRID INVERTER WITH OTHER INVERTERS

Ref.	No. of Switches	B	Duty cycle Limitations	G	RHP Zero	Control Elements	ac and dc output
[18]	5	$\frac{1}{(1-2D)}$	$0 < D < 0.5$	$\frac{M}{2M-1}$	Yes	4	No
[29]	6	$\frac{1}{(1-D)}$	$0 < D < 1$	1	Yes	4	Yes
[83]	7	$\frac{(1-D)}{(1-2D)}$	$0 < D < 0.5$	$\frac{M^2}{2M-1}$	Yes	5	Yes
[86]	7	$\frac{1}{(1-2D)}$	$0 < D < 0.5$	$\frac{M}{2M-1}$	Yes	5	Yes
[87]	7	$\frac{1}{(1-2D)}$	$0 < D < 0.5$	$\frac{M}{2M-1}$	Yes	5	Yes
Proposed Inverter	7	$\frac{1}{(1-D)^2}$	$0 < D < 1$	$\frac{1}{M}$	No	5	Yes

Figs. 5.4 (a), (b), (c) and (d) show the graph between output voltages and the loads current for the proposed hybrid inverter. Fig. 5.4 (a) shows the plot between the dc output voltage vs dc load current while keeping other parameters constant. Fig. 5.4 (a) confirms that for the dc load variations, dc output voltage remains constant and there is a good match between the theoretical and experimental dc output voltages. Similarly, Fig. 5.4 (b) shows the plot between the ac output voltage vs dc load current while keeping other parameters constant. Fig. 5.4 (b) confirms that for the ac load variations, peak value of ac output voltage remains constant and there is a good match between the theoretical and experimental values. Fig. 5.4 (c) verifies that for smooth variation in ac load, the dc output voltage remains constant. In the same way, Fig. 5.4 (d) verifies that for smooth change in the ac load current, the ac output remains same. Thus, plots in Fig. 5.4 confirm that the hybrid inverter output voltages (both ac and dc) remain almost constant for the smooth changes in dc and ac loads and hence, it validate the voltage source property of the proposed hybrid inverter.

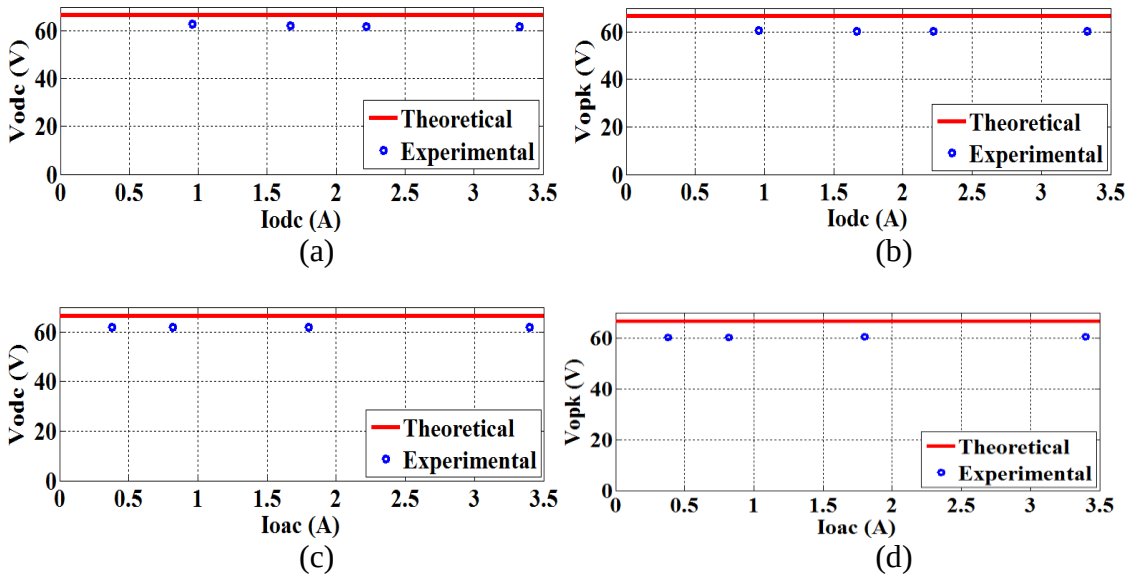


Fig. 5.4. Performce of the hybrid inverter (a) effect of changing R_{odc} on V_{odc}, (b) effect of changing R_{odc} on V_{opk}, (c) effect of changing R_{oac} on V_{odc}, (d) effect of changing R_{oac} on V_{opk} .

5.2.3 Dynamic Load Variation Analysis

The experimental results of the dynamic behaviour for the change in the load of the proposed hybrid inverter is shown in Fig. 5.5. As shown in Fig. 5.5 (a), the performance of the hybrid inverter for the step up change in the dc load current while keeping the ac load constant. It can be observed from Fig. 5.5 (a) that for step up change in the dc load, there is a minor dip in the dc output voltage (V_{odc}) whereas the ac load voltages and currents are unaffected. Similarly, Fig. 5.5 (b) shows the performance of the hybrid inverter for the step down change in the dc load current while keeping ac load constant. It can be observed from Fig. 5.5 (b) that for step down change in the dc load, there is a minor swell in the dc output voltage *(V_{odc})* whereas ac load voltages and currents are unaffected. Fig. 5.5 (c) shows the performance of the proposed hybrid inverter for dynamic increase in the ac load while keeping the dc load constant. It is evident from Fig. 5.5 (c) that for sudden dynamic increase in the ac load current, there is a minor dip in the ac voltage and the dc outputs (voltage and current)

remain same. Likewise, Fig. 5.5 (d) shows the performance of the proposed hybrid inverter for step down transient in the ac load while keeping the dc loads constant. It can be seen from Fig. 5.5 (d) that for step down transient in the ac load current, there is a minor swell in the ac voltage and the dc output voltage and current remain same.

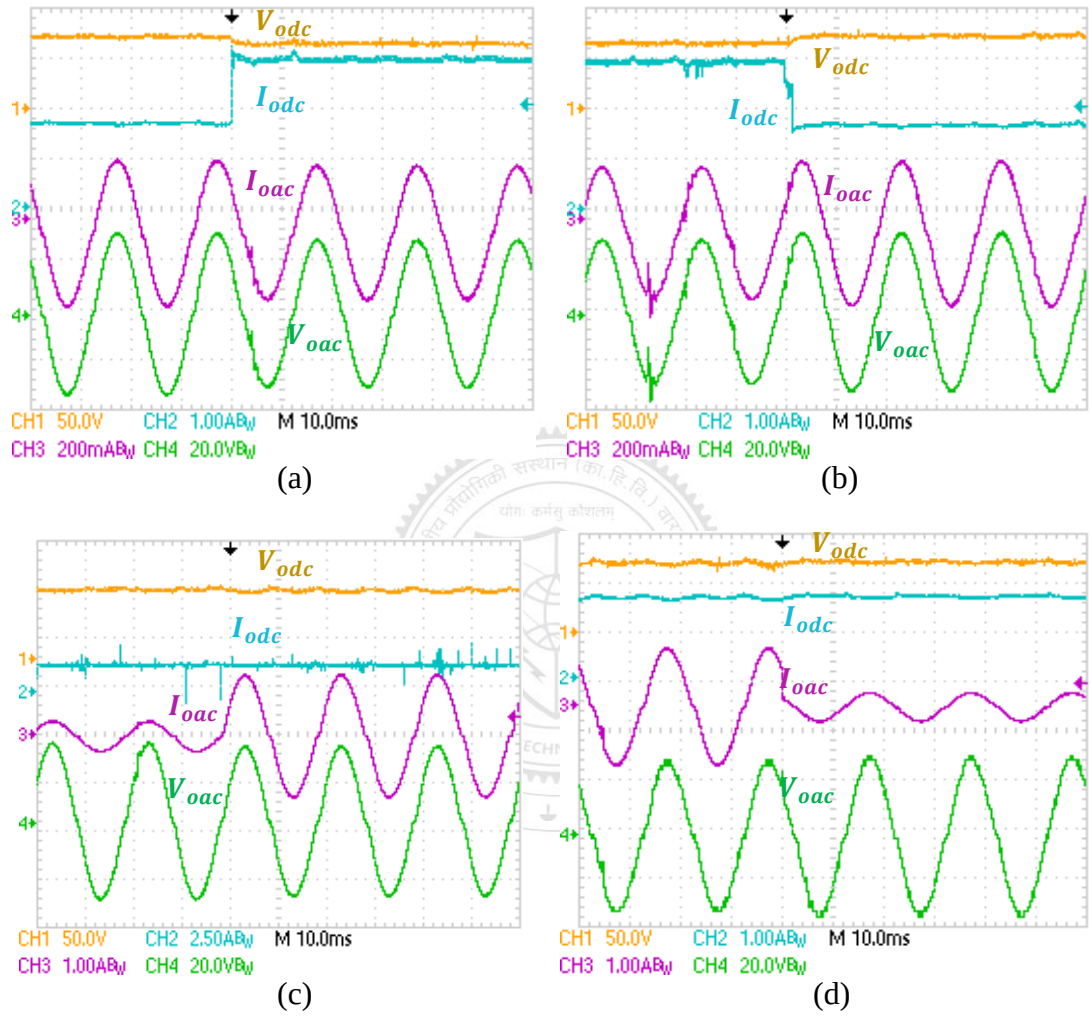


Fig. 5.5. Dynamic performance of the proposed hybrid inverter (a) step up change in the dc load curent, (b) step down change in dc load ,(c) step up change in the ac load current, (d) step down change in ac load current.

5.3 Verification of Quadratic Boost Derived Hybrid Multi-Output Converters

The proposed quadratic boost derived hybrid multi-output converter topologies are experimentally validated with 250 W prototype. DSP F28335 kit is used for implementing the hybrid PWM and for validating the proposed concept experimentally.

Parameters with their attributes are listed in the Table 2.3 and the components detailed are given in Table 5.3 with manufacturer. The experimental verification of PWM signals are shown in Fig. 5.6. The non-idealities of the inverter such as capacitor equivalent series resistance, inductor dc resistance, on state resistance of switches and forward voltage drops of the diodes are same as considered for the simulations analysis. The values of these non idealities are taken according to the experimental setup and are 1) dc resistance of inductor $r_L = 0.2\ \Omega$, 2) equivalent series resistance of the capacitor r_C = 0.035Ω, 3) switches forward voltage drop V_{FS} = 1.1V 4) switches ON state resistance r_S = 0.15Ω, and 5) diode forward voltage drop V_{FD}= 0.7V.

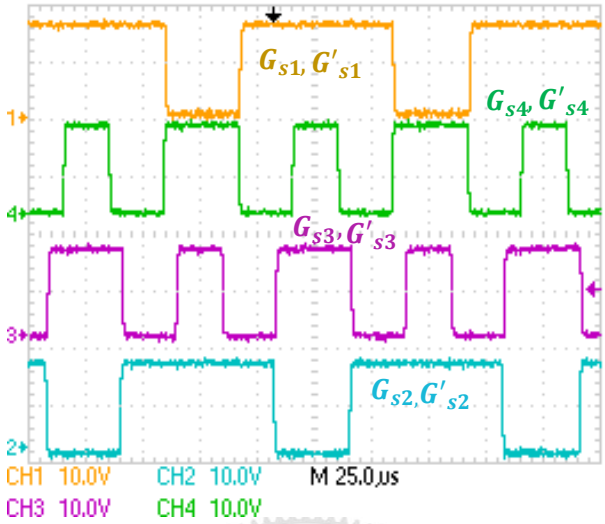
TABLE 5.3.
LISTS OF COMPONENTS USED FOR MULTI-OUTPUT CONVERTERS

Component List	
Components	**Manufacturer**
Inverter Switches	IRGP4790D (I.R.Corp.)
Diodes(D_a, D_b, D_c)	RURG5060(Fairchild)
Gate Drivers	FOD3184 (Fairchild)

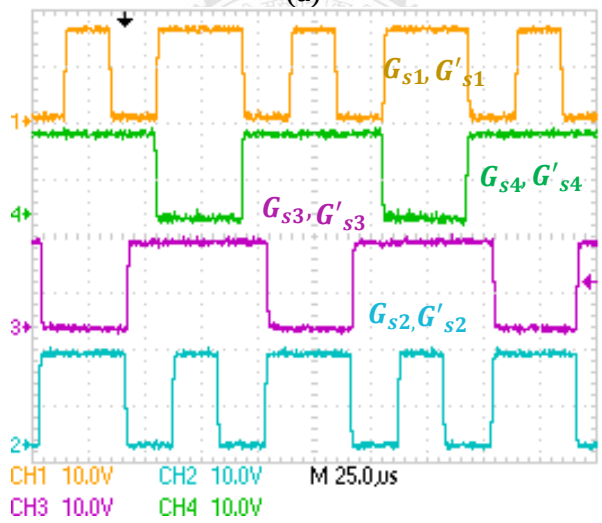
5.3.1 Proposed Converter in Parallel Mode

The proposed parallel mode concept is verified for the total load power of 250W (P_{dc} =150 W and P_{ac} =100 W). Experimental waveforms of hybrid PWM are shown in Figs. 5.6(a) and 5.6(b). In parallel converter topology, same switch node voltage is appeared across the parallel inverters and current drawn by the inverters are divided according to the ac loads. Steady state experimental verifications are shown in Fig. 5.7(a) and 5.7(b) for D = 0.4, M=0.5 and D = 0.5, M=0.4 respectively. From the Fig. 5.7(a), it can be observed that two ac output voltages V_{ac1} = 39.4V (pk-pk) and V_{ac2} = 39.0 V (pk-pk) along with dc output voltage V_{dc} = 57.12 V are obtained for the input voltage V_{in} = 24 V. Similarly, it can be observed from Fig. 5.7(b), that the proposed converter give two ac output voltages V_{ac1} = 47.6 V (pk-pk) and V_{ac2} = 46.4 V (pk-pk) along with dc output

voltage V_{dc} = 82.2V for the input voltage V_{in} = 24V. The experimental results confirm the steady state behavior of the proposed multi-output parallel mode topology for different values of D and M.



(a)



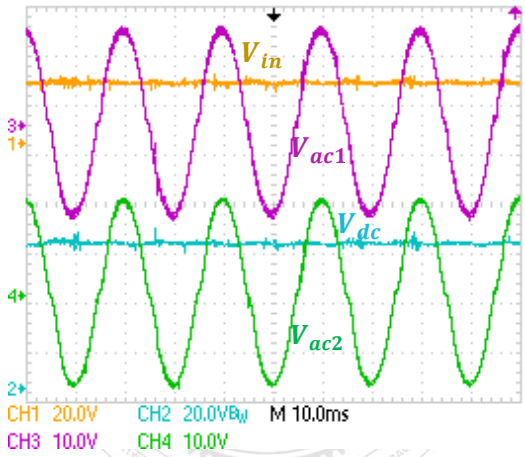
(b)

Fig. 5.6. Verification of PWM for proposed converter (D = 0.4 and M = 0.5) (a) PWM pattern when $V_{ref} > 0$, (b) PWM pattern when $V_{ref} < 0$.

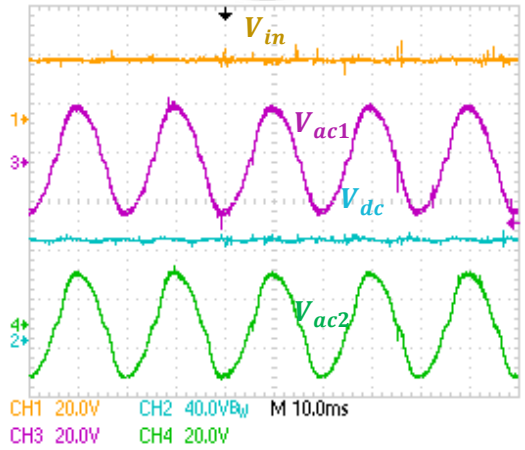
5.3.2 Proposed Converter in Series Mode

In series converter topology, current drawn by the inverters is same and switch node voltage is divided according to the ac loads. Steady state experimental results of the proposed converter considering non-idealities for two series ac and one dc outputs for D = 0.4 and M=0.5 are shown in Fig. 5.8. Steady state experimental verifications are

shown in Fig. 5.8(a) and 5.8(b) for D = 0.4, M=0.5 and D = 0.5, M=0.4, respectively. It is clear from Fig. 5.8(a), that two series ac output voltages V_{ac1} = 18.6V (pk-pk) and V_{ac2} = 19.7V (pk-pk) along with dc output voltage V_{dc} = 62.1V are obtained for the input voltage V_{in} = 24V, D = 0.4, and M = 0.5. Similarly, from Fig. 5.8(b), it can be observed that two ac output voltages V_{ac1} = 24.4 V (pk-pk) and V_{ac2} = 23.9V (pk-pk) along with dc output voltage V_{dc} = 73.2V are obtained for the input voltage V_{in} = 24 V, D = 0.5 and M=0.4. The, experimental results confirm the steady state behavior of the proposed multi-output series mode topology for different values of D and M.

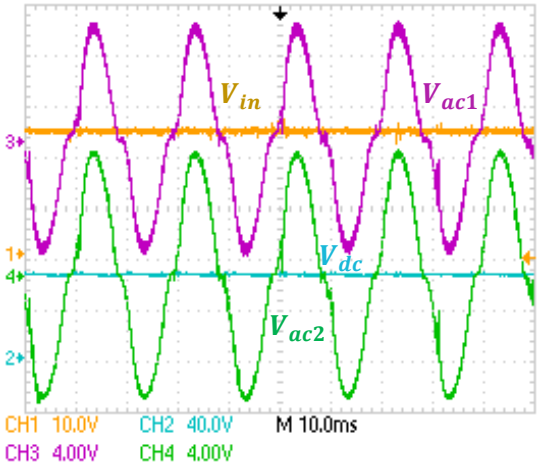


(a)

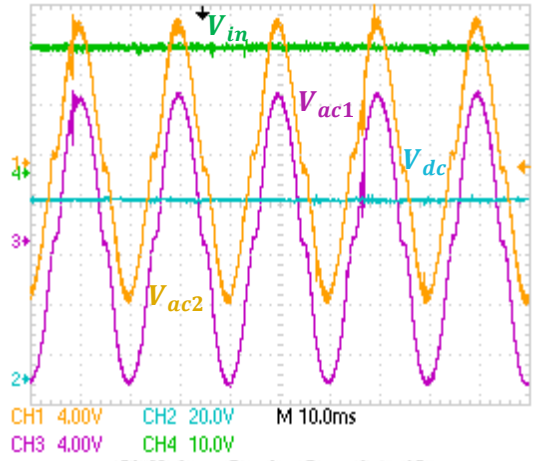


(b)

Fig. 5.7. Experimental verification for simultaneously two ac and one dc output hybrid parallel converter (a) verification of parallel topology hybrid multi-output converter operating at D = 0.4 and M = 0.5, (b) verification of parallel topology hybrid multi-output converter operating at D = 0.5 and M = 0.4.



(a)



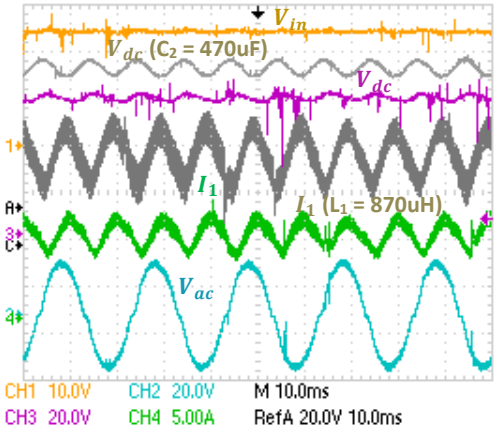
(b)

Fig. 5.8. Experimental verification for simultaneously two ac and one dc output series hybrid converter (a) verification of series topology hybrid multi-output converter operating at D = 0.4 and M = 0.5, (b) verification of series topology hybrid multi-output converter operating at D = 0.5 and M = 0.4.

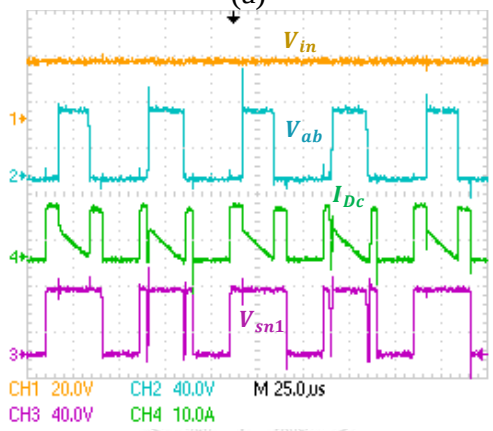
5.3.3 Experimental Performance analysis

For the analysis of current and voltage profiles of the proposed converter, some experimental results for D= 0.4 and M=0.5 are shown in Fig. 5.9. Fig. 5.9(a) shows the voltages and currents ripple information of the proposed converter. From Fig. 5.9(a) double frequency ripple content can be observed in input dc current (I_1) and output dc voltage (V_{dc}) profiles. It is important to note that the double frequency ripple magnitude can be reduced by selecting proper inductor and capacitor values. Figs. 5.9(b) and

5.9(c) show the current (I_{Dc}) through the diode D_2, switch node voltage (V_{sn1}) and inverter bridge voltage (V_{ab}) in positive and negative half cycles respectively.



(a)



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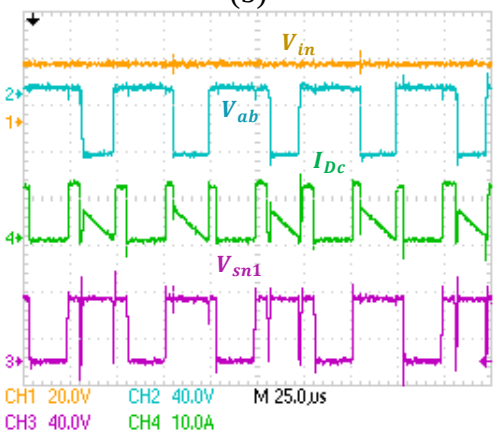


(c)

Fig. 5. 9. Operational waveform of proposed hybrid converter (a) Steady state input current and output voltage, (b) switching currents and voltages when $V_{ab} > 0$, (c) switching currents and voltages when $V_{ab} < 0$.

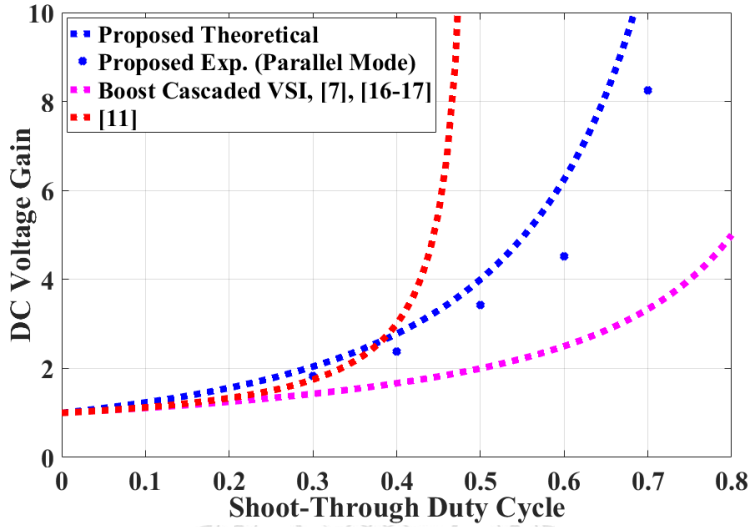
TABLE 5.4
COMPARISON OF PROPOSED HYBRID MULTI-OUTPUT CONVERTERS

Attributes	Proposed Converter		Boost Cascaded VSI	[29]	[30]	[31]	[110]
	Series Topologies	Parallel Topologies					
DC output	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Dead Time requirement	No	No	Yes	No	No	No	No
Multi-ac output	Yes	Yes	No	No	No	No	No
Number of Passive components	2+2	2+2	1+1	1+1	1+1	1+1	1+1
Number of switch	4+4	4+4	5	4	5	6	5
Number of Diode	3	3	1	1	5	0	2
Boost Factor	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)}$	$\frac{1}{(1-D)}$	$\frac{1}{(1-D)}$	$\frac{(1-D)}{(1-2D)}$	$\frac{(1-D)}{(1-2D)}$
Modulation Index (M)	M < (1-D)	M < (1-D)	M < 1	M < (1-D)	M < (1-D)	M < (1-D)	M < (1-D)
Peak ac voltage	$\frac{MV_{in}}{2(1-D)^2}$	$\frac{MV_{in}}{(1-D)^2}$	$\frac{MV_{in}}{(1-D)}$	$\frac{MV_{in}}{(1-D)}$	$\frac{MV_{in}}{(1-D)}$	$\frac{MV_{in}(1-D)}{(1-2D)}$	$\frac{MV_{in}(1-D)}{(1-2D)}$

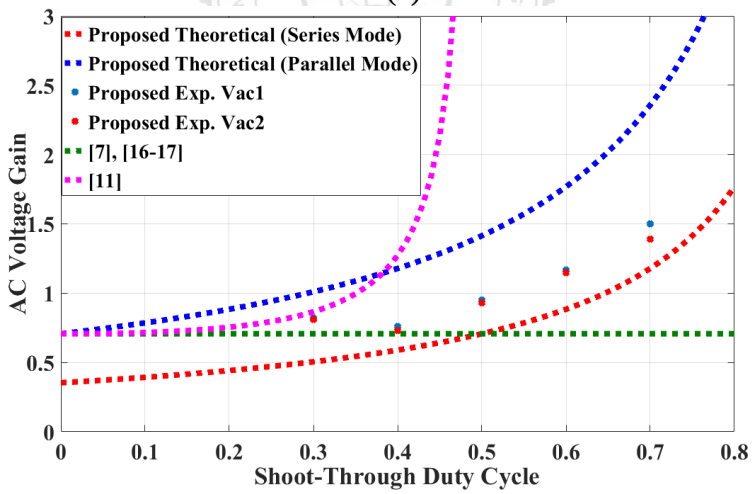
Further, in order to compare the performance of proposed converters, some closely related hybrid converters are considered. A complete comparative analysis between the proposed multi-output converter and other closely related converters are shown in Table 5.4. Some comparative observations between the proposed converter topologies and the existing hybrid converters (given in Table 5.4) are following.

1) Comparison of experimental and theoretical voltage gains (dc and ac) between the proposed converters and other conventional hybrid converter [29], [30], [110] is shown in Figs. 5.10(a) and Fig. 5.10(b), respectively It may be observed from Figs. 5.10(a), and 5.10(b) that the converter reported in [110] has less voltage gain up to about 0.4 duty cycle as compared to proposed topologies. Moreover, the converter reported in [110] is limited to less than 0.5 duty cycle whereas proposed topologies can operate with more than 0.5 shoot-through duty

cycle. In addition converter discussed in [110] gives only one dc and one ac outputs whereas the proposed topologies are able to give multi-ac and one dc outputs. Further, it may also be observed from Figs. 5.10(a) and 5.10(b) that the proposed converters give better voltage gains as compared to the other converter topologies discussed in [29]-[30] and can operated for wide duty cycle.



(a)

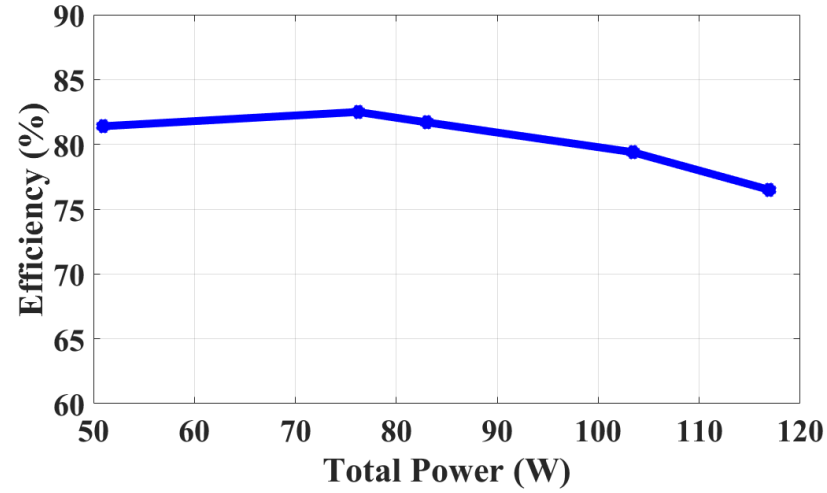


(b)

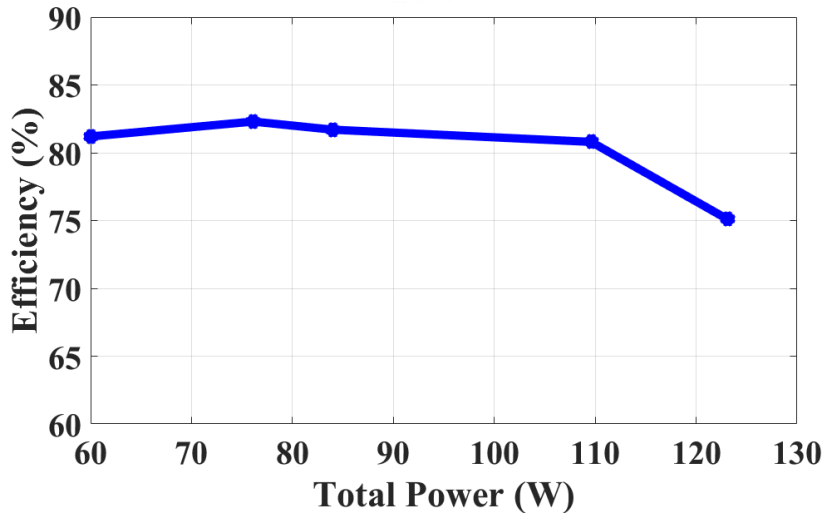
Fig. 5.10. Verification of experimental and calculated gains (a) maximum dc voltage gain w.r.t. D, (b) maximum ac voltage gain w.r.t. D.

2) The boost cascaded VSI topology mentioned in Table 5.4 may fail at the occurrence of a shoot-through event due to EMI noise which cannot be eliminated by using a dead-time circuit. As shoot-through of the inverter leg is

allowed in the proposed topologies, it exhibits better EMI noise immunity as compared to the boost cascaded VSI topology.



(a)



(b)

Fig. 5.11. Measured efficiency analysis of proposed topologies (a) Efficiency curve of the proposed parallel mode multi-output converter, (b) Efficiency curve of the proposed series mode multi-output converter.

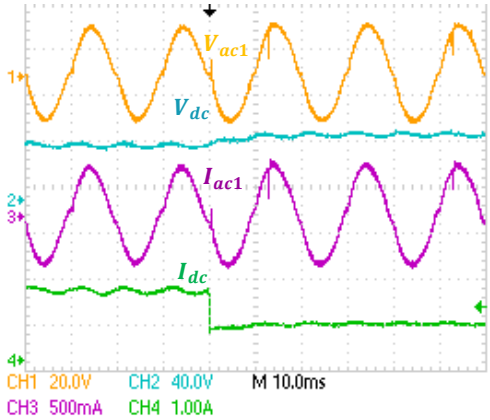
5.3.4 Efficiency Analysis

The measured efficiency analysis is also carried out for the proposed parallel mode hybrid multi-output converter and series mode hybrid multi-output converter and is shown in Figs. 5.11(a) and Fig. 5.11(b), respectively. Note that the efficiency analysis is carried out for boost factor of 2.77 and for all the three (two ac and one dc) load variations. Efficiency curve for the proposed parallel mode hybrid multi-output

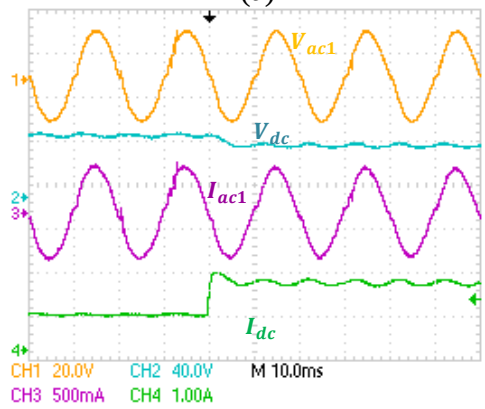
converter is shown in Fig. 5.11(a). It may be observed from Fig. 5.11(a) that the maximum efficiency for the proposed parallel mode multi-output converter is 82.5% at total power of 76.2W. Similarly, efficiency curve of the proposed series mode multi-output converter is shown in Fig. 5.11(b). It may be observed from Fig. 5.11(b) that the maximum efficiency for the proposed series mode multi-output converter is 82.3% at total power of 76.1W. In order to achieve multi outputs, the number of switches and passive filter components are increased in the proposed converters as compared to conventional two output hybrid converters. Thus, the switching, conduction and magnetic losses are slightly increased and therefore, the efficiency of the proposed converters is a bit low as compared to the conventional two output hybrid converters.

5.3.5 Dynamic Load Variation

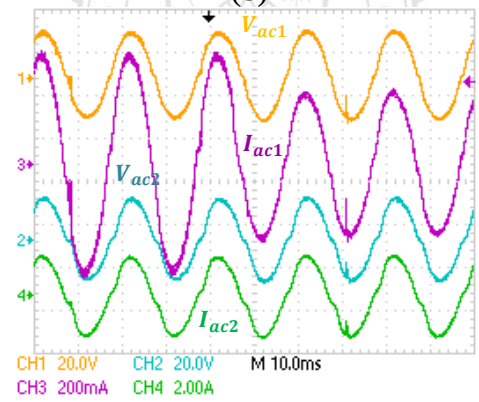
Experimentation is done to verify the dynamic behaviour of the proposed converters in open loop condition with the step change in the loads and the results are shown in Fig. 5.12. From the Fig. 5.12(a), it is clear that the experimental response of the converter for step down dc load (from I_{dc} = 1.65 A to = 800 mA) variation by keeping the ac loads constant. It is evident from Fig. 5.12 (a) that that dc load step down operation, there is small variation in the dc load voltage (V_{dc}) and no variations in the ac output voltage and current. Due to the measurement constraints with the oscilloscope, only one ac output voltage V_{ac1} and output current (I_{ac1}) could be shown Fig. 5.12 (a). Similarly, Fig. 5.12 (b) shows the step up dc load (from I_{dc} = 800 mA to 1.65 A) variation by keeping the ac loads constant. It can be observed from the Fig. 5.12 (b), that for dc step up operation, there is a small variation in the dc load voltage (V_{dc}) and no variations in the ac output voltage (V_{ac1}) and current (I_{ac1}). Fig. 5.12 (c) shows the response of the



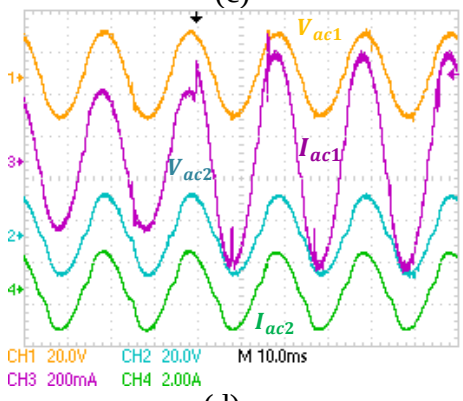
(a)



(b)



(c)



(d)

Fig. 5.12. Dynamic response of the proposed concept (a) Step down change in the dc load current, (b) Step up change in the dc load current, (c) Step down change in the ac load current, (d) Step up change in the ac load current.

converter for step down ac load (from I_{ac1} = 1.1A to = 610 mA) variation while keeping the dc load constant. Similarly from Fig. 5.12 (d), the step up ac load (from I_{ac1} = 610 mA to = 1.1 A) variation while keeping the dc load constant. It is clear from Fig. 5.12 (d) that for a step up operation in one of the ac loads there is no variation in ac load voltages ($V_{ac1}$and V_{ac2}) and other ac load current (I_{ac2}). An important observation is noticed that dc load voltage (V_{dc}) and currents (I_{dc}) are not affected while dynamic change in ac loads.

5.4. Experimental Verification of Switched-Boost Modified ZSI Topologies

In all the proposed ZSIs, the proposed CC-qZSI has continuous input current profile and has less switch capacitor voltage stress. So, experimental verification is performed on proposed CC-qZSI. The experimental setup of proposed work is shown in Fig. 5.13.

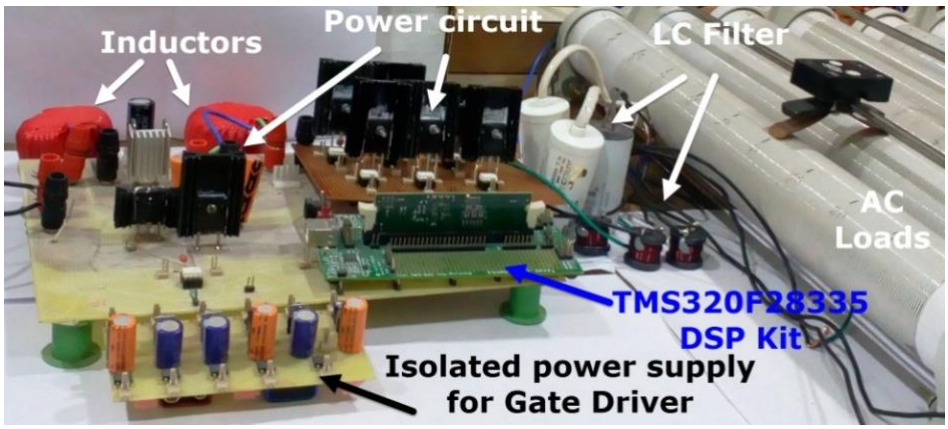
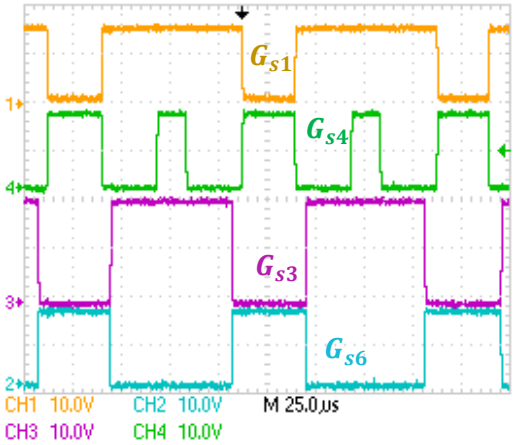
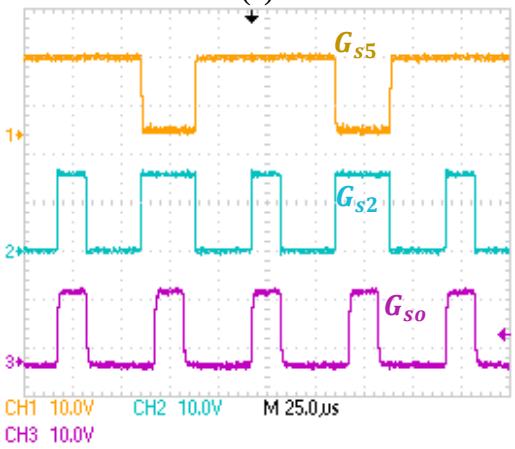


Fig. 5.13. Experimental setup of the proposed work.



(a)

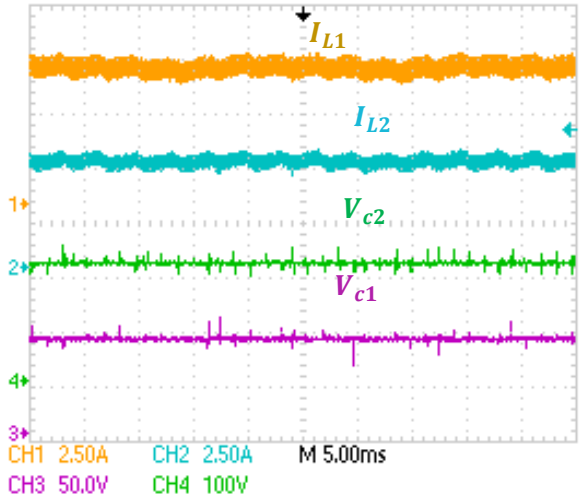


(b)

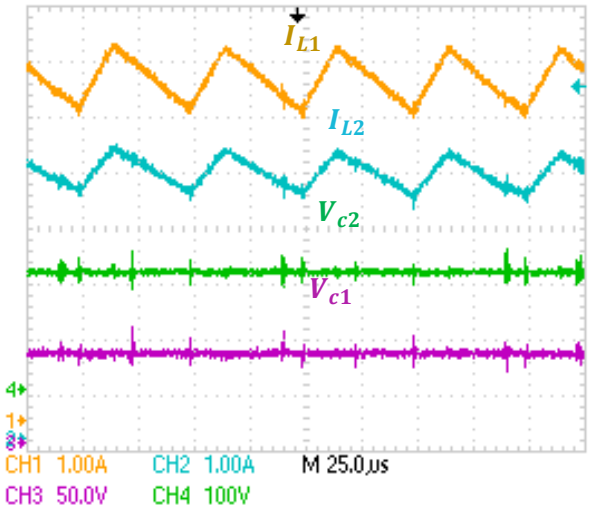
Fig. 5.14. PWM signals at D = 0.3 and M = 0.7 (a) gating signal to switches S_1, S_3, S_4, and S_6, (b) gating signal to switches S_5, S_2, and S_6.

5.4.1 Steady-State Verification of CC-qZSI

To verify the operation of the proposed CC-qZSI, experimental prototype of 500W is developed and PWM signals are generated using TMS320F28335 DSP kit. The experimental waveforms of the PWM signal at gate terminals of the switches for D = 0.3 and M = 0.7 are shown in Fig. 5.14. The steady state operation of the proposed CC-qZSI is given in Fig. 5.15. It is clear from Fig. 5.15(a) that the voltage across the capacitors V_{c1} and V_{c2} are 86.2 V and 215 V, respectively. Fig. 5.15 (b) shows the zoomed view of the results shown in Fig. 5.15(a).



(a)



(b)

Fig. 5. 15. Steady state results (a) inductors currents and capacitor voltages of the proposed CC-qZSI, (b) zoomed view.

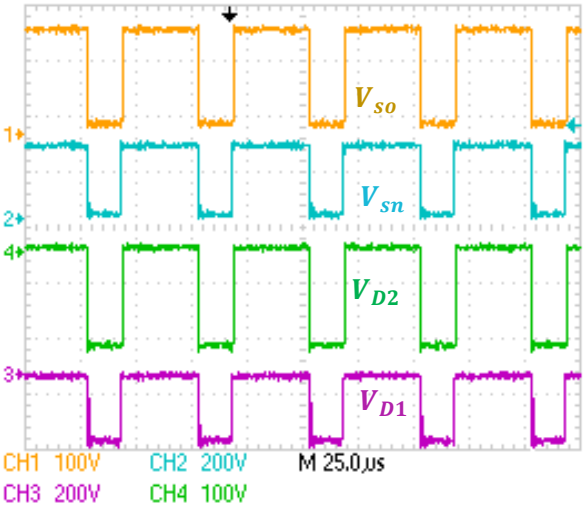
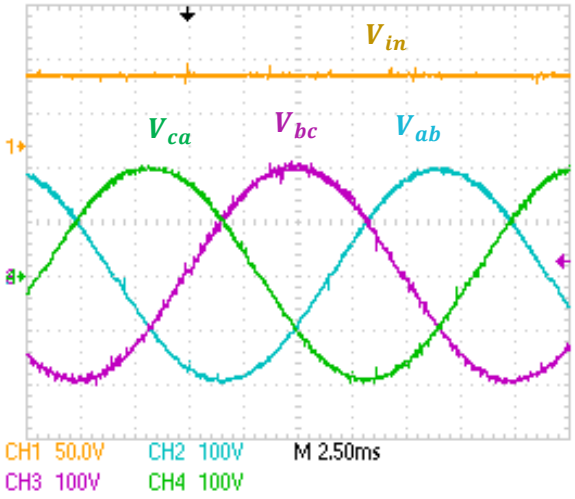
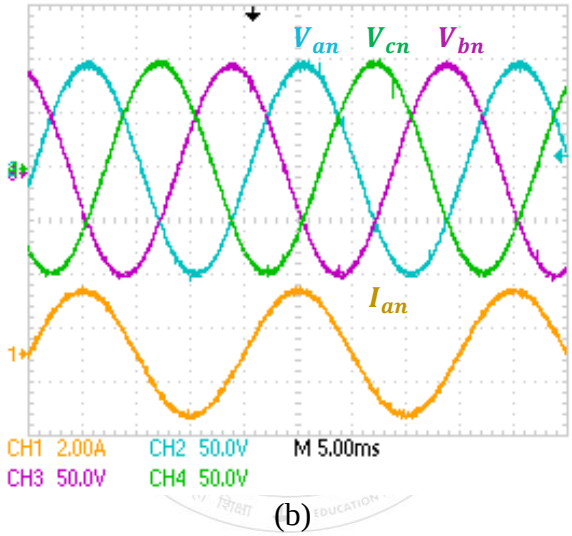


Fig. 5.16. Switches and diodes voltages.



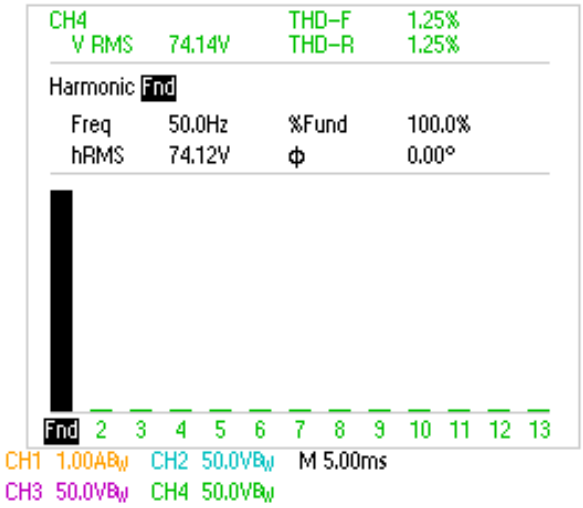
(a)



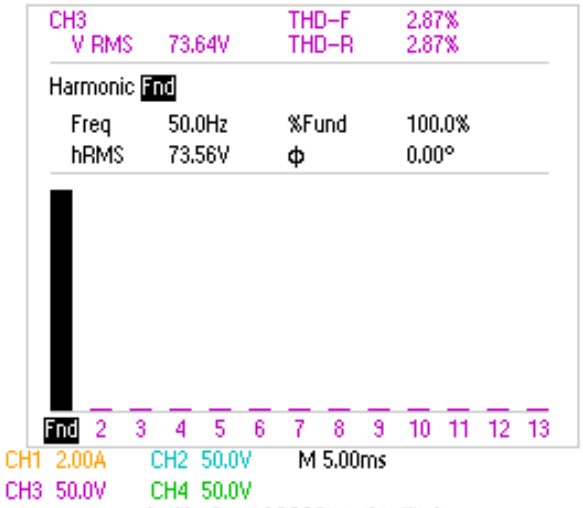
(b)

Fig. 5.17. Steady state output voltages of proposed CC-qZSI (a) input voltage with output line voltages, (b) output phase current and voltages.

The voltage across switches and diodes are shown in the Fig. 5.16. During non-shoot–through duty interval, the voltage across D_1, V_{D1}= 179.4 V and D_2, V_{D2}= 137.6 V. The voltage across the switches are V_{so}= 207 V and V_{sn} = 298 V, respectively during non-shoot-through duty interval. The experimental output line voltages are $V_{ab} = V_{bc} = V_{ca}$ = 396 V (pk- pk) as shown in Fig. 5.17(a). The steady state output phase voltages are shown in Fig. 5.17(b). It is clear from Fig. 5.17(b) that the experimental phase voltages are $V_{an} = V_{bn} = V_{cn}$ = 206 V (pk- pk).



(a)



(b)

Fig. 5.18. Experimental THD (a) proposed CC-qZSI, (b) conventional qZSI.

5.4.2 Harmonic Analysis

The harmonics spectrum of output phase voltage is shown in Fig. 5.18. It can be observed from Fig. 5.18 (a) that the THD of the proposed CC-qZSI is 1.25% at a load voltage of 74.14 V. Further, it can be observed from Fig. 5.18 (b) that for the same load voltage, the THD of the conventional qZSI is 2.87%. Thus, it is clear that the conventional qZSI has higher THD as compared to the proposed CC-qZSI.

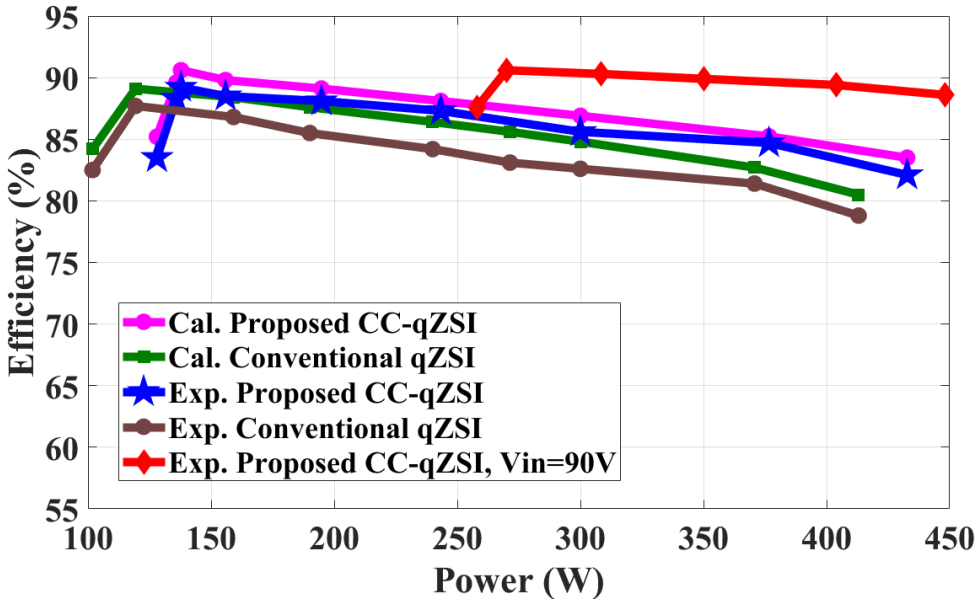


Fig. 5.19. Comparative efficiency analysis.

5.4.3 Efficiency Analysis

The efficiency analysis has also been carried out experimentally and comparative analysis of calculated and experimental efficiency is shown in Fig. 5.19. The experimental efficiency is measured for the boost factor 5.26 and dc input voltage of 65 V for conventional qZSI and the proposed CC-qZSI. It is clear from Fig. 5.19 that the maximum efficiency of the proposed CC-qZSI is 89.2%, whereas the maximum efficiency of the conventional qZSI for the same input voltage is 87.7%. However, the maximum calculated efficiency of the proposed CC-qZSI is 90.6% and that of conventional qZSI is 89.1%. It can also be observed from Fig. 5.19 that if the input voltage is increased to 90 V, the proposed CC-qZSI gives maximum measured efficiency of 90.6%. It can be observed from the results of Fig. 5.19 that the proposed CC-qZSI has higher efficiency than the conventional qZSI for the same input voltage.

5.5 Conclusion

The experimental verification of high gain minimum phase quadratic boost hybrid inverter, quadratic boost derived hybrid multi-output converters and switched boost

modified impedance source inverters topologies are presented in this chapter. The experimental results validate the steady state and dynamic performance of the proposed converter topologies.

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