PROPOSED CONVERTER: 3

SWITCHED-BOOST MODIFIED Z-SOURCE INVERTERS TOPOLOGIES

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4.1. Introduction

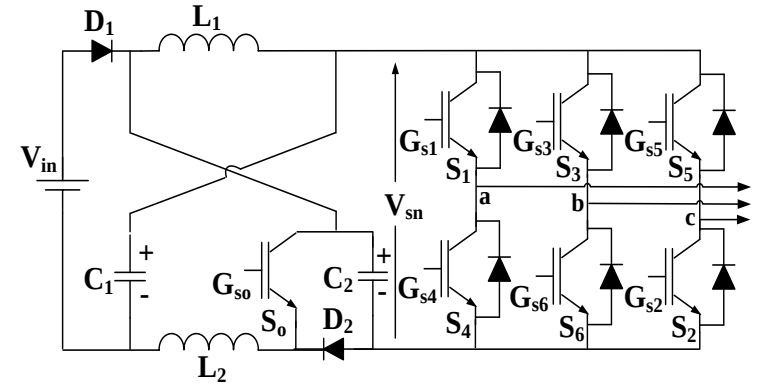
The multi-output quadratic boost converters topologies are capable of giving simultaneous n number of ac and dc outputs. The limitation of the multi-output converter is that it is suited for lower power level. Also, the efficiency is still slightly lesser. This is due to the fact that multi-output converter is derived from the single switch quadratic boost converter. In order to overcome the limitations of multi-output converters, a modified switched-boost ZSIs topologies are presented. The proposed ZSIs are a modified topologies of conventional ZSI in which high gain is achieved without use of extra passive components. Detailed steady-state analysis, PWM control techniques, comparative analysis and simulation studies are performed to validate the feasibility of proposed ZSIs. The detailed descriptions about the proposed converters are given in subsequent subsections.

4.2. Switched-Boost Modified ZSIs Topologies

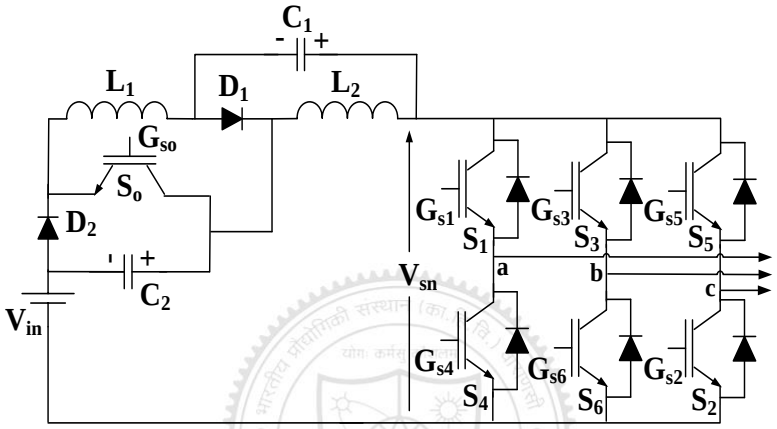
In this thesis, three-phase topologies of switched-boost modified Z-source inverters (ZSIs) with improved boost capability are presented. The improved voltage gain is achieved by adding one auxiliary switch and one diode without using additional passive components. The proposed concept is applied to traditional ZSI, discontinuous input current quasi-ZSI (qZSI) and continuous input current qZSI. In this way, three inverter topologies switched-boost ZSI (SB-ZSI), discontinuous input current qZSI (DC-qZSI) and continuous input current qZSI (CC-qZSI) are evolved. The proposed topologies give high voltage gain at low D as compared to the traditional ZSIs. The proposed ZSIs can be applied to dc-dc and dc-ac power conversion for renewable energy sources where low voltage input and high voltage gain is required. Since for the proposed ZSIs, $M+D \leq 1$, operating at low D gives flexibility to operate with wide ranges of M. This enables the proposed topologies to give higher ac voltage gain compared to traditional ZSIs.

4.2.1 Proposed Topologies of Switched-Boost Modified ZSIs

The proposed three topologies of modified ZSIs are shown in Fig. 4.1. The proposed switched-boost ZSI, discontinuous input current qZSI (DC-qZSI) and continuous input current qZSI (CC-qZSI) are shown in Figs. 4.1(a), 4.1(b) and 4.1(c) respectively. In the proposed ZSIs, one of the capacitor is switched using a switch and a diode, without using additional passive components unlike the traditional voltage-fed ZSI and qZSI. For medium and high-power rating IGBT is obvious choice due to several advantage associated with it as compared to MOSFET such as low duty cycle, high voltage level, low frequency. The proposed topologies consists of two states; shoot-through state (DT_s) and non-shoot-through state $(1-D)\,T_s$.



(a)



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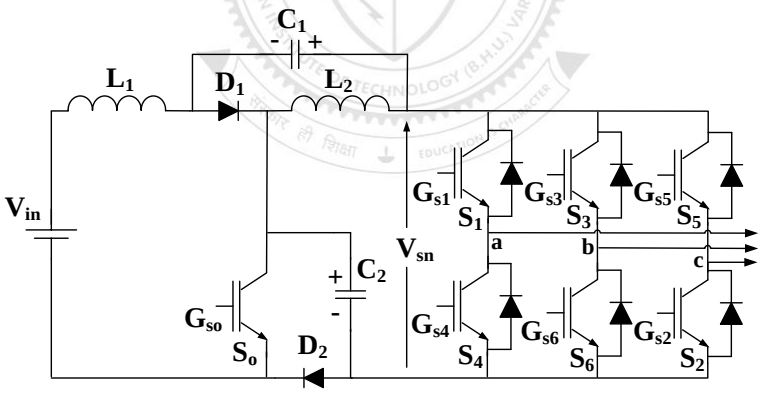


(c)

Fig. 4.1. Topologies of proposed modified ZSIs (a) switched-boost ZSI (SB-ZSI), (b) discontinuous input current qZSI (DC-qZSI), (c) continuous input current qZSI (CC-qZSI).

4.2.2 Operating Principle of SB- ZSI

The equivalent circuits for shoot-through and non-shoot-through states are presented in Figs. 4.2(a) and 4.2(b). The voltages across the inductors are V_{L1}, V_{L2} and the currents

through inductors are I_{L1} and I_{L2} respectively. The current through the capacitors are I_{c1}, I_{c2} and the voltage across the capacitors are V_{c1} and V_{c2} respectively. The switching voltage waveforms are shown in Fig. 4.2(c).

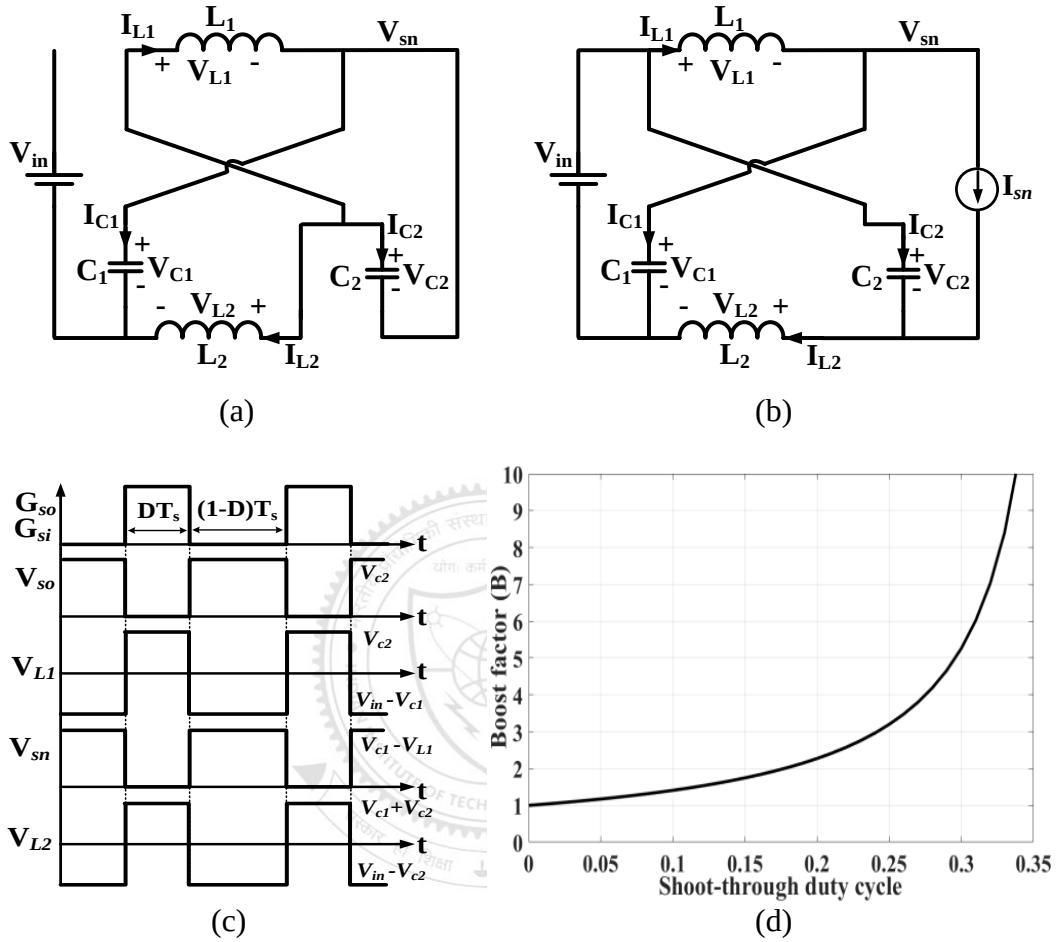


Fig. 4.2. Operating states waveform of proposed SB-ZSI (a) equivalent circuit in shoot-through interval, (b) equivalent circuit in non-shoot-through interval, (c) switch node voltages, (d) transfer characteristics.

1) Shoot-Through Interval

The diodes D_1 and D_2 are reverse biased and switch S_o conduct. In this interval, one of the inverter legs is also conducted. The input current is discontinuous as traditional ZSI. The voltage across the inductors and current through the capacitors in the shoot-through interval can be written as

$$L_1 \frac{di_{L1}}{dt} = V_{c2} \tag{4.1}$$

$$L_2 \frac{di_{L2}}{dt} = V_{c1} + V_{c2} \tag{4.2}$$

$$C_1 \frac{dV_{c1}}{dt} = -I_{L2} \tag{4.3}$$

$$C_2 \frac{dV_{c2}}{dt} = -I_{L1} - I_{L2} \tag{4.4}$$

2) Non-shoot-Through Interval

During the non-shoot-through behavior of proposed SB-ZSI switches, switch S_o is turned-OFF and inverter bridge is in power interval. In this case, both the diodes are in conduction mode. The voltage across the inductors and current through the capacitors in non-shoot-through interval are obtained as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{c1} \tag{4.5}$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} - V_{c2} \tag{4.6}$$

$$C_1 \frac{dV_{c1}}{dt} = I_{L1} - I_{sn} \tag{4.7}$$

$$C_2 \frac{dV_{c2}}{dt} = I_{L2} - I_{sn} \tag{4.8}$$

Under steady state condition, the average current through the capacitor and average voltage across the inductor over one switching cycle should be zero. By applying volt-seconds balance principle to the L_1 and L_2 over one switching period, (4.9) and (4.10) are obtained as

$$V_{c1} = \frac{(1-D)^2}{D^2-3D+1} V_{in} \tag{4.9}$$

$$V_{c2} = \frac{1-D}{D^2-3D+1} V_{in} \tag{4.10}$$

By applying charge-seconds balance principle to C_1 and C_2 over one switching period, (4.11) and (4.12) are obtained as

$$I_{L1} = \frac{1-D}{D^2-3D+1} I_{sn} \tag{4.11}$$

$$I_{L2} = \frac{D^2-3D+2}{D^2-3D+1} I_{sn} \tag{4.12}$$

From Figs. 4.2(a) and (b), the switched node voltage across the inverter bridge can be written as

$$V_{sn} = \frac{V_{in}}{D^2-3D+1} \tag{4.13}$$

The boost factor (*B*) is defined as

$$B = \frac{V_{sn}}{V_{in}} = \frac{1}{D^2-3D^2+1} \tag{4.14}$$

The transfer characteristic of proposed SB-ZSI is plotted in Fig. 4.2(d).

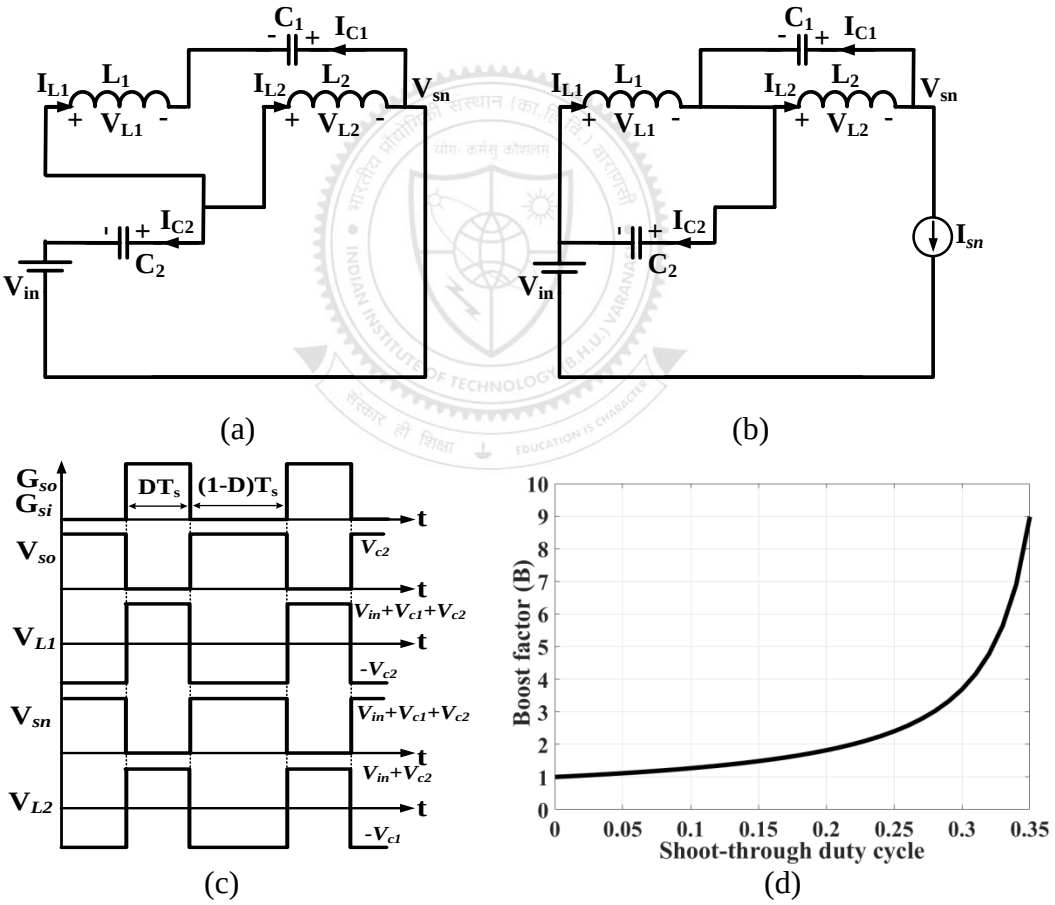


Fig. 4.3. Operating states waveform of DC-qZSI (a) equivalent circuit in shoot-through interval, (b) equivalent circuit in non-shoot-through interval, (c) switch node voltages, (d) transfer characteristics.

4.2.3 Operating Principle of DC- qZSI

The proposed DC-qZSI equivalent circuits of shoot-through interval and non-shoot-through interval are shown in Figs. 4.3(a) and 4.3(b). The voltages across the inductors are V_{L1}, V_{L2} and currents through inductors are I_{L1} and I_{L2}. The current through the capacitors are I_{c1}, I_{c2} and voltage across the capacitors are V_{c1} and V_{c2}. The switching voltage waveforms are shown in Fig. 4.3(c), and transfer characteristic of proposed DC-qZSI is plotted in Fig. 4.3(d).

1) Shoot-Through Interval

In this mode of operation, the diodes D_1 and D_2 are reverse biased, and one of the inverter legs is also conducted as shown in Fig. 4.3(a). The inductor voltages and capacitor currents are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} + V_{c1} + V_{c2} \tag{4.15}$$

$$L_2 \frac{di_{L2}}{dt} = V_{in} + V_{c2} \tag{4.16}$$

$$C_1 \frac{dV_{c1}}{dt} = -I_{L1} \tag{4.17}$$

$$C_2 \frac{dV_{c2}}{dt} = -I_{L1} - I_{L2} \tag{4.18}$$

2) Non-Shoot-Through Interval

The non-shoot-through behavior of the proposed DC-qZSI is shown as an equivalent circuit in Fig. 4.3(b). Applying KVL in the equivalent circuit of the non shoot-through interval, following is obtained:

$$L_1 \frac{di_{L1}}{dt} = - V_{c2} \tag{4.19}$$

$$L_2 \frac{di_{L2}}{dt} = -V_{c1} \tag{4.20}$$

$$C_1 \frac{dV_{c1}}{dt} = I_{L2} - I_{sn} \tag{4.21}$$

$$C_2 \frac{dV_{c2}}{dt} = I_{L1} - I_{sn} \tag{4.22}$$

Applying volt-seconds balance principle to L_1 and L_2 over one switching period, (4.23) and (4.24) are obtained as

$$V_{c1} = \frac{D(1-D)}{D^2-3D+1} V_{in} \tag{4.23}$$

$$V_{c2} = \frac{D}{D^2-3D+1} V_{in} \tag{4.24}$$

Applying charge-seconds balance principle to C_1 and C_2 over one switching period, (4.25) and (4.26) are obtained as

$$I_{L1} = \frac{1-D}{D^2-3D+1} I_{sn} \tag{4.25}$$

$$I_{L2} = \frac{(1-D)^2}{D^2-3D+1} I_{sn} \tag{4.26}$$

From Fig. 4.3(a) and 4.3(b), the switched node voltage across the inverter bridge can be written as

$$V_{sn} = V_{in} + V_{c1} + V_{c2} = \frac{(1-D)}{D^2-3D+1} V_{in} \tag{4.27}$$

The Boost factor (*B*) is defined as

$$B = \frac{V_{sn}}{V_{in}} = \frac{(1-D)}{D^2-3D+1} \tag{4.28}$$

4.2.4 Operating Principle of CC- qZSI

The proposed CC-qZSI topology equivalent circuits for shoot-through and non-shoot-through states are shown in Figs. 4.4(a) and (b) respectively. The voltages across the inductors are V_{L1}, V_{L2} and the currents through inductors are I_{L1} and I_{L2}. The current through the capacitors are I_{c1}, I_{c2} and the voltage across the capacitors are V_{c1} and V_{c2}. The switching voltage waveforms are shown in Fig. 4.4(c).

1) Shoot-Through Interval

In this mode of operation, the diodes D_1 and D_2 are reverse biased as shown in Fig. 4.4(a). The inductor currents I_{L1} and I_{L2} built-up-to maximum value through the capacitor C_1 and C_2. The inductor voltages and capacitor currents are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} + V_{c1} + V_{c2} \tag{4.29}$$

$$L_2 \frac{di_{L2}}{dt} = V_{c2} \tag{4.30}$$

$$C_1 \frac{dV_{c1}}{dt} = -I_{L1} \tag{4.31}$$

$$C_2 \frac{dV_{c2}}{dt} = -I_{L1} - I_{L2} \tag{4.32}$$

2) Non-Shoot-Through Interval

Equivalent circuit in the non-shoot-through interval is shown in Fig. 4.4(b). In this mode of operation, the switch S_o is reverse biased, and the inverter bridge operates in power mode. The inductor voltages and capacitor currents in non-shoot-through interval are given as follows:

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{c2} \tag{4.33}$$

$$L_2 \frac{di_{L2}}{dt} = -V_{c1} \tag{4.34}$$

$$C_1 \frac{dV_{c1}}{dt} = I_{L2} - I_{sn} \tag{4.35}$$

$$C_2 \frac{dV_{c2}}{dt} = I_{L1} - I_{sn} \tag{4.36}$$

Applying volt-seconds balance principle to the L_1 and L_2 over one switching period, (4.37) and (4.38) are obtained.

$$V_{c1} = \frac{D}{D^2 - 3D + 1} V_{in} \tag{4.37}$$

$$V_{c2} = \frac{1 - D}{D^2 - 3D + 1} V_{in} \tag{4.38}$$

Applying charge-seconds balance principle to the C_1 and C_2 over one switching period, (4.39) and (4.40) are obtained.

$$I_{L1} = \frac{1 - D}{D^2 - 3D + 1} I_{sn} \tag{4.39}$$

$$I_{L2} = \frac{(1-D)^2}{D^2-3D+1} I_{sn} \tag{4.40}$$

From Figs. 4.4(a) and (b), the switched node voltage across the inverter bridge can be written as

$$V_{sn} = V_{c1} + V_{c2} = \frac{V_{in}}{D^2-3D+1} \tag{4.41}$$

The Boost factor (*B*) is defined as

$$B = \frac{V_{sn}}{V_{in}} = \frac{1}{D^2-3D+1} \tag{4.42}$$

The transfer characteristics of proposed CC-qZSI is shown in Fig. 4.4(d). From this plot, it is clear that proposed inverter gives improved boost factor as compared to the traditional qZSI. Improve gain can also be achived in qZSI by using embedded switch inductor technique with the help of switch and diode as mentioned in appendix E.

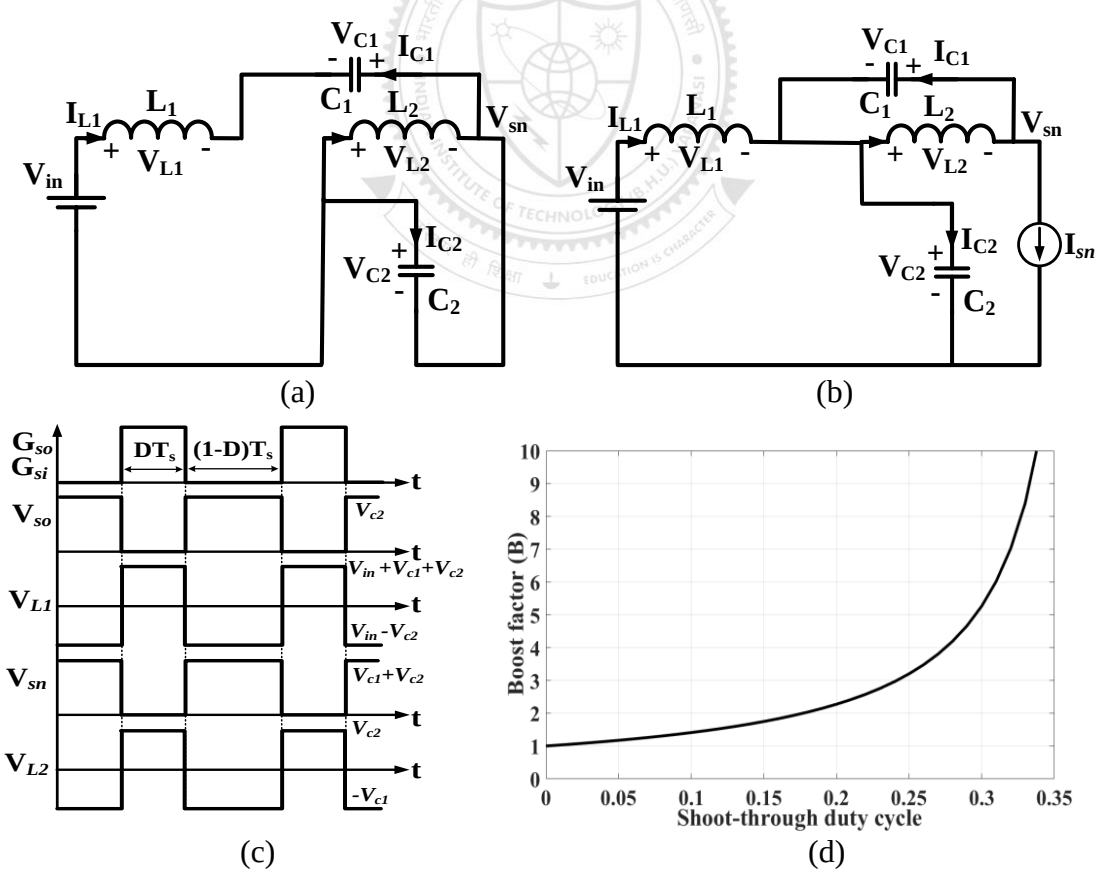


Fig. 4.4. Operating states waveform of proposed CC-qZSI (a) equivalent circuit in shoot-through interval, (b) equivalent circuit in non-shoot-through interval, (c) switch node voltages, (d) transfer characteristics.

4.3. Passive Components Design

In three-phase ZSI/qZSI, the capacitors and inductors are designed to limit the ripple voltage and switching frequency current ripple. Thus, for the proposed three-phase CC-qZSI, the inductors and capacitors are obtained as follows:

$$L_i = \frac{DV_{Li}}{\Delta i_{Li}\% \, I_{Li} \, f_s K_{sht}} \tag{4.43}$$

$$C_i = \frac{DI_{ci}}{\Delta V_{ci}\% \, V_{ci} \, f_s K_{sht}} \tag{4.44}$$

where i =1and 2. $V_{L1}$and V_{L2} are the voltages across the inductors L_1 and L_2, $I_{L1}$and I_{L2} are the currents flowing through L_1 and L_2, Δi_{L1} and Δi_{L2} represent percentage ripple currents in L_1 and L_2 during shoot-through interval D. $V_{c1}$and V_{c2} are the voltages across the capacitors C_1 and C_2, $I_{c1}$and I_{c2} are the currents flowing through C_1 and C_2. ΔV_{c1} and ΔV_{c2} represent percentage ripple voltages in C_1 and C_2 during D. f_s is the switching frequency and K_{sht} is a coefficient factor, which is equal to the number of shoot-through intervals in one switching cycle. The corresponding voltage and current expressions of capacitors and inductors are given as follows:

$$\left.\begin{aligned} V_{L1} &= \frac{D^2-3D+2}{D^2-3D+1} V_{in} \\ V_{L2} &= \frac{1-D}{D^2-3D+1} V_{in} \\ I_{L1} &= \frac{P_o}{V_{in}} \\ I_{L2} &= \frac{(1-D)P_o}{V_{in}} \\ V_{c1} &= \frac{D}{D^2-3D+1} V_{in} \\ V_{c2} &= \frac{1-D}{D^2-3D+1} V_{in} \\ I_{C1} &= \frac{P_o}{V_{in}} \\ I_{C2} &= \frac{(2-D)P_o}{V_{in}} \end{aligned}\right\} \tag{4.45}$$

where P_o is the output power. By substituting (4.45) in (4.42) and (4.43), the inductances and capacitances can be obtained as follows:

$$L_1 = \frac{D}{P_o f_s K_{sht} \Delta I_{L1}\%} \frac{D^2-3D+2}{D^2-3D+1} V_{in}^2 \quad (4.46)$$

$$L_2 = \frac{D}{P_o f_s K_{sht} \Delta I_{L2}\%} \frac{1}{D^2-3D+1} V_{in}^2 \quad (4.47)$$

$$C_1 = \frac{P_o}{f_s K_{sht} \Delta V_{c1}\%} \frac{D^2-3D+1}{V_{in}^2} \quad (4.48)$$

$$C_2 = \frac{P_o(2-D)D}{f_s K_{sht} \Delta V_{c2}\%} \frac{D^2-3D+1}{(1-D)V_{in}^2} \quad (4.49)$$

In order to operate the inverter in continuous conduction mode, the minimum inductor currents (I_{Li_min}) should be greater than 0. This is equal to the peak value of the phase current (I_{an}). Mathematically, it is written as,

$$I_{Li\_min} = I_{Li} - \frac{1}{2}\Delta i_{Li} \geq I_{an} \quad (4.50)$$

By putting the value of inductor currents I_{L1} and Δi_{Li} in (4.50), following is obtained

$$\left(\frac{3V_{an}I_{an}Cos\emptyset}{V_{in}} - \frac{V_{c1}D}{2L_1 I_{L1} K_{sth} f_s}\right) \geq I_{an} \quad (4.51)$$

After simplification of the (4.51), the critical inductances L_{1c} of the inductor L_1 is obtained as

$$L_{1c} \geq \frac{V_{c1}D\, V_{in} Z_{an}}{2V_{an} I_{L1} K_{sth} f_s (3V_{an} cos\emptyset - V_{in})} \quad (4.52)$$

where $Z_{an} = R_L + jX_L$, R_L is the resistive load per phase, X_L is inductive load per phase, and $cos\emptyset$ is power factor of the load. Similarly, for inductor L_2, the critical inductances L_{2c} is calculated as

$$L_{2c} \geq \frac{V_{c1}D\, V_{in} Z_{an}}{2V_{an} I_{L2} K_{sth} f_s (3(1-D)V_{an} cos\emptyset - V_{in})} \quad (4.53)$$

It is important to mention that for single-phase system, both high frequency and low frequency ripples (double line frequency) are present. However, in three-phase system, the double line frequency ripples do not exist. Therefore, in order to reduce peak-to-peak ripple, dominated by double line frequency ripples, higher values of passive components are required in single-phase case as compared to three-phase case [111]-

[112]. Thus, for the proposed three-phase inverter, lesser value of capacitors and inductors are required as compared to single-phase case.

TABLE 4.1
VOLTAGE STRESSES OF PROPOSED ZSIS

	Proposed SB-ZSI	Proposed DC-qZSI	Proposed CC-qZSI
C_1	$\frac{(1-D)^2}{D^2-3D+1}V_{in}$	$\frac{D(1-D)}{D^2-3D+1}V_{in}$	$\frac{D}{D^2-3D+1}V_{in}$
C_2	$\frac{(1-D)}{D^2-3D+1}V_{in}$	$\frac{D}{D^2-3D+1}V_{in}$	$\frac{(1-D)}{D^2-3D+1}V_{in}$
D_1	$-\frac{1}{D^2-3D+1}V_{in}$	$-\frac{(1-D)}{D^2-3D+1}V_{in}$	$-\frac{1}{D^2-3D+1}V_{in}$
D_2	$-\frac{(1-D)}{D^2-3D+1}V_{in}$	$-\frac{D}{D^2-3D+1}V_{in}$	$-\frac{(1-D)}{D^2-3D+1}V_{in}$
S_o	$\frac{(1-D)}{D^2-3D+1}V_{in}$	$\frac{D}{D^2-3D+1}V_{in}$	$\frac{(1-D)}{D^2-3D+1}V_{in}$
S_i	$\frac{1}{D^2-3D+1}V_{in}$	$\frac{(1-D)}{D^2-3D+1}V_{in}$	$\frac{1}{D^2-3D+1}V_{in}$

TABLE 4.2
CURRENT STRESSES OF PROPOSED ZSIS

	Proposed SB-ZSI	Proposed DC-qZSI	Proposed CC-qZSI
L_1	$\frac{1-D}{D^2-3D+1}I_{sn}$	$\frac{(1-D)}{D^2-3D+1}I_{sn}$	$\frac{(1-D)}{D^2-3D+1}I_{sn}$
L_2	$\frac{D^2-3D+2}{D^2-3D+1}I_{sn}$	$\frac{(1-D)^2}{D^2-3D+1}I_{sn}$	$\frac{D^2-2D+1}{D^2-3D+1}I_{sn}$
D_1	$\frac{1}{D^2-3D+1}I_{sn}$	$\frac{1}{D^2-3D+1}I_{sn}$	$\frac{1}{D^2-3D+1}I_{sn}$
D_2	$\frac{D^2-3D+2}{D^2-3D+1}I_{sn}$	$\frac{(1-D)}{D^2-3D+1}I_{sn}$	$\frac{(1-D)}{D^2-3D+1}I_{sn}$
S_o	$\frac{D^2-3D+2}{D^2-3D+1}I_{sn}$	$\frac{(1-D)}{D^2-3D+1}I_{sn}$	$\frac{(1-D)}{D^2-3D+1}I_{sn}$
S_i	$\frac{D^2-4D+3}{D^2-3D+1}I_{sn}$	$\frac{D^2-3D+2}{D^2-3D+1}I_{sn}$	$\frac{D^2-3D+2}{D^2-3D+1}I_{sn}$

4.4. Voltage and Current Stresses

The voltage and current stresses of the proposed ZSI topologies are given in Table 4.1 and Table 4.2 respectively. The proposed SB-ZSI and CC-qZSI has same boost factor, whereas the DC-qZSI has comparatively lower boost factor. The capacitor voltage stress of CC-qZSI has lower than SB-ZSI with continuous input current. The switch current stress of the SB-ZSI is higher than the DC-qZSI and CC-qZSI. Therefore, CC-qZSI is used in comparative analysis, simulation and experimentally verifications.

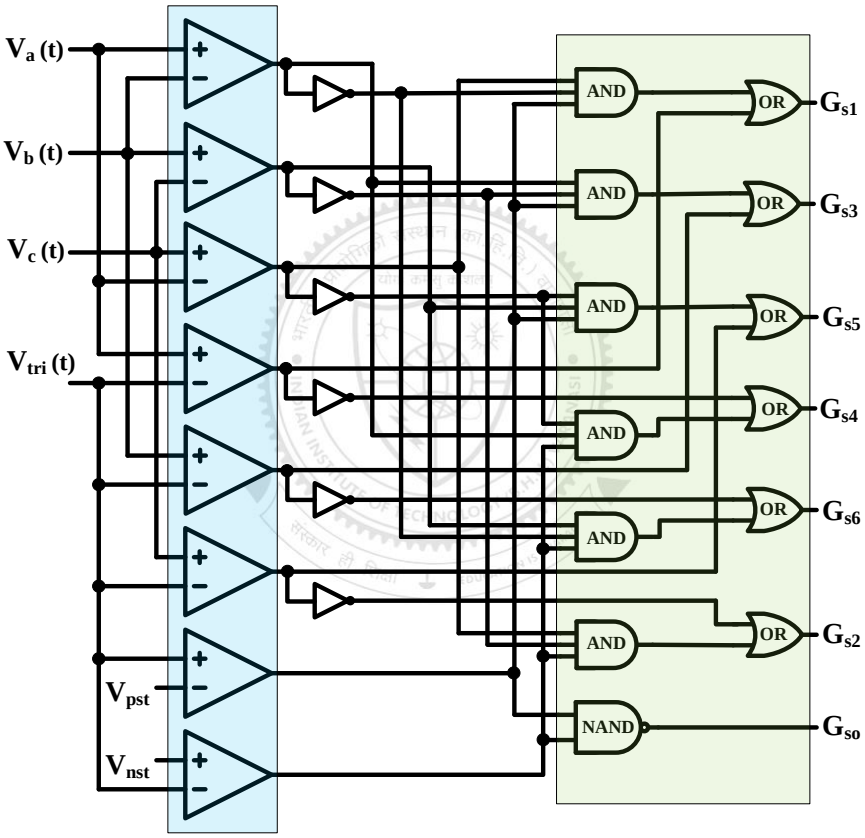
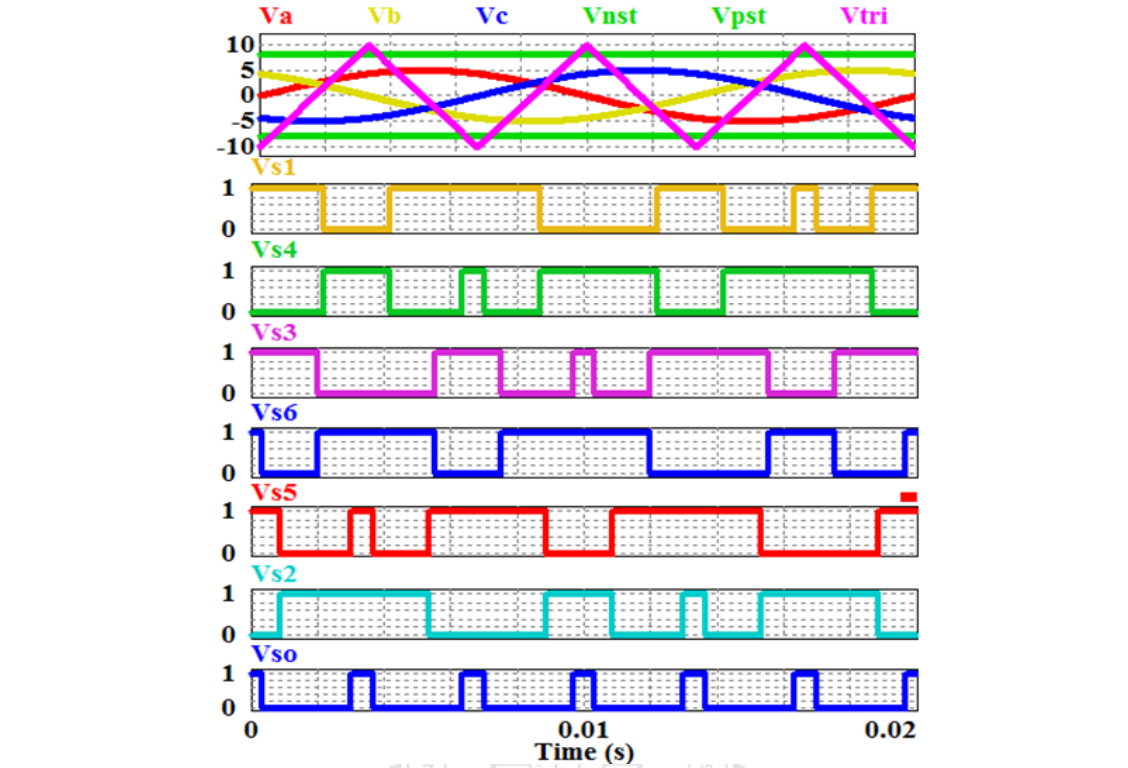


Fig. 4.5. Analog model of PWM generation.

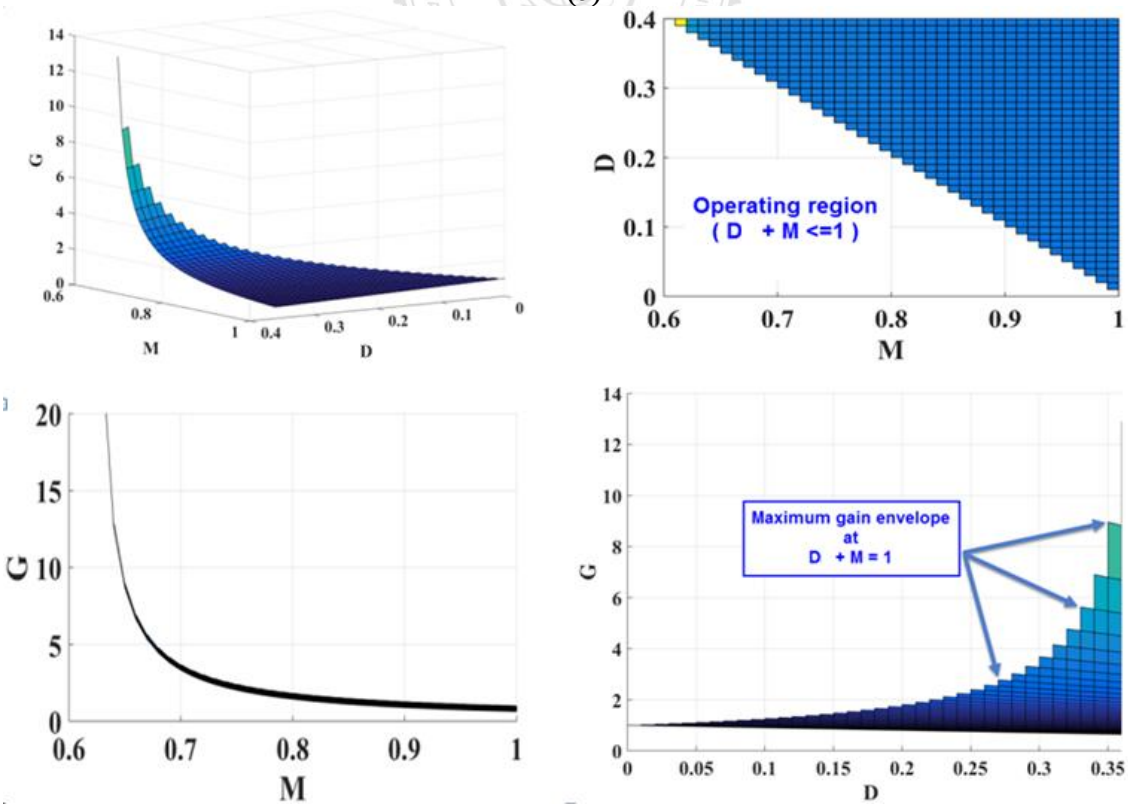
4.5. PWM Control Technique

To verify the operation of the proposed three-phase continuous input current qZSI (CC-qZSI), the PWM control technique discussed in [113]-[115] is used as shown in Fig. 4.5 and Fig. 4.6. Fig. 4.5 shows the analog representation of PWM generation. In Fig.

4.6(a), the high-frequency triangular waveform (V_{tri}) is compared with two shoot-through signals ($V_{pth}$and V_{nth}) and three reference sinusoidal signals ($V_a, V_b,$ and V_c).



(a)



(b)

Fig. 4.6. Behavior of modulation and duty cycle (a) PWM waveform for switches, (b) relation among *G*, *M* and *D*.

The two shoot-through signals are equal in magnitude but opposite in polarity. The constraint of shoot-through duty cycle (D) and modulation index (M) is given as

$$D + M \leq 1 \tag{4.54}$$

The peak ac gain factor (G) is given as

$$G = \frac{V_o}{V_{in}} = \frac{M}{D^2 - 3D + 1} \tag{4.55}$$

From the constraint (4.55), it is clear that the gain is depended upon the M and *D*. Fig. 4.6(b) shows a plot of *G* versus *D* and M. It may also be observed from Fig. 4.6 (b) that the maximum operating value of *D* and *M* is governed by $D + M \leq 1$.

The output phase voltage (rms) is given by

$$V_{an} = V_{bn} = V_{cn} = \frac{MBV_{in}}{2\sqrt{2}} \tag{4.56}$$

The output line voltage (rms) is given as

$$V_{ab} = V_{bc} = V_{ca} = \frac{MBV_{in}\sqrt{3}}{2\sqrt{2}} \tag{4.57}$$

4.6. Comparative Analysis of the Proposed ZSI with others ZSIs

In this section, the detailed comparative analysis is performed in terms of components count, voltage gain, cost function, power loss, efficiency, voltage stress, and current stress of the proposed CC-qZSI with other conventional ZSIs. As the proposed inverter is a transformer less continuous input current quasi Z source inverter (CC-qZSI). Therefore, to make fair comparison, only transformer less continuous input current profile based ZSIs are considered and ripple input current profile inverters as well as discontinuous input current based ZSIs are not taken in to account.

4.6.1 Components Count and Gain

Table 4.3 shows the comparison of components count and boost factor among the proposed inverter and the conventional ZSIs. From Table 4.3, it is clear that the numbers of diodes used in the literature [101]-[105], are comparatively higher than the proposed CC-qZSI. Higher number of inductors are used in the [101]-[102], and [104] as compared to the proposed CC-qZSI. However, [86] has less passive components but has low boost factor in comparison to the proposed CC-qZSI. Inverter discussed in [34] has lower boost factor compared to the proposed CC-qZSI and switched inverter reported in [103] has identical boost factor as that of the CC-qZSI but has two additional diodes.

TABLE 4.3
COMPARASION OF THE PROPOSED CC-QZSI WITH OTHERS ZSIS

Attributes	Proposed CC-qZSI	qZSI [34]	qSBI [86]	SL-qZSI [101]	cSL-qZSI [102]	SB-ZSI [103]	E-boost ZSI [104]	ASL/SL-qZSI [105]
Switch	7	6	7	6	6	7	6	7
Diode	2	1	2	4	7	4	3	5
Inductor	2	2	1	3	4	2	3	2
Capacitor	2	2	1	2	2	2	3	1
B	$\frac{1}{D^2-3D+1}$	$\frac{1}{1-2D}$	$\frac{1}{1-2D}$	$\frac{1+D}{1-2D-D^2}$	$\frac{1}{1-3D}$	$\frac{1}{1-3D+D^2}$	$\frac{1}{2D^2-3D+1}$	$\frac{1+D}{1-3D}$
G	$\frac{M}{M^2+M-1}$	$\frac{M}{2M-1}$	$\frac{M}{2M-1}$	$\frac{2M-M^2}{4M-M^2-2}$	$\frac{M}{3M-2}$	$\frac{M}{M^2+M-1}$	$\frac{1}{2M-1}$	$\frac{2M-M^2}{3M-2}$

4.6.2 Voltage and Current Stresses

The voltage and current expressions of the components are given in the Table 4.4. The voltage stress is defined as the ratio of voltage across the switch to G.V_{in} [101]. The total capacitor voltage, diode voltage, switch voltage, diode current, and switch current stresses are analyzed as shown in Fig. 4.7. Fig. 4.7(a) shows the comparative analysis of boost factor (B) with the variations in shoot-through duty cycle (*D*). From Fig.

4.7(a), it is clear that inverters reported in [102] and [105] have higher boost factor but [102] has two more inductors and five more diodes as compared to CC-qZSI. Inverter reported in [105] has three additional diodes as compared to CC-qZSI but saves one capacitor. It can be observed from Figs. 4.7(b) and (c) that the capacitors and diode voltage stresses, of the proposed CC-qZSI is less. However, total switch voltage stress of [86], [103], and [105] is higher than proposed CC-qZSI as shown in Fig. 4.7(d). From Fig. 4.7(e), it is clear that the proposed CC-qZSI has least total switch current stress as compared to other ZSIs. The total diode current stress of the proposed CC-qZSI is lesser as shown in Fig. 4.7(f) as compared to [101]-[103], [105].

4.6.3 Stored Energy Analysis and Reliability

In this section, the stored energy in passive elements is discussed for determining the size, weight, and cost estimation of the inverters [116]-[117]. The cost and volume of the system increase linearly with the stored energy. However, for switching elements cost function also depends upon the voltage and current stresses of the active elements. The expressions for the stored electrostatic and magnetic energies are calculated assuming that the passive components are ideal and same amount of ripple is considered for all the analysis.

The magnetic energy stored in the inductor and the stored energy in the capacitor is defined as E_{LW} and E_{CW} respectively.

The stored energy in the inductors $E_{LW} = \sum_{i=0}^{N} \frac{L_i I_{avi}^2}{2}$ (4.58)

The stored energy in the capacitors $E_{CW} = \sum_{i=0}^{N} \frac{C_i V_{ci}^2}{2}$ (4.59)

where N is number of inductors and I_{av} is the average inductor current.

TABLE 4.4
COMPARASION OF VOLATGE AND CURRENT EXPRESSIONS WITH OTHERS ZSIS

Attributes	Proposed CC-qZSI	qZSI [34]	qSBI [86]	SL-qZSI [101]	cSL-qZSI [102]	SB-ZSI [103]	E-boost ZSI [104]	ASL/SL-qZSI [105]
V_{c1}/V_{in}	D_sB	$\frac{(B+1)}{2}$	B	$\frac{2D_sB}{(1+D_s)}$	$\frac{(1-D_s)B}{(1+D_s)}$	B	D_sB	B
V_{c2}/V_{in}	$(1-D_s)B$	$\frac{(B+1)}{2}$	NA	$\frac{(1-D_s)B}{(1+D_s)}$	$\frac{2D_sB}{(1+D_s)}$	D_sB	D_sB	NA
V_{c3}/V_{in}	NA	NA	NA	NA	NA	NA	$(1-2D_s)B$	NA
I_{L1}/i_{sn}	$(1-D_s)B$	$\frac{(B+1)}{2}$	$\frac{(B+1)}{2}$	$(1-D_s)B$	$(1-D_s)B$	$(1-D_s)B$	$(1-D_s)^2B$	$\frac{(1-D_s)B}{(1+D_s)}$
I_{L2}/i_{sn}	$(1-D_s)^2B$	$\frac{(B+1)}{2}$	NA	$\frac{(1-D_s)B}{(1+D_s)}$	$(1-D_s)B$	$(1-D_s)^2B$	$(1-D_s)^2B$	$\frac{(1-D_s)B}{(1+D_s)}$
I_{L3}/i_{sn}	NA	NA	NA	$\frac{(1-D_s)B}{(1+D_s)}$	$(1-D_s)B$	NA	$(1-D_s)B$	NA
I_{L4}/i_{sn}	NA	NA	NA	NA	$(1-D_s)B$	NA	NA	NA
i_{D1}/i_{sn}	B	B	$\frac{(B+1)}{2}$	B	$(1+D_s)B$	$(1-D_s)B$	$(1-D_s)^2B$	$\frac{(1-D_s)B}{(1+D_s)}$
i_{D2}/i_{sn}	$(1-D_s)B$	NA	$\frac{(B-1)}{2}$	$\frac{(1-D_s)B}{(1+D_s)}$	$(1-D_s)B$	$D_s(2-D_s)B$	$(1-D_s)B$	$\frac{(1-D_s)B}{(1+D_s)}$
i_{D3}/i_{sn}	NA	NA	NA	$\frac{(1-D_s)B}{(1+D_s)}$	$(1-D_s)B$	$(1-D_s)B$	$(1-D_s)B$	$\frac{(1-D_s)B}{(1+D_s)}$
i_{D4}/i_{sn}	NA	NA	NA	$\frac{(1-D_s)B}{(1+D_s)}$	$(1-D_s)B$	$(1-D_s)B$	NA	$\frac{2D_sB}{(1+D_s)}$
i_{D5}/i_{sn}	NA	NA	NA	NA	$(1-D_s)B$	NA	NA	$\frac{(1-D_s)B}{(1+D_s)}$
i_{D6}/i_{sn}	NA	NA	NA	NA	$(1-D_s)B$	NA	NA	NA
i_{D7}/i_{sn}	NA	NA	NA	NA	$(1-D_s)B$	NA	NA	NA
v_{D1}/V_{in}	$-B$	$-B$	$-B$	$-B$	$-2B$	$-B$	$-B$	$-\frac{2D_sB}{(1+D_s)}$
v_{D2}/V_{in}	$-B(1-D_s)$	NA	$-B$	$-\frac{(1-D_s)B}{(1+D_s)}$	$-\frac{(1-D_s)B}{(1+D_s)}$	$-B$	$-(1-2D_s)B$	$-\frac{2D_sB}{(1+D_s)}$
v_{D3}/V_{in}	NA	NA	NA	$-\frac{D_sB}{(1+D_s)}$	$-B(1-D_s)$	$-B(1-D_s)$	$-D_sB$	$-\frac{2(1-D_s)B}{(1+D_s)}$
v_{D4}/V_{in}	NA	NA	NA	$-\frac{D_sB}{(1+D_s)}$	$-\frac{D_s(1+2D_s^2)B}{(1+D_s)}$	$-BD_s$	NA	$-B$
v_{D5}/V_{in}	NA	NA	NA	NA	$-\frac{2D_sB}{(1+D_s)}$	NA	NA	$-B$
v_{D6}/V_{in}	NA	NA	NA	NA	$-B(1-D_s)$	NA	NA	NA
v_{D7}/V_{in}	NA	NA	NA	NA	$-\frac{2D_sB}{(1+D_s)}$	NA	NA	NA
v_{so}/V_{in}	$(1-D_s)B$	NA	B	NA	NA	B	NA	B
i_{so}	I_{L1}	NA	I_{L1}	NA	NA	I_{L1}	NA	$2I_{L1}$
i_{sn}	$I_{L1}+I_{L2}$	$2I_{L1}$	I_{L1}	$I_{L1}+I_{L2}+I_{L3}$	$2I_{L1}+2I_{L3}$	$I_{L1}+I_{L2}$	$I_{L1}+I_{L2}+I_{L3}$	$2I_{L1}$

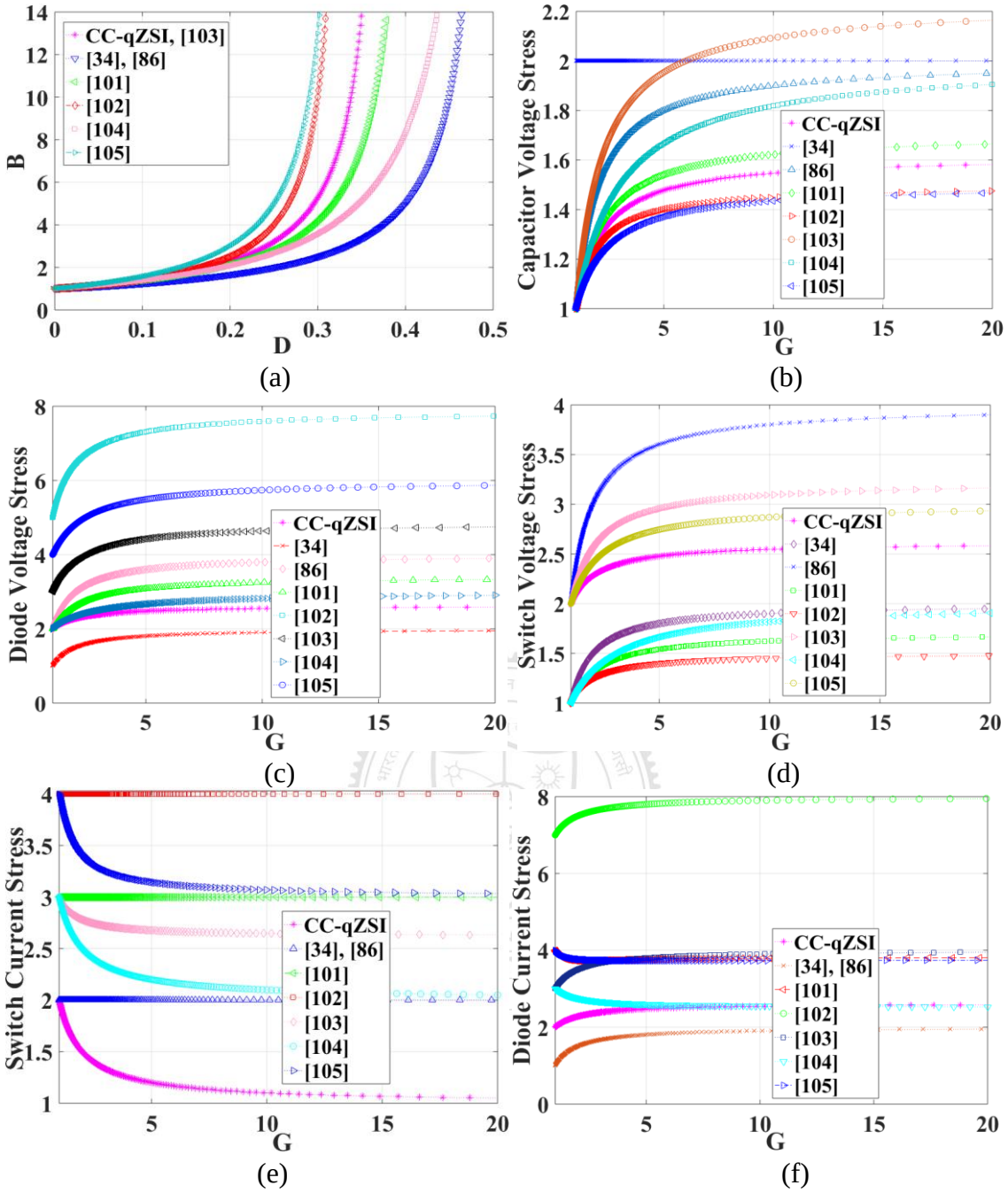


Fig. 4.7. Comparative analysis (a) boost factor variation with *D*, (b) capacitor voltage stress, (c) diode voltage stress, (d) switch voltage stress, (e) switch current stress, (f) diode current stress.

The stored energies in the conventional qZSI are calculated using:

$$E_{LW} = \frac{P_o D(1-D)}{f_s K_{sht} \Delta I_L \% \, (1-2D)} \tag{4.60}$$

$$E_{CW} = \frac{P_o D}{2 f_s K_{sht} \Delta V_c \% \, (1-2D)} \tag{4.61}$$

where P_o is the output power , f_s is switching frequency , K_{sht} is the number of shoot-through in one triangular cycle, D is the shoot-through duty cycle, I_L is the average inductor current, V_c is capacitor voltage, and $D = (B-1)/2B$.

Similarly, using values of passive components expressed in (4.46) - (4.49), the stored energies in the proposed CC-qZSI can be obtained using:

$$E_{LW} = \frac{P_o D(2D^2-5D+3)}{2f_s K_{sht} \Delta I_L\% \, (D^2-3D+1)} \tag{4.62}$$

$$E_{CW} = \frac{P_o D(D^2-4D+2)}{2f_s K_{sht} \Delta V_c\% \, (D^2-3D+1)} \tag{4.63}$$

where $= 1.5 - \sqrt{\frac{5B+4}{4B}}$. The total stored energy ($E_{LW} + E_{CW}$) of the proposed inverter is compared with the conventional qZSI as shown in Fig. 4.8. It can be observed from Fig. 4.8 that the proposed inverter requires lesser stored energy when B >1.8 for 0.5 kW power output. However, for 1 kW output power, the conventional qZSI is suited for $B <$ 1.75. It is also clear from Fig. 4.8 that the proposed inverter require lesser stored energy when operating at B =1.75 for 1kW power rating. In this way, it can be concluded that for higher power rating, the proposed inverter is suitable as it significantly saves size, weight, and cost of the passive elements.

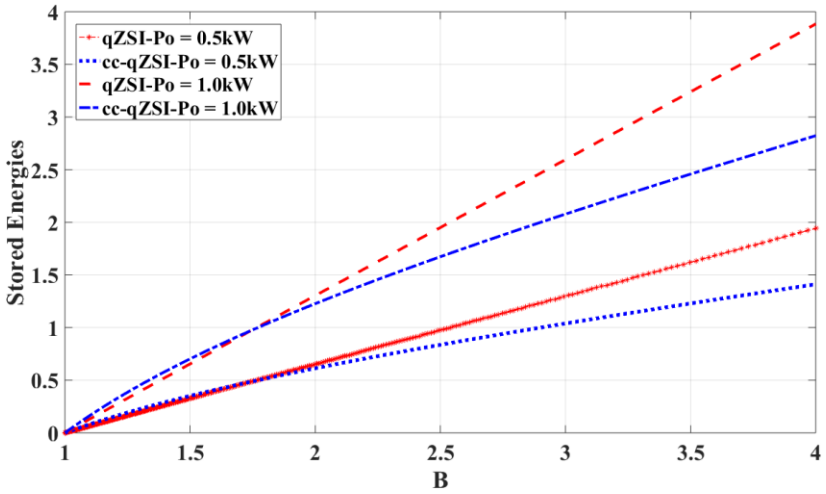


Fig. 4.8. Comparative analysis of stored energy.

The cost function depends both on passive elements as well as active elements. The passive components are analyzed by the stored energy analysis. However, for active elements cost function depends upon the voltage and current stresses of these elements. So, for cost analysis of active elements, the switch device power (SDP) analysis is carried out. The SDP of switching elements is expressed as the product of voltage and current stresses. The total SDP of an inverter is defined as the aggregate of SDP of all the switching devices used in the circuit [118]. The total SDP is a measure of the total switching devices. Thus, SDP is an important cost indicator of active elements used in the inverter. The SDP analyses of the active elements are given below.

$$\text{Total Average SDP} = (SDP)_{av} = \sum_1^n V_n I_{n\_av} \tag{4.64}$$

and

$$\text{Total Peak SDP} = (SDP)_{pk} = \sum_1^n V_n I_{n\_pk} \tag{4.65}$$

where n is the number of devices (switches and diodes), I_{n_av} and I_{n_pk} are the average and peak current flowing through the device, respectively, and V_n is the peak voltage across the devices. Thus, for conventional qZSI, the SDPs are calculated as follows:

$$(SDP)_{av} = \frac{1+2D}{1-2D} P_o + \frac{8}{Cos\emptyset\pi} P_o \tag{4.66}$$

$$(SDP)_{pk} = \frac{1}{(1-D)(1-2D)} P_o + \max\left\{\left(\frac{8}{MCos\emptyset} P_o\right), \left(\frac{4}{MCos\emptyset} P_o + \frac{4}{1-2D} P_o\right)\right\} \tag{4.67}$$

For the proposed CC-qZSI, the SDPs are obtained as follows:

$$(SDP)_{av} = \frac{2-4D^2+2D^3}{1-3D+D^2} P_o + \frac{8}{Cos\emptyset\pi} P_o \tag{4.68}$$

$$(SDP)_{pk} = \frac{2-2D+D^3}{(1-D)(1-3D+D^2)} P_o + \max\left\{\left(\frac{8}{MCos\emptyset} P_o\right), \left(\frac{4}{MCos\emptyset} P_o + \frac{4-2D}{1-3D+D^2} P_o\right)\right\} \tag{4.69}$$

The analysis of the $\frac{(SDP)}{P_o}$ ratio of both peak as well as average value with respect to the boost factor (B) is shown in Fig. 4.9. It is clear from Fig. 4.9 that the SDP requirement is reduced when power factor increases linearly. From the analysis it is clear that the proposed CC-qZSI has less peak SDP to P_o ratio as compared to conventional qZSI when operating at $B \geq 2$. Further, for operating around $B = 4$, the proposed CC-qZSI requires less average SDP to P_o ratio as compared to conventional qZSI. So, the proposed CC-qZSI is beneficial when operating at the boost factor (B) higher than 2 as compared to the conventional qZSI.

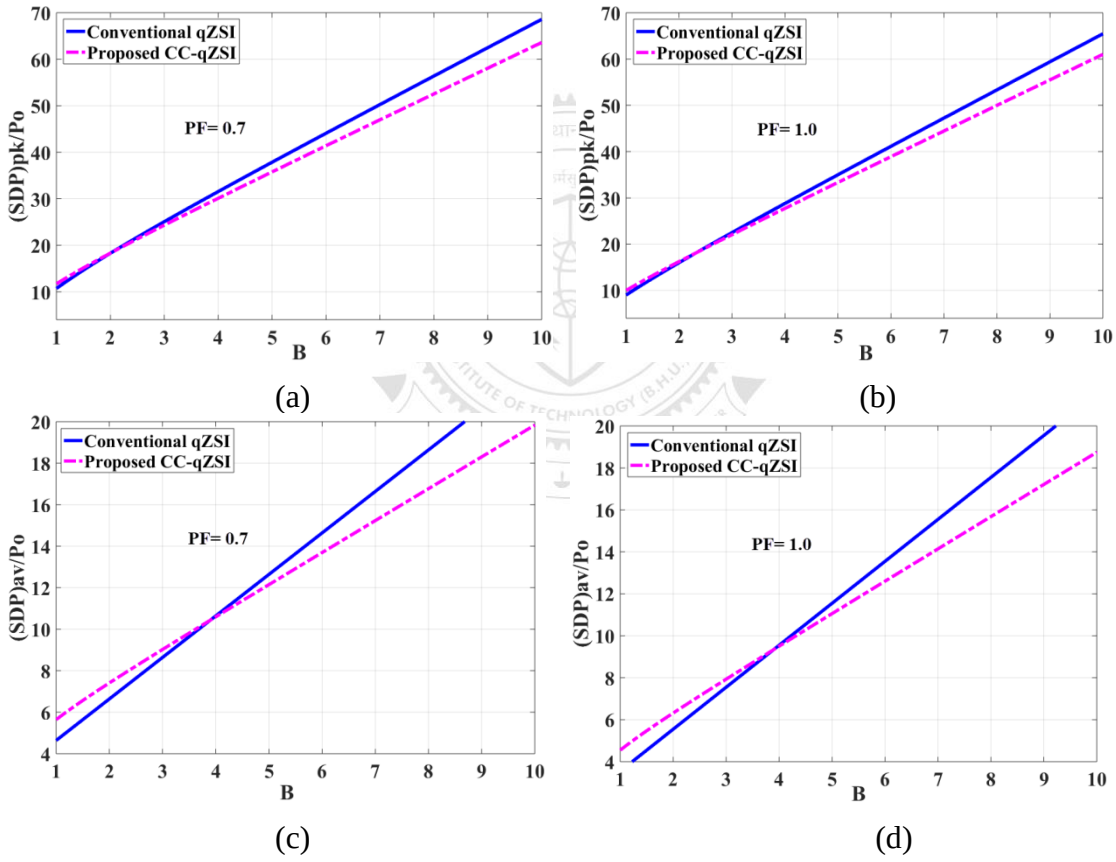


Fig. 4.9. Switch device power (SDP) comparative analysis (a) peak SDP variation at pf = 0.7, (b) peak SDP variation at pf = 1.0, (c) average SDP variation at pf = 0.7, (d) average SDP variation at pf = 1.0.

The shoot-through problem caused due to misgating because of EMI noises is the one of the major threats to the reliability of the classical voltage source inverters. As

the proposed ZSIs has inherent shoot through ability, misgating problem is addressed in it similar to the classical ZSI. The reliability of the inverter depends on many factors, such as voltage stress, power rating, and temperature [119]. As, the proposed inverter has lesser voltage and current stresses, lesser stored energy in passive components, its reliability increases.

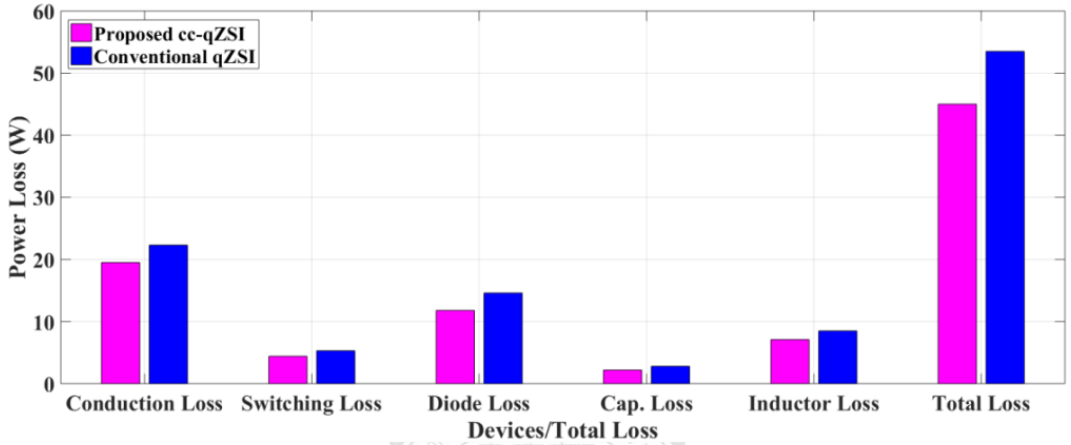
4.6.4 Power Loss and Efficiency Analysis

For the power loss analysis the parameters are defined as 1) on-state resistance of active switch is r_s and forward voltage drop is V_{FS}, 2) series resistance of the diode is r_D and forward voltage drop is V_{FD}, and 3) the resistances of inductors and capacitors are represented by r_L and r_C, respectively. In this thesis, the power loss calculation method discussed in [120], [121] is used for components power loss calculations. The power loss of proposed CC-qZSI and conventional qZSI are calculated for the parameters given in Table 4.5 for V_{in}= 65 V and boost factor B = 5.26. It is clear from Fig. 4.10 that conduction losses are maximum and capacitor losses are minimum. The conduction and switching losses are lesser in the proposed cc-qZSI as compared to conventional qZSI. It is clear from Fig. 4.10 (a) that the total power loss of the conventional qZSI is 53.5W and the total power loss of the proposed inverter is 45 W.

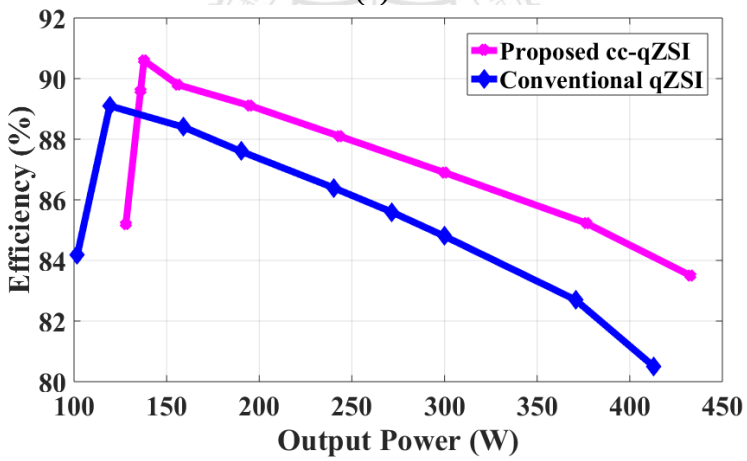
TABLE 4.5
COMPONENTS PARAMETERS FOR POWER LOSS CALCULATIONS

Components	**Specification**
Switches (FGH75T65SQD)	V_{FS} = 1.1V , r_S = 138mΩ
Diodes (40EPF06)	V_{FD} = 0.85V , r_D = 112mΩ
ESR of C_1 and C_2	r_{C1} = 125mΩ, r_{C2} = 61mΩ,
Parasitic resistance of L_1 and L_2	r_{L1} =150mΩ, r_{L2} = 155mΩ
Boost Factor(B)	5.26
Power rating	500W

Fig. 4.10(b) shows the calculated efficiency at different operating output power loads for 65 V input. From Fig. 4.10(b), it is clear that the proposed inverter has maximum efficiency of 90.6 %, whereas the conventional qZSI has maximum efficiency of 89.1%. This shows that the proposed inverter has higher efficiency than the conventional qZSI.



(a)



(b)

Fig. 4.10. Power loss and efficiency analysis (a) power loss distributions, (b) efficiency.

4.7. Extension of Proposed ZSI for Enhance Boost Capability

The boost capability of the proposed CC-qZSI is further extendable (n-stage) as shown in Fig. 4.11. By extending the proposed CC-qZSI to n- number of stages, the boost capability can further be increased. It can be observed from Fig. 4.11 that two capacitors (C_1 and C_2), diode (D_1), and inductor (L_2) form one cell and n- number of

such cells can be connected in cascade and thus, even higher boost factor can be achieved. The operation of the extended CC-qZSI is similar to the basic CC-qZSI, which is discussed in section 4.1.1. In the shoot-through interval all the diodes are in non-conduction modes. All the diodes conduct in non-shoot-though mode. A brief discussion about the n-stage CC-qZSI is as follows:

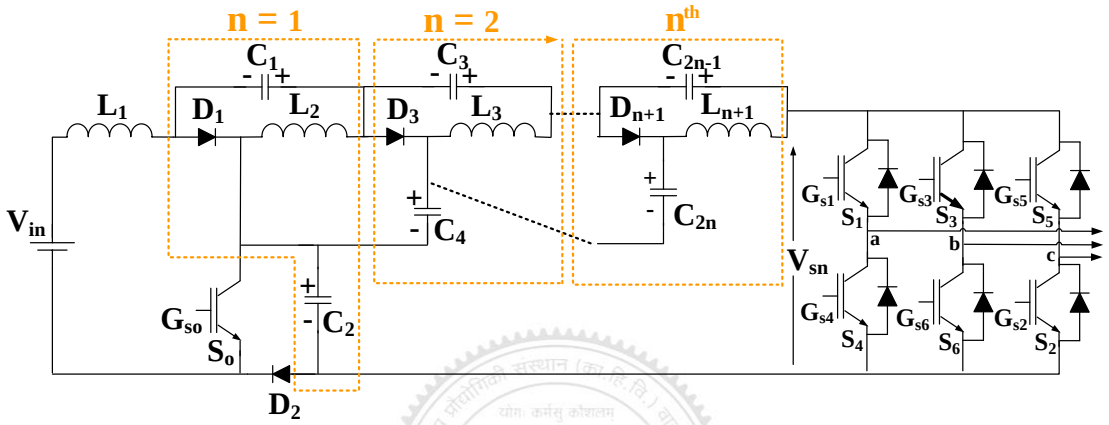


Fig. 4.11. Proposed extended CC-qZSI.

The capacitor voltages are obtained by applying volt-seconds balance principle to the L_1 , L_2 ,…… L_{n+1} over one switching period.

$$V_{c1} = V_{c3} = V_{c(2n-1)} = \frac{DV_{in}}{nD^2-(n+2)D+1} \tag{4.70}$$

$$V_{c4} = V_{c6} = V_{c(2n)} = \frac{DV_{in}}{nD^2-(n+2)D+1} \tag{4.71}$$

$$V_{c2} = \frac{(1-nD)V_{in}}{nD^2-(n+2)D+1} \tag{4.72}$$

$$V_{sn} = V_{c2} + \{V_{c1} + V_{c3} + \cdots . + V_{c(2n-1)}\} \tag{4.73}$$

V_{sn} depends upon the extended capacitor voltages as shown in Fig. 4.11. Voltage $V_{c1} = V_{c3}$ and $V_{c4} = V_{c6}$ as is clear from (4.70) and (4.71). The boost factor (B) for n-stage CC-qZSI can be written as follows.

$$B = \frac{V_{sn}}{V_{in}} = \frac{1}{nD^2-(n+2)D+1} \tag{4.74}$$

For two extensions (n = 2) Boost factor (B) is given as

$$\text{Boost factor (B)} = \frac{1}{2D^2-4D+1} \tag{4.75}$$

From (4.75) it is clear that the extendable CC-qZSI is capable of giving even higher boost factor as shown in Fig. 4.12. The detailed discussion of two stage extended diode assisted and capacitor assisted are found in Appendix F.

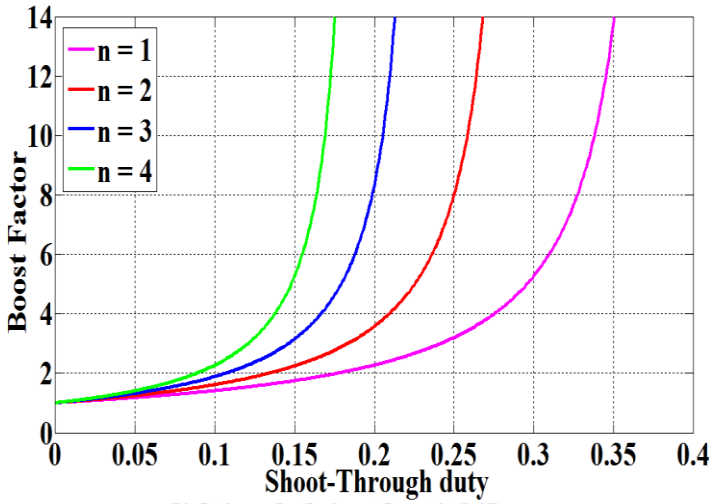


Fig. 4.12. Transfer characteristic of extended CC-qZSI for different stage.

4.8. Simulation of Switched-Boost Modified ZSIs Topologies

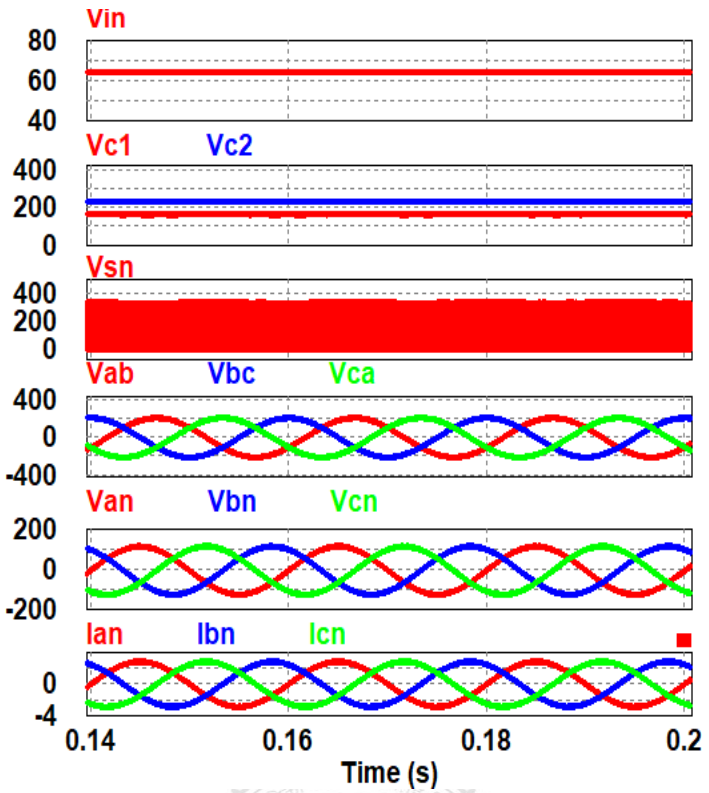
In all the proposed ZSIs, the proposed SB-ZSI, DC-qZSI are discontinuous input current profile based inverter. The boost factor of SB-ZSI and CC-qZSI are same but DC-qZSI has lesser boost factor as compared to CC-qZSI and SB-ZSI but have higher have conventional ZSI. The simulation verification is done using PSIM 11.0. The simulation verifications of all the proposed ZSIs are given in the subsequent subsections.

4.8.1 Simulation of SB-ZSI

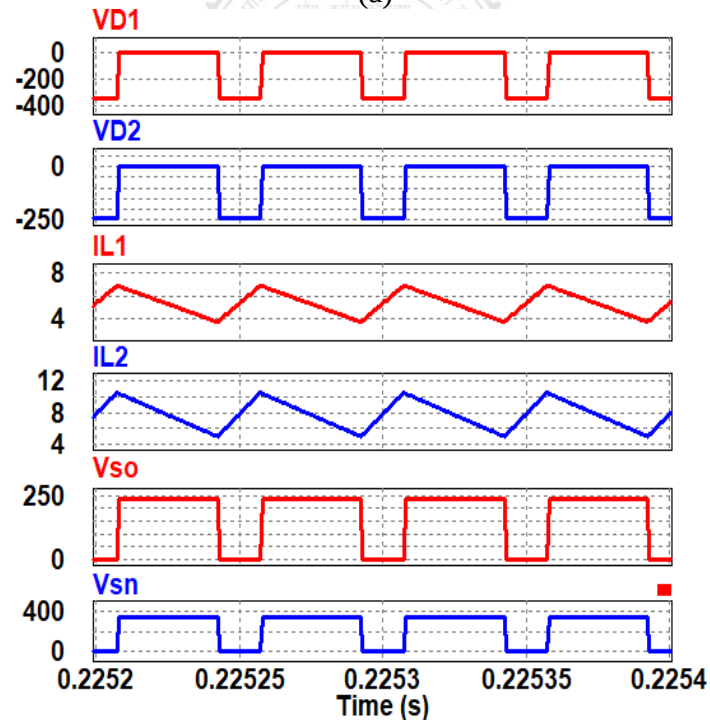
The operation of the proposed modified SB-ZSI is verified for 500 W with D = 0.3 and M= 0.7. The capacitors (C_1, C_2) values are 470 μF and 690 μF; inductor values are L_1 = 0.81 mH, L_2 = 0.85 mH; and per phase resistive load is 43 Ω. The ac filter inductors and capacitors per phase values are 1 mH and 10 µF, respectively. The proposed CC-qZSI gives V_{c1} =167 V, V_{c2} = 240 V; line output voltage ($V_{ab} = V_{bc} = V_{ca}$) = 415V (pk-pk); phase output voltage ($V_{an} = V_{bn} = V_{cn}$) = 244V (pk-pk); and phase output current ($I_{an} = I_{bn} = I_{cn}$) = 5.46A (pk-pk) for input voltage V_{in}=65 V as shown in Fig. 4.13(a). The simulation analysis shows that the boost factor (B) = 5.26 and peak ac gain (G) = 3.68. From the Fig. 4.13(b) it is clear that the peak diode voltages are V_{D1} = -342 V, V_{D2} = -240 V. The average inductor currents, I_{L1} = 5.4A, I_{L2} = 7.8A and maximum switch voltage is calculated as V_{so} = 240 V.

4.8.2 Simulation of DC-qZSI

The operation of proposed DC-qZSI is also verified for D = 0.3 and M= 0.7. The per phase resistive load is 43 Ω, and have taken the same parameters as used in SB-ZSI. The simulation verification of DC-qZSI are given in the Fig. 4.14. From the Fig. 4.14(a) it is clear that the input voltage is 65V, and capacitors voltages are as V_{c1} =71.8 V, V_{c2} = 102 V. The line output voltage ($V_{ab} = V_{bc} = V_{ca}$) is obtained as 290V (pk-pk), phase output voltage ($V_{an} = V_{bn} = V_{cn}$) is obtained as 167V (pk-pk) and phase output current ($I_{an} = I_{bn} = I_{cn}$) is obtained as 4.2A (pk-pk). From the simulation verification, the boost factor (B) and peak ac gain (G) is calculated as 3.7 and 2.6 respectivelly for the D = 0.3 and M= 0.7. The diode voltage stresses, inductor currents, and switch voltage stresses are shown in Fig. 4.14(b).

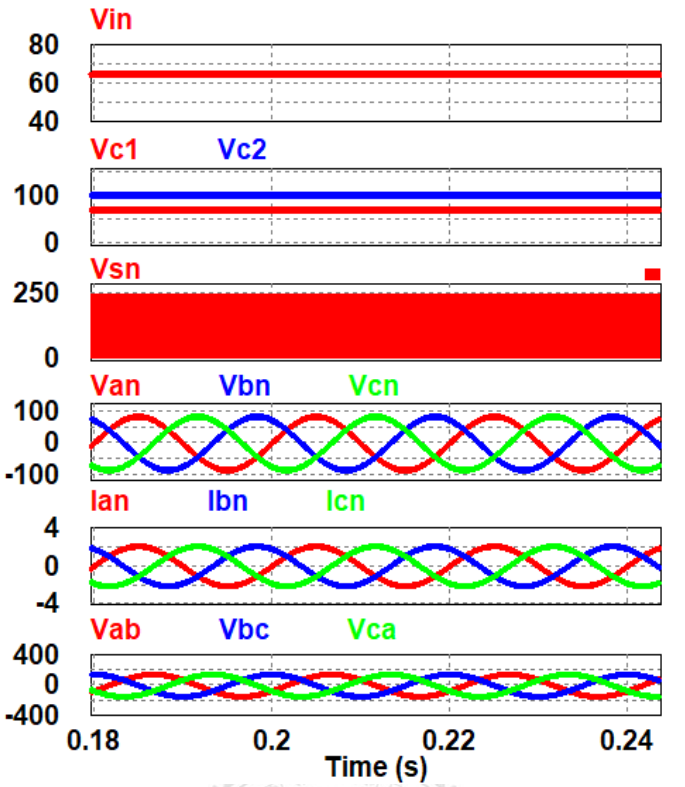


(a)

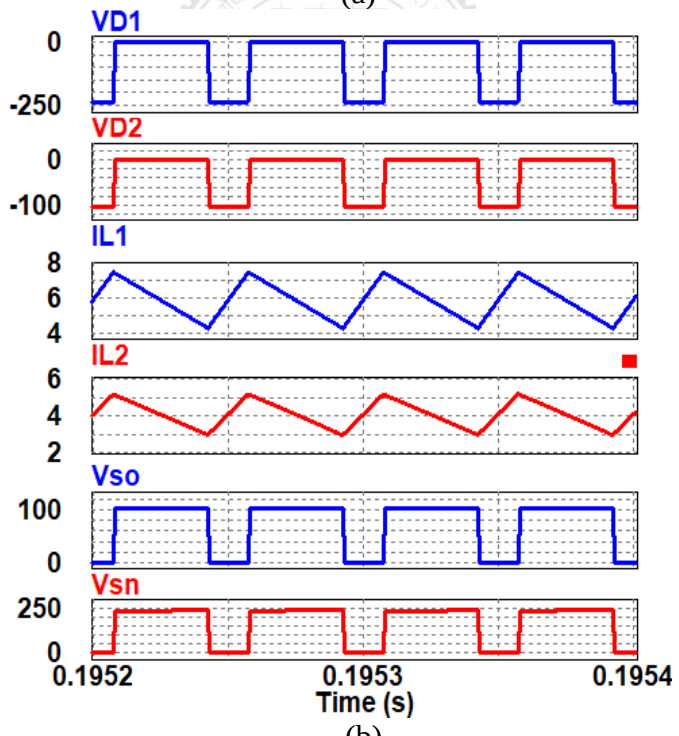


(b)

Fig. 4.13. Simulation results of the proposed SB-ZSI (a) steady state capacitor voltages, output line voltages, output phase voltages, and currents, (b) voltage across the diodes, switches, and inductors current.

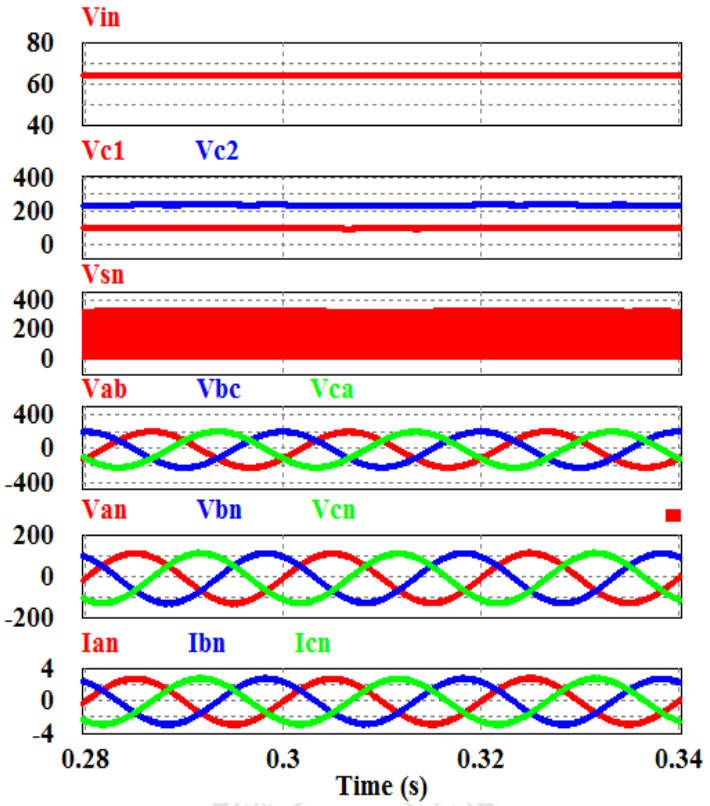


(a)

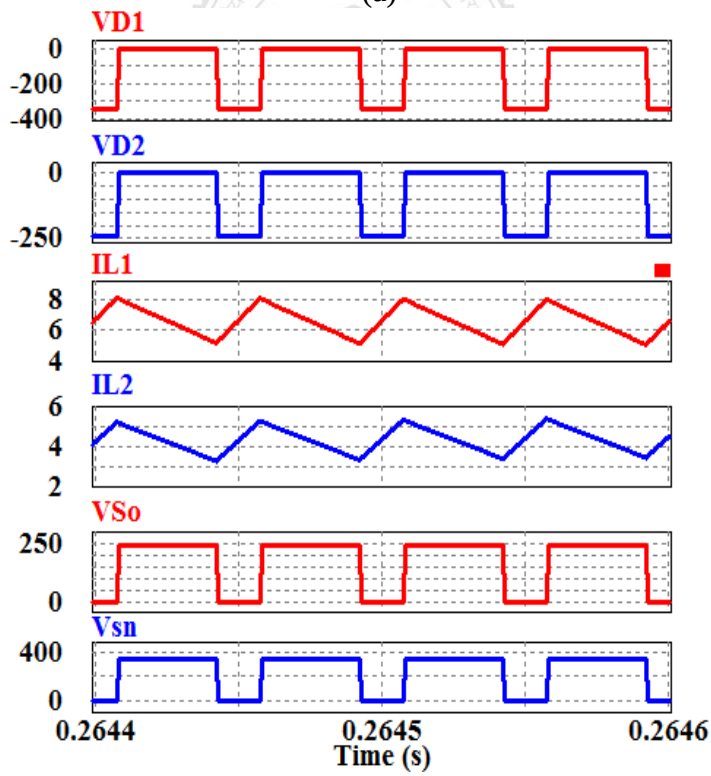


(b)

Fig. 4.14. Simulation results of the proposed DC-qZSI (a) steady state capacitor voltages, output line voltages, output phase voltages, and currents, (b) voltage across the diodes, switches, and inductors current.



(a)



(b)

Fig. 4.15. Simulation results of the proposed CC-qZSI (a) steady state capacitor voltages, output line voltages, output phase voltages, and currents, (b) voltage across the diodes, switches, and inductors current.

4.8.3 Simulation of CC-qZSI

The proposed CC-qZSI is designed for 500W prototype and operated at D = 0.3 and M= 0.7. The ac filter inductors and capacitors per phase values are 1 mH and 10 µF, respectively. The capacitors (C_1, C_2) values are 470 μF and 690 μF; inductor values are L_1 = 0.81 mH, L_2 = 0.85 mH; and per phase resistive load is 43 Ω. The simulated waveforms are given in Fig. 4.15. The proposed CC-qZSI gives V_{c1} =102.8 V, V_{c2} = 239.5 V; line output voltage ($V_{ab} = V_{bc} = V_{ca}$) = 416V (pk-pk); phase output voltage ($V_{an} = V_{bn} = V_{cn}$) = 244V (pk-pk); and phase output current ($I_{an} = I_{bn} = I_{cn}$) = 5.5A (pk-pk) for input voltage V_{in}=65 V as shown in Fig. 4.15(a). The values of the boost factor (B) = 5.26 and peak ac gain (G) = 3.68. The diode voltage stresses, inductor currents, and switch voltage stresses are shown in Fig. 4.15(b).

4.9. Comparative Analysis Proposed Converters

In this thesis, three converters are proposed for microgrid applications. The first converter is derived from the quadratic boost converter which gives high voltage gain in small duty cycle. The proposed high gain inverter does not have right half plane zero which makes the system minimum phase. Thus, due to no RHPZ, the controller design is simpler. Also, presence of RHPZ in the control-to-output transfer function also poses problem of lower bandwidth of the system and gives difficulty in achieving adequate phase margin. This proposed minimum phase inverter also capable of simultaneous dc and ac outputs. The drawback of this inverter is that it has passive damping components which reduce the efficiency in the lieu of no RHPZ. Moreover, for different load requirement the proposed minimum phase inverter is not suited.

TABLE 4.6
COMPARATIVE ANALYSIS OF PROPOSED CONVERTERS

Proposed Converters	Boost factor	Multi-Output	RHPZ	Efficiency	Key Advantage	Comments
High Gain Minimum Phase Inverter	$\frac{1}{(1-D)^2}$	Yes	Yes	Lower	High gain with no-RHPZ	✓ No RHPZ ✓ High Gain. ✓ Simultaneous single ac and single dc output.
Multi-output Parallel Mode	$\frac{1}{(1-D)^2}$	Yes	No	Moderate	n number of ac with single dc output.	✓ Multi ac output and single dc. ✓ No. of passive components save. ✓ Suitable for constant voltage and variable current loads. ✓ Suitable for constant current and variable voltage loads.
Multi-output Series Mode	$\frac{1}{n(1-D)^2}$					
SB-ZSI	$\frac{1}{D^2-3D^2+1}$	No	No	Higher	Improve ZSI topol-ogies with less loss and less cost.	✓ Suitable for high power and when required B ≥ 2 as compared to conventional ZSI. ✓ Low cost. ✓ High efficiency. ✓ Improve ZSI topologies. ✓ Extendable for further high gain.
DC-qZSI	$\frac{(1-D)}{D^2-3D^2+1}$					
CC-qZSI	$\frac{1}{D^2-3D^2+1}$					

The proposed multi-output quadratic converters are also derived from quadratic boost converter. These converters eliminate the drawback of the minimum phase inverter and have improved efficiency, multiple ac outputs and compact size. The proposed multi-output series mode topologies give n-number of ac outputs with variable voltages and same currents along with one dc output. Also, the multi-output parallel mode topologies give n-number of ac outputs with same voltages and variable currents along with one dc output.

The drawbacks of the proposed multi-output converters are that they are not suited for higher power rating and have slightly lower efficiency. Moreover, the converters operate at relatively higher duty ratio to achieve high voltage gain. The drawbacks of these converters are eliminated by the proposed ZSIs. The proposed ZSIs are capable of giving higher gain with low shoot-through duty cycle. The proposed ZSIs have low cost and higher efficiency as compared to the conventional ZSI.

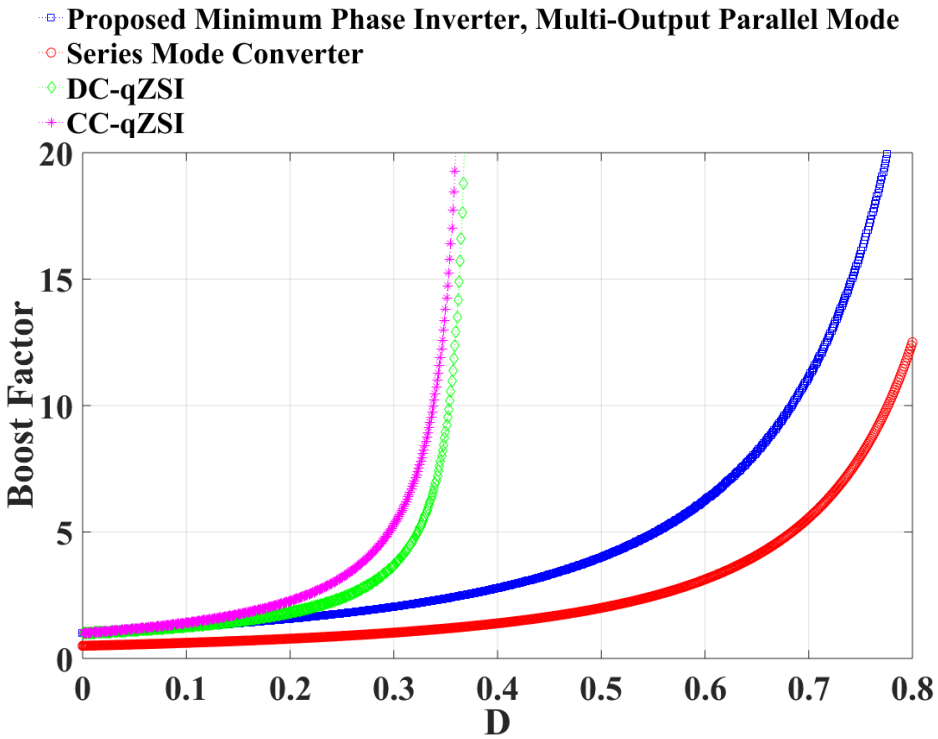


Fig. 4.16. Comparative analysis of boost factor

The proposed converters comparative analyses are given in the Table 4.6. From the Table 4.6, it is clear that proposed ZSI has highest boost factor as compared to other proposed converters as shown in Fig. 4.16. The proposed high gain minimum phase inverter and multi-output quadratic converters are both hybrid type and have capability to simultaneous ac and dc output. However, proposed ZSI is only having single-input single-output based converters topologies similar to conventional ZSI. The proposed

minimum phased inverter have no RHPZ in the control-to-output transfer function, but this feature is absent in proposed multi-output converter and proposed ZSIs. For different load requirements single multi-output converter is most suited. The use of damping network in the minimum phase converter reduces the converter efficiency. The efficiency of the proposed ZSI is higher and also cost is low when operating at $B \geq 2$.

4.10 Conclusion

In this chapter, three-modified ZSIs topologies are presented. In the proposed ZSIs, the voltage gain is increased significantly by adding one auxiliary switch and one diode without using additional passive components. The comparative analysis shows that the proposed CC-qZSI has higher boost factor (B) and higher efficiency with lesser capacitor voltage and switch current stresses, as compared to conventional qZSI. Moreover, proposed CC-qZSI has lesser stored energy in the passive components and lesser peak SDP to output power ratio as compared to conventional qZSI when operating at $B \geq 2$. Finally, the proposed ZSIs operations are tested with the simulation studies.

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