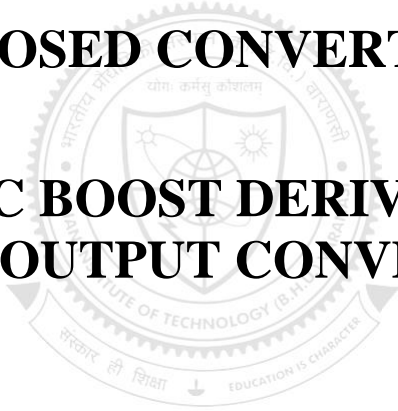# PROPOSED CONVERTER: 2

QUADRATIC BOOST DERIVED HYBRID MULTI-OUTPUT CONVERTERS

3

QUADRATIC BOOST DERIVED HYBRID MULTI-OUTPUT CONVERTERS

3.1 Introduction

The high gain minimum phase quadratic boost inverter has major advantage of no-RHPZ. However, it has less efficiency because of the presence of damping network. Since in microgrid, low voltage generation renewable energy system is a common phenomena and efficiency is a key point in this aspect. In order to incorporate the limitation of minimum phase quadratic boost converter and compact size of the system multi-output based quadratic boost converters are proposed in this chapter. The proposed multi-output based series and parallel mode topologies are presented with detailed analysis. Detailed small signal modeling, PWM control techniques and simulation studies are performed to validate the performance of proposed hybrid inverter. The detailed descriptions about the proposed converters are given in subsequent subsections.

3.2 Quadratic Boost Derived Hybrid Multi-Output Converters

With the objective of multiple ac outputs and one dc output, two (series mode and parallel mode) quadratic boost derived hybrid multi-output converters are proposed in this thesis. The proposed converters are derived by replacing the main switch of the quadratic boost converter with n- number of H Bridge inverters connected either in series or parallel. The topology which is developed from n-series connected H-bridges give series mode of the proposed converter and it is capable of giving n-number of ac outputs with variable voltages and same currents (to all the ac loads) along with one dc output. Further, the topology which is developed from n-parallel connected H-bridges give parallel mode of the proposed converter and it is capable of giving n-number of ac outputs with same voltages (to all the ac load) and variable currents along with one dc output. In this ways, the proposed hybrid converter topologies are capable of directly meeting out more than one different ac load demands directly (without any extra regulator or adaptor) unlike the conventional existing hybrid converters. Due to quadratic behaviour relatively (compared to the classical hybrid converters) small shoot-through duty is required to achieve high voltage gain. Moreover, the proposed topologies (series mode and parallel mode) have higher power density and improved reliability (due to inherent shoot-through protection property) which make them suitable to be used in compact systems with multiple ac and one dc loads. Steady state analysis, small signal modelling, and design of hybrid pulse width modulation (PWM) technique are carried out for the proposed converters (for two ac and one dc outputs) in the thesis.
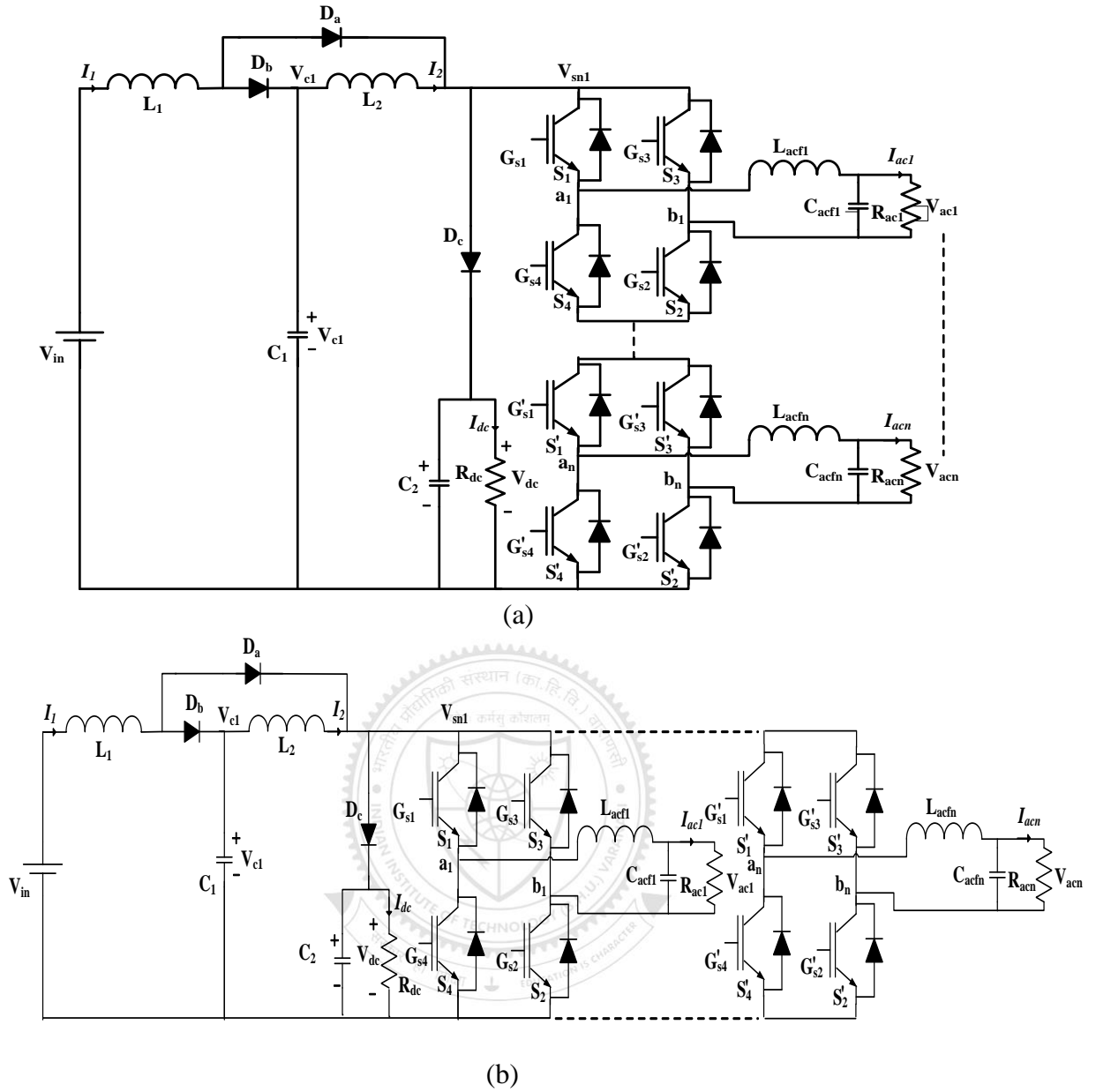
(a)

(b)

Fig. 3.1. Proposed hybrid multi-output converter topology (a) hybrid series topology, (b) hybrid parallel topology.

3.2.1 Proposed High Gain Hybrid Multi-Output Converters

The architecture of the proposed converter topologies for multiple ac and one dc outputs are shown in Fig. 3.1. Fig. 3.1(a) shows the series mode of the proposed multi-output hybrid converter which is derived by using n-number of series connected H-bridges. It is clear from Fig. 3.1(a) that the series mode of the proposed hybrid multi-output converter is capable of giving n-variable ac voltages with same currents along

with one dc output. Further, parallel mode of the proposed multi-output hybrid converter is shown in Fig. 3.1(b) which is derived by using n-number of parallel connected H- bridges. It may be noticed that the parallel mode of the proposed hybrid multi-output converter is capable of giving n-variable ac currents with same voltage along with one dc output. It is important to mention that the proposed converters are validated for n = 2 (i.e. two ac and one dc outputs) in this thesis. Thus, the subsequent sections and sections of the work deals with the proposed converter topologies for n=2 (two ac and one dc outputs).
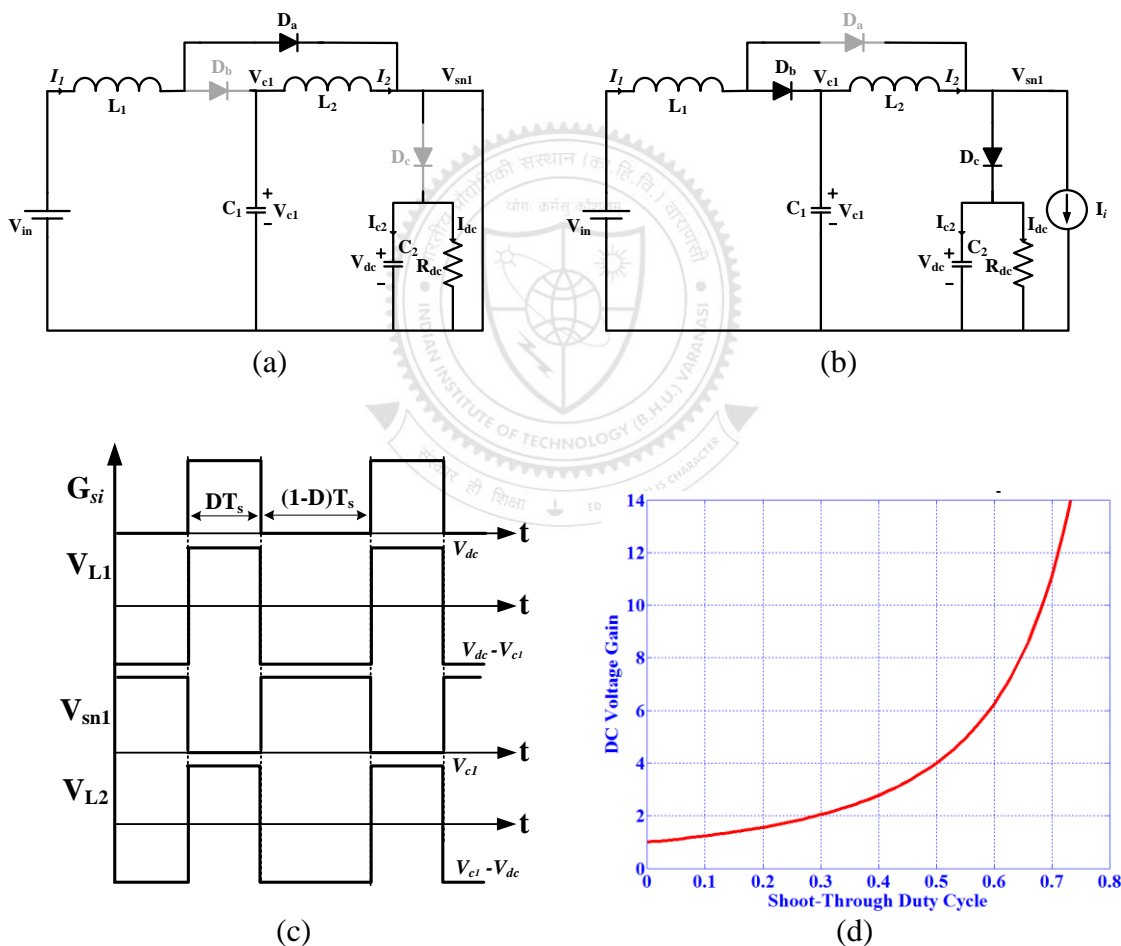

Fig. 3.2. Steady state performance of proposed converter (a) equivalent circuit during D interval, (b) equivalent circuit during $(1 - D)$ interval, (c) steady state waveform, (d) transfer characteristic of proposed converter.

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3.2.2 Operating Modes of Proposed Hybrid Multi-output Converter

The operation of the converter is divided into two states; 1) shoot through state (DT_s) and 2) non-shoot through state $(1\text{-}D)T_s$ and equivalent circuits are presented in Fig. 3.2(a) and 3.2(b) respectively. Sum of the two states is equal to one switching period. It is assumed that all the switches and elements are ideal. The operating waveforms and the transfer characteristic of the proposed hybrid multi output converters are shown in Figs. 3.2(c) and 3.2(d) respectively.

1) Shoot through state ($0 \leq t \leq DT_s$)

In this interval, diode D_a and either switches S_1-S_4 or S_2-S_3 of H-bridge network are conducting and the diodes D_b, D_c are reverse biased. Inductor L_1 stores the energy from the input dc supply and inductor L_2 stores the energy from the intermediate capacitor (C_1).

2) Non-shoot through state ($DT_s \leq t \leq (1 - D)T_s$)

In this interval, diodes D_b-D_c and either switches S_1-S_2 or S_3-S_4 of H-bridge network are conducting and diode D_a is reverse biased. The combined energy of the inductors and input dc supply is transferred to the dc and ac loads and some part of the energy is used to charge the capacitors also.

3.2.3 Steady State Analysis

The instantaneous voltage and current expressions of the energy storage elements can be derived from Fig. 3.2(a) during shoot through state.

$$L_1 \frac{di_1}{dt} = v_{in} \tag{3.1}$$

$$L_2 \frac{di_2}{dt} = v_{C1} \tag{3.2}$$

$$C_1 \frac{dv_{C1}}{dt} = -i_2 \tag{3.3}$$

$$C_2 \frac{dv_{C2}}{dt} = -i_{dc} = -\frac{v_{C2}}{R_{dc}} \tag{3.4}$$

$$v_{si} = 0 \tag{3.5}$$

Where v_{si} is the voltage across the inverter bridge. During non shoot through state following equations are derived from the Fig. 3.2(b)

$$L_1 \frac{di_1}{dt} = v_{in} - v_{C1} \tag{3.6}$$

$$L_2 \frac{di_2}{dt} = v_{C1} - v_{C2} \tag{3.7}$$

$$C_1 \frac{dv_{C1}}{dt} = i_1 - i_2 \tag{3.8}$$

$$C_2 \frac{dv_{C2}}{dt} = i_2 - i_{dc} - i_i \tag{3.9}$$

$$v_{Si} = v_{C2} \tag{3.10}$$

Under steady state condition, the average voltage across the inductor and average current through the capacitor in one switching cycle should be zero.

By applying volt-sec balance principle on L_1 and L_2, capacitor voltages are as follows,

$$V_{c1} = \frac{V_{in}}{(1-D)} \tag{3.11}$$

$$V_{C2} = \frac{V_{c1}}{(1-D)} = \frac{V_{in}}{(1-D)^2} \tag{3.12}$$

From the Fig. 3.1, dc output voltage relation is as follows,

$$V_{dc} = V_{C2} = \frac{V_{c1}}{(1-D)} = \frac{V_{in}}{(1-D)^2} \tag{3.13}$$

By applying charge-sec balance principle on C_1 and C_2

$$I_1 = \frac{I_2}{(1-D)} \tag{3.14}$$

$$I_2 = I_i + \frac{I_{dc}}{(1-D)} \tag{3.15}$$

From the above two current expressions, input current is calculated as follows,

$$I_{in} = I_1 = \frac{I_i}{(1-D)} + \frac{I_{dc}}{(1-D)^2} \tag{3.16}$$

From the transfer characteristic, it can be observed that duty cycle is varied from the $0 < D < 1$ unlike Z source inverter (ZSI) [18], switched boost inverter (SBI) [82], [86]-[87] in which shoot-through duty cycle limited to 0.5.

3.2.4 AC and DC Power Expressions

From (3.13), the dc Boost factor $= B = \frac{V_{dc}}{V_{in}} = \frac{1}{(1-D)^2}$

Note that the hybrid PWM used for this proposed hybrid multi out converter has the following constraint between modulation index (M) and D,

$$D + M \leq 1 \tag{3.17}$$

Thus, the relation between V_{in} and peak ac output voltages (V_{acpk1} and V_{acpk2}) are given below.

A. Series mode of operation

In this mode, the V_{dc} is equally divided across the inverter bridges for symmetrical ac loads and peak ac voltages (V_{acpk1} and V_{acpk2}) will be equal.

$$V_{acpk1} = V_{acpk2} = M \times \frac{V_{dc}}{2} = \frac{MV_{in}}{2(1-D)^2} \tag{3.18}$$

Where V_{acpk} ($= V_{acpk1} = V_{acpk2}$) is peak ac voltage. The ratio of peak ac voltage and input voltage can be written as

$$G = \frac{V_{acpk}}{V_{in}} = \frac{1}{2M} \tag{3.19}$$

The r.m.s. ac output voltage gain is given as $G_{ac} = \dfrac{1}{M 2\sqrt{2}}$

From (3.13) and (3.18), the ac output power (P_{ac}) and dc output power (P_{dc}) can be deduced as

$$P_{dc} = \frac{V_{dc}^2}{R_{dc}} = \frac{V_{in}^2}{R_{dc}(1-D)^4} \qquad (3.20)$$

$$P_{ac} = \frac{V_{ac}^2}{R_{ac}} = \frac{V_{acpk}^2}{2R_{ac}} = \frac{M^2 V_{in}^2}{8R_{ac}(1-D)^4} \qquad (3.21)$$

From (3.20) and (3.21), it is clear that the value of P_{dc} depends on D only and P_{ac} depends on both M and D.

B. Parallel mode of operation

In this mode the same V_{dc} is appeared across the inverter bridges for symmetrical ac loads and peak ac voltages (V_{acpk1} and V_{acpk2}) will be equal.

$$V_{acpk1} = V_{acpk2} = M \times V_{dc} = \frac{M V_{in}}{(1-D)^2} \qquad (3.22)$$

Where $V_{acpk} (= V_{acpk1} = V_{acpk2})$ is peak ac voltage. The ratio of peak ac voltage and input voltage can be written as

$$\mathrm{G} = \frac{V_{acpk}}{V_{in}} = \frac{1}{M} \qquad (3.23)$$

The r.m.s. ac output voltage gain is given as $G_{ac} = \dfrac{1}{M\sqrt{2}}$

From (3.13) and (3.22), the ac output power (P_{ac}) and dc output power (P_{dc}) can be deduced as

$$P_{dc} = \frac{V_{dc}^2}{R_{dc}} = \frac{V_{in}^2}{R_{dc}(1-D)^4} \qquad (3.24)$$

$$P_{ac} = \frac{V_{ac}^2}{R_{ac}} = \frac{V_{acpk}^2}{2R_{ac}} = \frac{M^2 V_{in}^2}{2R_{ac}(1-D)^4} \qquad (3.25)$$

From (3.24) and (3.25), it is clear that the value of P_{dc} depends on D only and P_{ac} depends on both M and D.

3.2.5 Switch Stress and Current Expressions

Voltage stresses of each component in the shoot-through duty interval (DT_s), and non-shoot-through interval ($(1-D)T_s$) interval are shown in Table 3.1. whereas current expressions of each component of the proposed converter in different states are shown in Table 3.2. Table 3.3 shows the switch current expressions of different inverter bridge switches in different states.

TABLE 3.1
VOLTAGE STRESS OF EACH COMPONENT IN DIFFERENT INTERVAL

Parameters	Shoot-through state	Non-Shoot-through state
V_{L1}	V_{in}	$\dfrac{-DV_{in}}{1-D}$
V_{L2}	$\dfrac{V_{in}}{1-D}$	$\dfrac{-DV_{in}}{(1-D)^2}$
V_{C1}	$\dfrac{V_{in}}{1-D}$	$\dfrac{V_{in}}{1-D}$
V_{C2}	$\dfrac{V_{in}}{(1-D)^2}$	$\dfrac{V_{in}}{(1-D)^2}$
V_{Da}	0	$\dfrac{-DV_{in}}{(1-D)^2}$
V_{Db}	$\dfrac{-V_{in}}{1-D}$	0
V_{Dc}	$\dfrac{-V_{in}}{(1-D)^2}$	0
V_{Si}	0	$\dfrac{V_{in}}{(1-D)^2}$

TABLE 3.2
CURRENT STRESS OF EACH COMPONENT IN DIFFERENT INTERVAL

Components	Shoot- through state	Non-Shoot through state
I_{L1}	I_{in}	I_{in}
I_{L2}	$(1-D)I_{in}$	$(1-D)I_{in}$
I_{C1}	$-(1-D)I_{in}$	DI_{in}
I_{C2}	$-I_o$	$I_2 - I_o - I_{inv}$
I_{Da}	I_{in}	0
I_{Db}	0	I_{in}
I_{Dc}	0	$\dfrac{I_{dc}}{(1-D)}$
I_{Si}	I_{in}	0

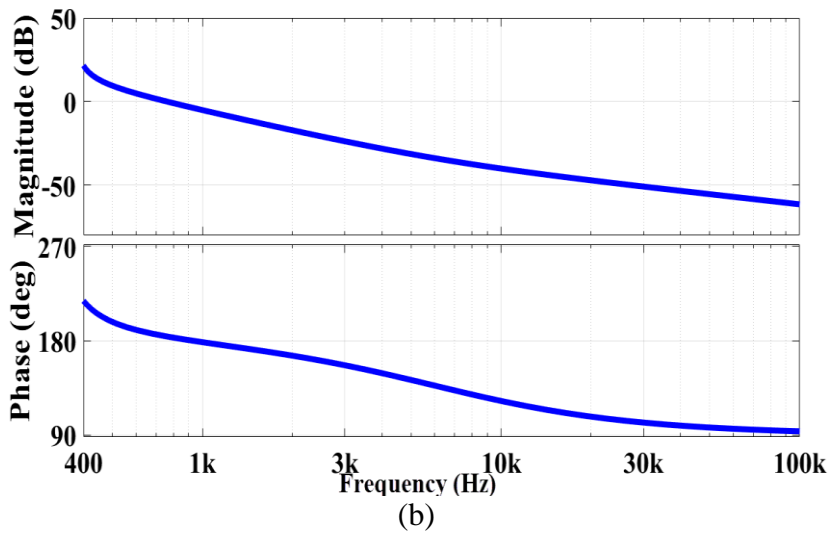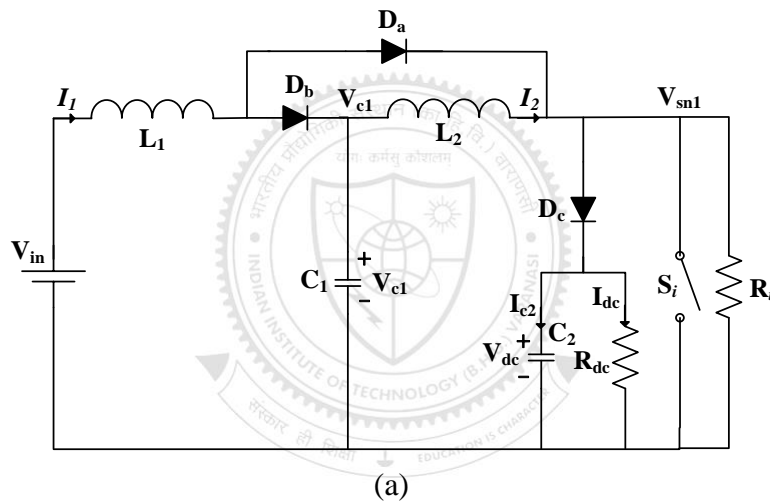| Operation Intervals	Conducting Switches	Current expression through switches			
		i_{s1}	i_{s2}	i_{s3}	i_{s4}
Shoot-Through Interval	S_1, S_4, S_2	I_2	I_{ac1}	0	$I_2 - I_{ac1}$
	S_1, S_4, S_3	$I_2 + I_{ac1}$	0	$-I_{ac1}$	I_2
	S_3, S_2, S_4	0	$I_2 + I_{ac1}$	I_2	$-I_{ac1}$
	S_3, S_2, S_1	I_{ac1}	I_2	$I_2 - I_{ac1}$	0
Power Interval	S_1, S_2	I_{ac1}	I_{ac1}	0	0
	S_3, S_4	0	0	$-I_{ac1}$	$-I_{ac1}$
Zero Interval	S_1, S_3	I_{ac1}	0	$-I_{ac1}$	0
	S_2, S_4	0	I_{ac1}	0	$-I_{ac1}$

(a)

(b)

Fig. 3.3. Small signal analysis of proposed multi-output converter (a) Simplifies circuit diagram for proposed converter, (b) Gain and phase plots.

3.3 Small Signal Analysis of Proposed Converter

The simplified equivalent circuit of proposed converter is shown in fig. 3.3(a). The small signal ac variation is denoted as ($\tilde{}$). Lower cases correspond to the instantaneous value, and upper cases correspond to the steady state value. It can be observed from Fig. 3.3(a), that in simplified circuit the inverter switch is represented as a single switch (S_i) with a parallel connection of switch load R_i. From the state space averaging technique the following differential equations are obtained.

$$L_1 \frac{d\tilde{\imath}_1}{dt} = \tilde{v}_{in} - (1-d)\tilde{v}_{C1} \tag{3.26}$$

$$L_2 \frac{d\tilde{\imath}_2}{dt} = \tilde{v}_{C1} - (1-d)\tilde{v}_{C2} \tag{3.27}$$

$$C_1 \frac{d\tilde{v}_{C1}}{dt} = (1-d)\tilde{\imath}_1 - \tilde{\imath}_2 \tag{3.28}$$

$$C_2 \frac{d\tilde{v}_{C2}}{dt} = (1-d)\tilde{\imath}_2 - \frac{\tilde{v}_{C2}}{R_{dc}} - (1-d)\frac{\tilde{v}_{C2}}{R_i} \tag{3.29}$$

The d is 1 during shoot-through interval and d is 0 during non-shoot-through interval. After applying perturbation and linearization technique to (3.26) - (3.29), leads to following state space model.

$$K\hat{\dot{x}} = A\hat{x} + B\hat{v}_{in} + [(A_1 - A_2)X + (B_1 - B_2)V_{in}]\hat{d} \tag{3.30}$$

$$\hat{\dot{x}} = (K^{-1}A)\hat{x} + (K^{-1}B)\hat{v}_{in} + K^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_{in}]\hat{d} \tag{3.31}$$

Let $\quad S_1 = (K^{-1}A); \ S_2 = (K^{-1}B); \ S_3 = K^{-1}[(A_1 - A_2)X + (B_1 - B_2)V_{in}]$

After simplify (3.31) leads to (3.32)

$$\hat{\dot{x}} = S_1\hat{x} + S_2\hat{v}_{in} + S_3\hat{d} \tag{3.32}$$

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} ; \quad A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & -1 & 1 & 0 \\ 0 & 0 & 0 & -1/R_{dc} \end{bmatrix} ;$$

$$A_2 = \begin{bmatrix} 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 \\ 1 & -1 & 1 & 0 \\ 0 & 1 & 0 & -\dfrac{1}{R_i} - \dfrac{1}{R_{dc}} \end{bmatrix}$$

$$B_1 = [1 \quad 0 \quad 0 \quad 0]^T \; ; \; B_2 = [1 \quad 0 \quad 0 \quad 0]^T ;$$

$$A_1 - A_2 = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 1/R_i \end{bmatrix}$$

$$B_1 - B_2 = [0 \quad 0 \quad 0 \quad 0]^T$$

$$A = A_1 D + A_2(1-D) = \begin{bmatrix} 0 & 1 & -(1-D) & 0 \\ 0 & 0 & 1 & -(1-D) \\ -(1-D) & -1 & 0 & 0 \\ 0 & -(1-D) & 0 & -\dfrac{(1-D)}{R_i} - \dfrac{1}{R_{dc}} \end{bmatrix} \quad (3.33)$$

$$B_1 D + B_2(1-D) = [1 \quad 0 \quad 0 \quad 0]^T \tag{3.34}$$

$$X = [I_1 \quad I_2 \quad V_{C1} \quad V_{C2}]^T ; \tag{3.35}$$

$$\dot{x} = \frac{d}{dt}[i_1 \quad i_2 \quad v_{C1} \quad v_{C2}]^T \tag{3.36}$$

From (3.32), the control to output transfer function for the proposed converter deduced as follows:

$$\frac{\hat{v}_o}{\hat{d}} = [0 \quad 0 \quad 0 \quad 1 \quad 0][sI - S_1]^{-1}S_3 \tag{3.37}$$

$$\frac{\widehat{V_0}}{\hat{d}} = \frac{A's^3 + B's^2 + C's + D'}{A''s^4 + B''s^3 + C''s^2 + D''s + E''} \tag{3.38}$$

The values of coefficients $A' - D'$ and $A'' - E''$ of (3.38) are given in the Appendix D. The gain and phase plots of the transfer function (3.38) are shown in Fig. 3.3(b) for the values mentioned in Table 3.4. From Fig. 3.3(b), it can be observed that the bandwidth (gain cross over frequency) of the proposed converter is 764Hz and the Phase margin of the proposed converter is 3.94^0. This information may be utilized to design the feedback loop for the proposed converters as per load requirement.

TABLE 3.4
LISTS OF PARAMETERS WITH THEIR ATTRIBUTES

Prototype Specification	
Parameters	**Attributes**
Inductors	L_1= 1183 µH, L_2=2023 µH
Capacitance	C_1 =147 µF, C_2 =940 µF
Carrier Frequency	f_{tg}=10 kHz
Fundamental Frequency	50Hz

3.4 Simulation Studies

The proposed quadratic boost derived hybrid multi-output converter topologies are validated with 250 W prototype. Parameters with their attributes are listed in the Table 3.6. The PWM control technique for the proposed multi-output converter is given in Fig. 3.4. Figs. 3.4(a) and (b) shows the simulation results of the gating signal given to the switches of the proposed multi-output converter when $V_{ref} > 0$ and $V_{ref} < 0$, respectively.
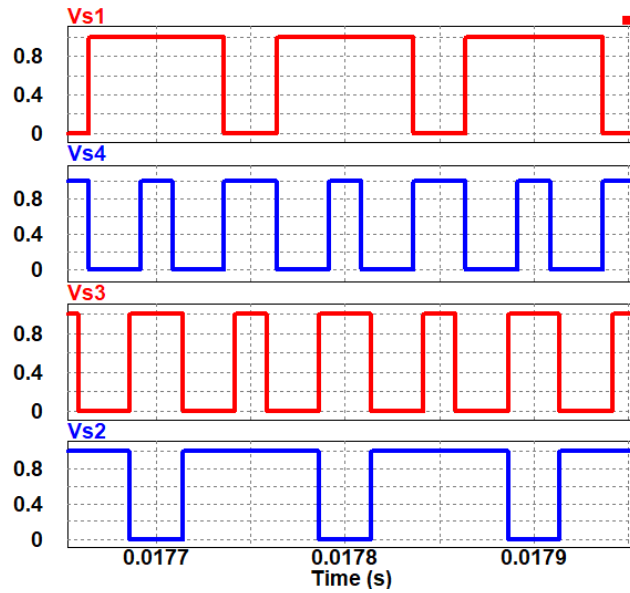
(a)
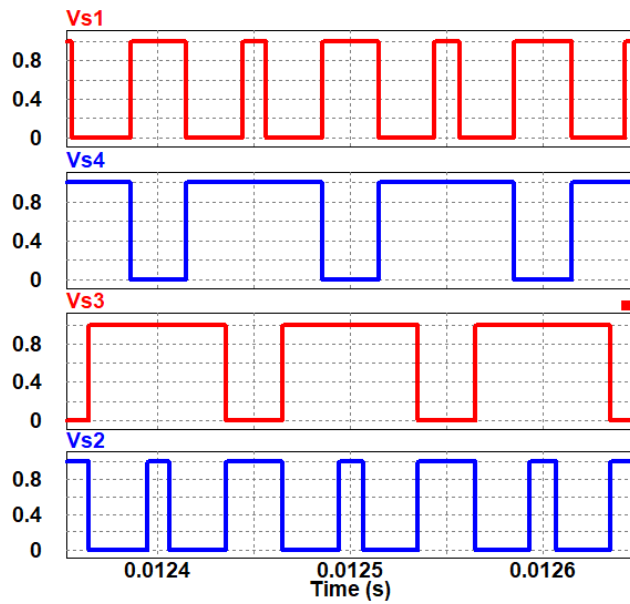
(b)

Fig. 3.4 Simulation verification of PWM for the proposed hybrid multi-output inverter (a) when $V_{ref} > 0$, (b) when $V_{ref} < 0$.

3.4.1 Proposed Converter in Parallel Mode

The proposed concept is verified with simulation for parallel mode of operation (P_{dc} =150 W and P_{ac} =100 W). In parallel converter topology, same switch node voltage is appeared across the parallel inverters and current drawn by the inverters are divided according to the ac loads. Steady state simulation results of the proposed converter

considering non-idealities for two parallel ac and one dc outputs for $D = 0.4$ and $M=0.5$ are shown in Fig. 3.5. It is observed from Fig. 3.5 that two ac output voltages $V_{ac1} = 66.7$ V (pk-pk) and $V_{ac2} = 66.7$ V (pk-pk) along with dc output voltage $V_{dc} = 66.7$ V are obtained from the input voltage $V_{in} = 24$ V.
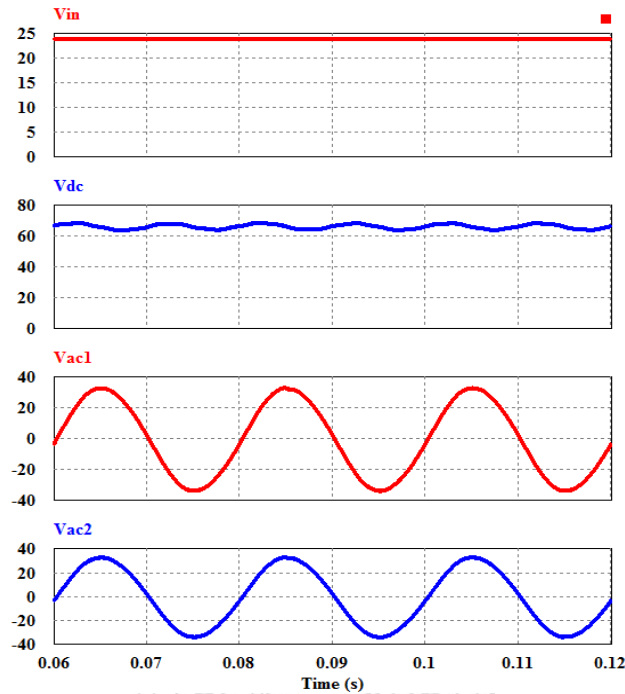

Fig. 3.5. Simulation verification for parallel topology ($D = 0.4$ and $M = 0.5$).

3.4.2 Proposed Converter in Series Mode

In series converter topology, current drawn by the inverters is same and switch node voltage is divided according to the ac loads. Steady state simulation results of the proposed converter for two series ac and one dc outputs for $D = 0.4$ and $M=0.5$ are shown in Fig. 3.6. It is observed from Fig. 3.6 that the proposed series mode hybrid converter give two series ac output voltages $V_{ac1} = 19.4$V (pk-pk) and $V_{ac2} = 20.5$V (pk-pk) along with dc output voltage $V_{dc} = 63.6$V for the input voltage $V_{in} = 24$V. The, simulation results confirm the steady state behavior of the proposed multi-output series mode topology.
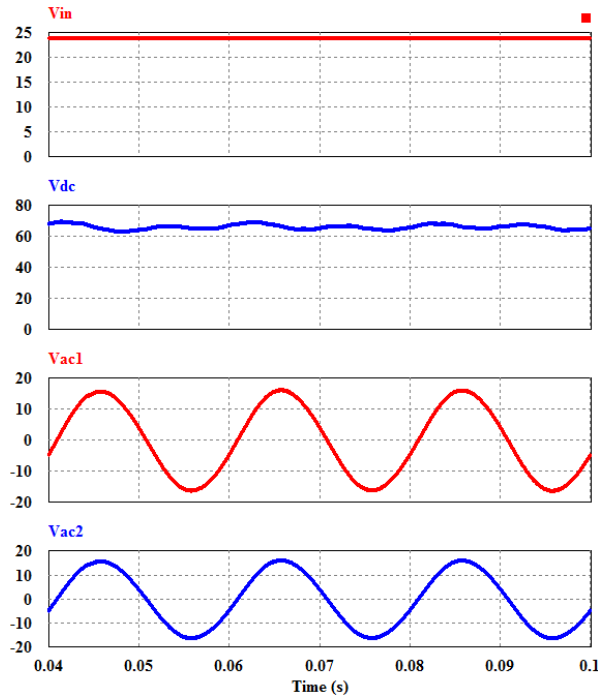
Fig. 3.6. Simulation verification for series topology ($D = 0.4$ and $M = 0.5$).

3.4.3 Dynamic Performance

The dynamic performance of the proposed converters (parallel mode) is validated in closed loop with simulation results. The simulation results of the closed loop dynamic performance are given in Fig. 3.7. The dc output voltage is set as 67 V and both ac output voltages are set equal to 39 V peak for reference signal of 50 Hz. The dc load resistance changes between 30 Ω to 15 Ω and the load current changes between 2.24 A to 4.48 A keeping the ac loads constant. It may be observed from Fig. 3.7(a) and 3.7(b) that for the dc load change, the dc output voltage settles within 40 ms, which shows the dc voltage controller effectiveness. Further, the ac1 load resistances changes between 20 Ω to 10 Ω (load current 1.94A (p-p) to 3.54A (p-p)) keeping dc and ac2 loads constant. It may be observed from the Figs. 3.7(c) and 3.7(d) that ac1 output voltage quickly settles for ac1 load changes, which show effectiveness of ac voltage controller.
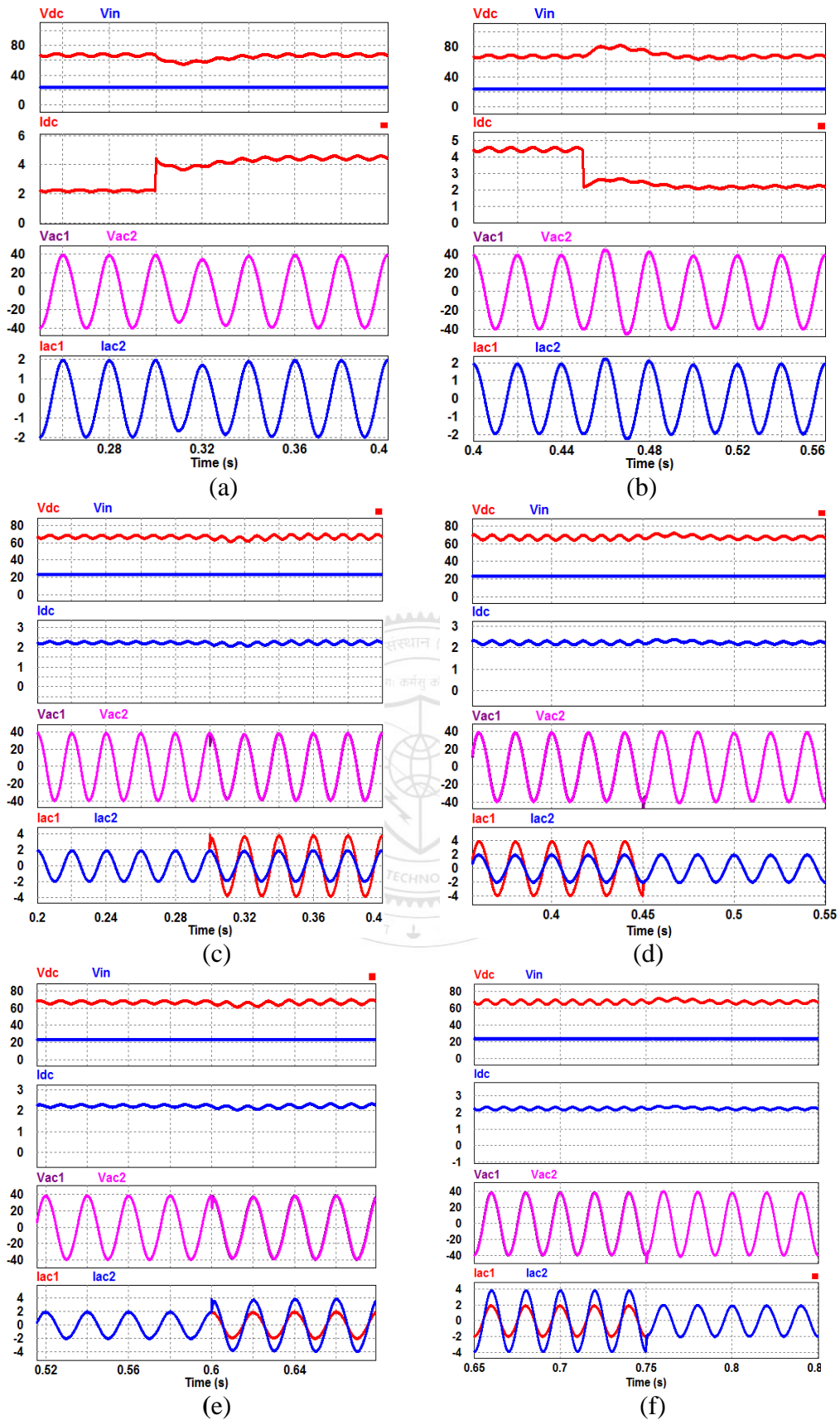
Fig. 3.7. Closed loop dynamic response of the proposed concept (a) Step-up change in the dc load current, (b) Step-down change in the dc load current, (c) Step-up change in the ac1 load current, (d) Step-down change in the ac1 load current, (e) Step-up change in the ac2 load current, (f) Step-down change in the ac2 load current.

In the same manner, the ac2 load resistance changes between 20 Ω to 10 Ω keeping dc and ac1 loads constant. It is clear from Fig. 3.7(e) and 3.7(f) that ac2 output voltage quickly settles for ac2 load changes. The results shown in Fig. 3.7 validate the effectiveness of ac and dc voltage controller.

3.5 Conclusion

The proposed converters are derived by replacing the main switch of the quadratic boost converter with n- number of H Bridge inverters connected either in series or parallel. The topology which is developed from n-series connected H-bridges give series mode of the proposed converter and it is capable of giving n-number of ac outputs with variable voltages and same currents (to all the ac loads) along with one dc output. Steady state, small signal modeling and dynamic modeling have been carried out for analyzing the behavior of the proposed hybrid converter for two ac and one dc outputs. Simulation studies are performed to test the proposed parallel and series mode topologies for two ac outputs and single dc output.