PROPOSED CONVERTER: 1

HIGH GAIN MINIMUM PHASE QUADRATIC BOOST HYBRID INVERTER

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2.1 Introduction

The cascaded boost with VSI is commonly used topologies for microgrid applications. To achieve gain let say 5 times of input voltage, converter need to operates at extreme duty cycle, which further leads to severe reverse recovery of the diodes, increases EMI, and decreases efficiency. The summation of duty cycle and modulation index is also restricted to one. So, to achieve higher gain converter need to operate on higher duty cycle but this leads to lower modulation index. The low values of modulation index will result into poor fundamental frequency component with increased harmonic distortion. In that case quadratic boost converter is a good option to achieve high gain in low duty cycle. The basic bi-directional dc-dc quadratic converter without coupled inductor and with couple inductor is given in the appendix A and B. The quadratic based converter is capable of high gain in small duty cycle. In this chapter, high gain minimum phase quadratic boost hybrid inverter is proposed for microgrid applications. The detailed

operating principles, steady-state analysis, small signal modeling, PWM control techniques and simulation studies are performed for the proposed hybrid inverter. The detailed description about the proposed inverter is given in subsequent subsections.

2.2 Minimum Phase Quadratic Boost Hybrid Inverter

The proposed hybrid inverter is derived from the quadratic boost converter therefore, for relatively low duty ratio high voltage gain can be achieved for dc output. Point wise advantages and features of the proposed hybrid inverter are as follows:

1. The proposed hybrid inverter does not display any RHPZ in the control-to-output transfer function and therefore, it gives minimum phase behaviour unlike the conventional inverters such as ZSI, SBI, etc. It provides simultaneously ac and dc outputs and thus, gives better processing density and high reliability (due to inherent shoot through protection).

2. It is capable of operating on wide range of shoot-through duty cycle ($0 < D < 1$). In the proposed inverter, the shoot through duty ratio is not limited to 0.5 (unlike to classical hybrid inverters where the maximum possible shoot through duty is 0.5 only). Therefore, it is capable of giving high dc voltage step-up.

3. It gives better EMI noise immunity and inherent shoot through protection ability.

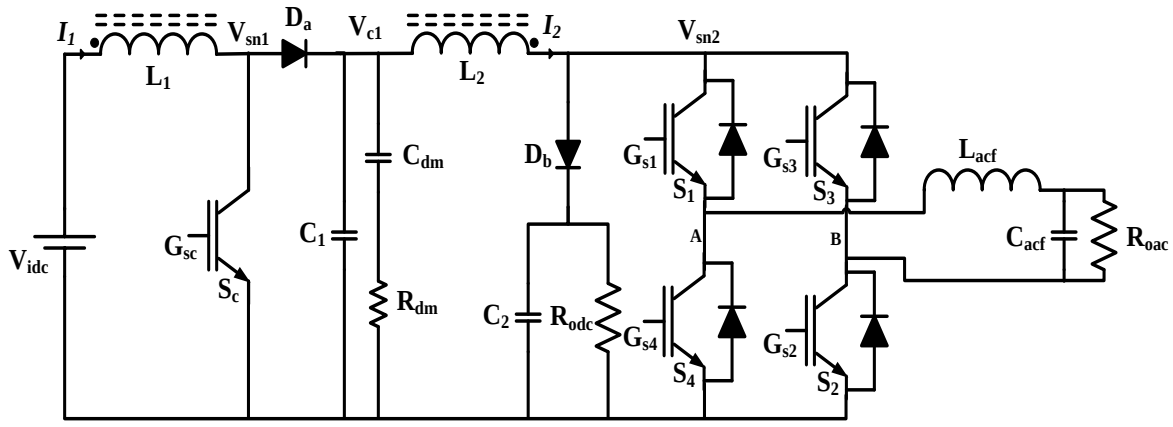


Fig. 2.1. Proposed high gain hybrid quadratic boost inverter.

2.2.1 Operating Principle of High Gain Hybrid Inverter

The proposed high step–up hybrid inverter is shown in Fig. 2.1. It can be observed from Fig. 2.1 that the filter inductors (L_1, L_2) of the quadratic boost converter are magnetically coupled having mutual inductance M_i, and a R_{dm} - C_{dm} damping system is introduced in the circuit. Further, load side switch of the classical quadratic boost converter is replaced with an H-bridge voltage source inverter network. With this circuit arrangement, the proposed hybrid inverter gives simultaneous ac and dc outputs with no RHPZ in the control-to-output transfer function and thereby giving minimum phase system. Switches S_1-S_4 shown in Fig. 2.1 are the four switches of the H-bridge inverter leg, whereas control switch is S_c having gate signal G_1- G_4 and G_{sc} respectively. V_{sn1} and V_{sn2} are the two switch node voltages; V_{c1} is voltage across capacitor C_1 with input voltage (V_{idc}). Ac voltage across the load R_{oac} is $V_{oac,}$ and dc voltage across the load R_{odc} is V_{odc}.

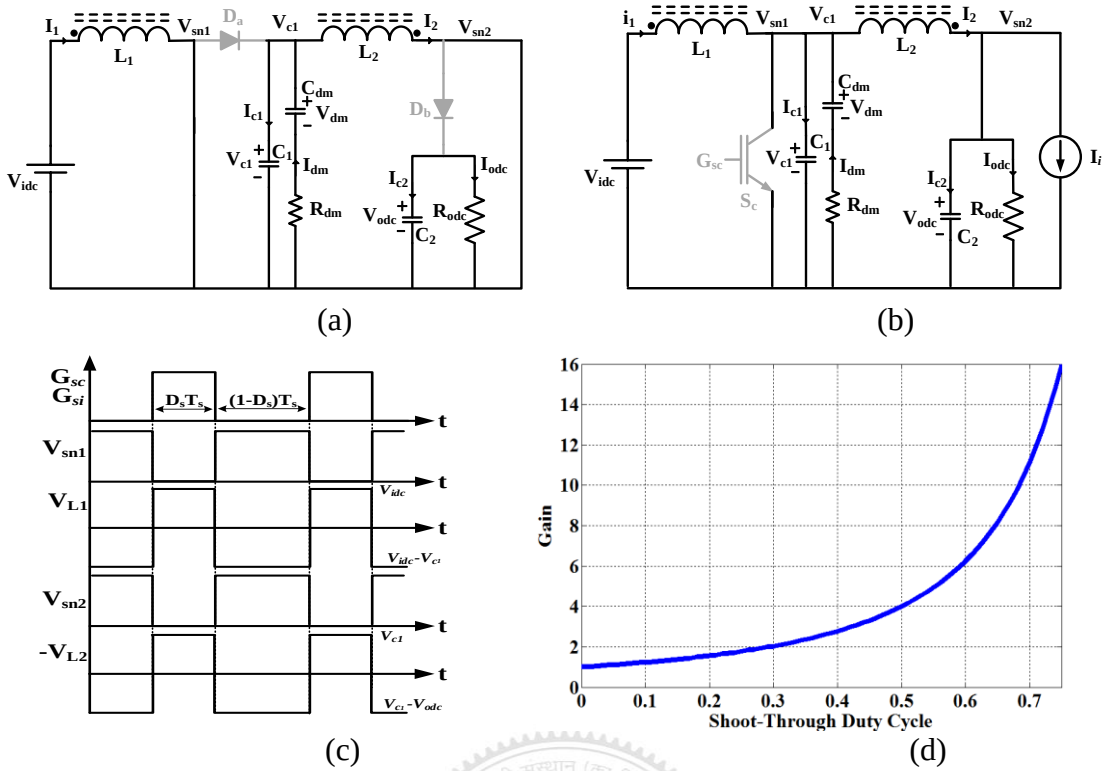


Fig. 2.2. Steady state performance of the proposed inverter (a) equivalent circuit during DT_s interval, (b) equivalent circuit during $(1-D)T_s$) interval, (c) steady state operating waveforms, (d) transfer characteristic of proposed hybrid inverter.

2.2.2 Operating Modes of the Proposed High Gain Hybrid Inverter

Operation of the proposed hybrid inverter is shown in Figs. 2.2 (a) and 2.2(b) show the equivalent circuit of the proposed hybrid inverter in shoot-through interval (DT_s) and non-shoot-through interval $((1-D)T_s)$, respectively. It is assumed that there is no parasitic effect. All the switches and elements are assumed to be ideal. Sum of both the intervals is equal to the one switching period T_s ($T_s = \frac{1}{f_{tg}}$). Fig. 2.2(c) shows the key operating waveforms and Fig. 2.2(d) shows the transfer characteristic of the proposed hybrid inverter.

1) Shoot-through interval Mode

During the shoot-through interval (DT_s), the control switch (S_c) and either switches S_1-S_4 or S_3-S_2 are ON. This makes diode D_a and D_b reverse biased. Both

the switch nodes voltages (V_{sn1} and V_{sn2}) are zero. In this mode, inductors (L_1, L_2) currents start building-up and reaches up to a maximum value.

2) Non-shoot-through interval Mode

During the non-shoot-through interval ($(1-D)T_s$), stored energy in the inductors is transferred to the output through diode, D_a and D_b. During this interval control switch S_c is OFF and either switches S_1 - S_2 or S_3 - S_4 conducted. Capacitors C_1, C_2, and C_{dm} are charged through the input supply voltage V_{idc} with currents I_1 and I_2. In this interval supply V_{idc} and both inductor (L_1, L_2) current supply the power to the inverter circuit.

2.2.3 Steady-State Analysis

Assuming small ripple approximation, during the DT_s interval, following equations can be derived from Fig. 2.2(a)

$$V_{idc} = L_1 \frac{di_1}{dt} - \frac{M_i di_2}{dt} \tag{2.1}$$

$$V_{c1} = L_2 \frac{di_2}{dt} - \frac{M_i di_1}{dt} \tag{2.2}$$

$$C_1 \frac{dV_{c1}}{dt} = \left(\frac{V_{dm}-V_{c1}}{R_{dm}}\right) - i_2 \tag{2.3}$$

$$C_{dm} \frac{dV_{dm}}{dt} = -\left(\frac{V_{dm}-V_{c1}}{R_{dm}}\right) \tag{2.4}$$

$$C_2 \frac{dV_{odc}}{dt} = -\frac{V_{odc}}{R_{odc}} \tag{2.5}$$

Assuming small ripple approximation, during the $(1-D)T_s$ interval, following equations are derived from the Fig. 2.2(b)

$$V_{idc} - V_{c1} = L_1 \frac{di_1}{dt} - \frac{M_i di_2}{dt} \tag{2.6}$$

$$V_{c1} - V_{odc} = L_2 \frac{di_2}{dt} - \frac{M_i di_1}{dt} \tag{2.7}$$

$$C_1 \frac{dV_{c1}}{dt} = i_1 + i_{dm} - i_2 \tag{2.8}$$

$$C_{dm}\frac{dV_{dm}}{dt} = -\left(\frac{V_{dm}-V_{c1}}{R_{dm}}\right) \tag{2.9}$$

$$C_2\frac{dV_{c2}}{dt} = \ i_2 - V_{odc}\left(\frac{1}{R_{odc}}+\frac{1}{R_i}\right) \tag{2.10}$$

Under steady state condition, the average voltage across the inductor and average current through the capacitor in one switching cycle should be zero.

By applying voltage second balance on L_1, following is obtained

$$V_{idc}D + (V_{idc} - V_{c1})(1-D) = 0 \tag{2.11}$$

$$\Longrightarrow V_{c1} = \frac{V_{idc}}{(1-D)}$$

Similarly, following is achieved by applying voltage second balance on L_2.

$$V_{c2}D + (V_{c1} - V_{odc})(1-D) = 0$$

$$\Longrightarrow V_{odc} = \frac{V_{c1}}{(1-D)} = \frac{V_{idc}}{(1-D)^2} \tag{2.12}$$

By applying charge second balance on C_1, following is obtained.

$$(-I_2)D + (I_1 - I_2)(1-D) = 0 \tag{2.13}$$

$$\Longrightarrow I_1 = \frac{I_2}{(1-D)}$$

Similarly, By applying charge second balance on C_2, following is achieved.

$$\left(-\frac{V_{odc}}{R_{odc}}\right)D + I_2 - V_{odc}\left(\frac{1}{R_{odc}}+\frac{1}{R_i}\right)(1-D) = 0 \tag{2.14}$$

$$\Longrightarrow I_2 = \frac{V_{odc}}{(1-D)}\left(\frac{1}{R_{odc}}+\frac{1-D}{R_i}\right)$$

(2.14) can be also be written as,

$$I_{odc} = (I_2 - I_i)(1-D) \tag{2.15}$$

$$\Longrightarrow I_{odc} = (1-D)^2 I_1 - (1-D)I_i \tag{2.16}$$

Switched current is calculated as

$$I_i = (1-D)I_1 - \frac{V_{idc}}{(1-D)^3 R_{odc}} \tag{2.17}$$

By using (2.12), the transfer characteristic ($\frac{V_{odc}}{V_{idc}}$) is plotted and shown in Fig.2.2 (d). It can be noted here that for proposed hybrid inverter, duty cycle can be varied between 0 and 1 (0 < D <1) unlike the ZSI, SBI and current fed switched boost inverter in which shoot-through duty cycle limited to 0.5.

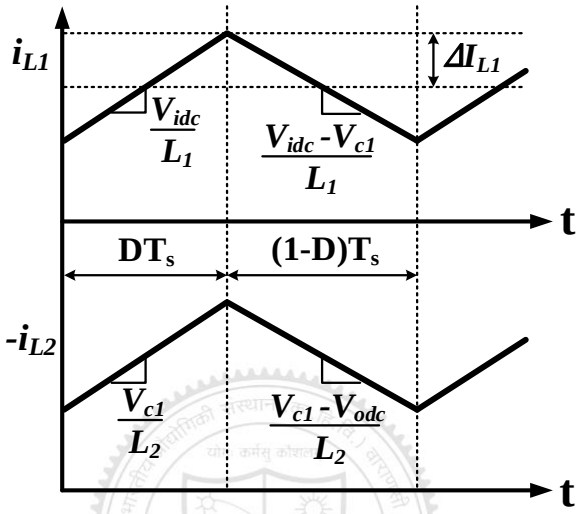


Fig. 2.3. Inductor currents behaviour in the proposed inverter.

2.2.4 High Frequency Ripple Analysis

High frequency inductor current ripple and capacitor voltage ripple are also investigated. As shown in the Fig. 2.3 during shoot-through interval (DT_s) inductor stores energy and energy is released during non-shoot-through interval ((1- D) T_s). The corresponding equations are given in (2.1)-(2.2) and (2.6)-(2.7).

From Fig. 2.3, slope of inductor current (i_{L1}) during interval DT_s is

$$\frac{di_{L1}(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_{idc}}{L_1} \tag{2.18}$$

and slope of inductor current (i_{L1}) during interval (1-D) T_s is

$$\frac{di_{L1}(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_{idc}-V_{c1}}{L_1} \tag{2.19}$$

Similarly, for inductor current (i_{L2}) slope during interval DT_s and (1-D) T_s are written as

$$\frac{di_{L2}(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{V_{c1}}{L_2} \tag{2.20}$$

$$\frac{di_{L2}(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{V_{c1} - V_{odc}}{L_2} \tag{2.21}$$

High frequency ripple is calculated by analyzing the change in the inductor current during shoot-through interval DT_s. Total inductor current (i_{L1}, i_{L2}) ripples during this interval is calculated as follows by multiplying the slope with the length of the interval:

$$2\Delta i_{L1} = \frac{V_{idc}}{L_1} DT_s$$

$$\Delta i_{L1} = \frac{V_{idc}}{2L_1} DT_s \tag{2.22}$$

Similarly, $$\Delta i_{L2} = \frac{V_{c1}}{2L_2} DT_s \tag{2.23}$$

Thus, by selecting a desired high frequency ripple magnitude, the inductor values can be calculated from (2.22) and (2.23).

Capacitor voltage is analyzed based on the high frequency ripple is shown in Fig. 2.4. The corresponding equations are given in (2.3)-(2.5) and (2.8)-(2.10) of the revised manuscript. Current in the $R_{dm} - C_{dm}$ damping network is almost negligible ($i_{dm} \approx 0$). So, it is assumed that the $V_{dm} \approx V_{c1}$.

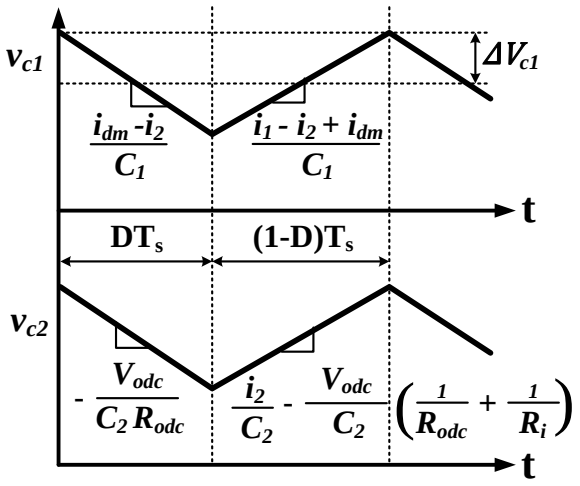


Fig. 2.4. Capacitor voltages behaviour in the proposed inverter.

From Fig. 2.4, the slope of capacitor voltage (V_{c1}) during interval DT_s is

$$\frac{dV_{c1}(t)}{dt} = \frac{i_{c1}(t)}{C_1} = \frac{i_{dm} - i_2}{C_1} \tag{2.24}$$

and the slope capacitor voltage (V_{c1}) during interval (1-D) T_s is

$$\frac{dV_{c1}(t)}{dt} = \frac{i_{c1}(t)}{C_1} = \frac{i_1 - i_2 + i_{dm}}{C_1} \tag{2.25}$$

Similarly, for the capacitor voltage (V_{c2}), slopes during interval DT_s and (1-D) T_s are written as follows

$$\frac{dV_{c2}(t)}{dt} = \frac{i_{c2}(t)}{C_2} = -\frac{V_{odc}}{C_2 R_{odc}} \tag{2.26}$$

$$\frac{dV_{c2}(t)}{dt} = \frac{i_{c2}(t)}{C_2} = \frac{i_2}{C_2} - \frac{V_{odc}}{C_2}\left(\frac{1}{R_{odc}} + \frac{1}{R_i}\right) \tag{2.27}$$

High frequency voltage ripple is calculated by analyzing the change in capacitor voltages during shoot-through interval DT_s. Total capacitor voltage (V_{c1}, V_{c2}) ripples during this interval is calculated as follows by multiplying the slopes with the length of the interval:

$$2\Delta V_{c1} = \frac{i_{dm} - i_2}{C_1}\, DT_s$$

$$\Longrightarrow \Delta V_{c1} = \frac{i_{dm} - i_2}{2C_1}\, DT_s \tag{2.28}$$

Similarly, $$\Delta V_{c2} = \frac{V_{odc}}{2C_2 R_{odc}}\, DT_s \tag{2.29}$$

Using (2.28) and (2.29), the values of capacitors can be calculated.

2.2.5 AC and DC Power Expressions

Form (2.12), it is obtained that the dc Boost factor = $B = \frac{V_{odc}}{V_{idc}} = \frac{1}{(1-D)^2}$

Further, the PWM used for the proposed hybrid inverter has the following constraint on modulation index (M) and D as

$$M + D \leq 1 \tag{2.30}$$

It is important to note here that the maximum ac output voltage would be obtained for $M = 1 - D$.

The relation between V_{idc} and ac output peak voltage (V_{opk}) is given as,

$$V_{opk} = M \times V_{odc} = \frac{MV_{idc}}{(1-D)^2} \tag{2.31}$$

where V_{opk} voltage is the peak ac voltage and ratio can be written as,

$$\text{G} = \frac{V_{opk}}{V_{idc}} = \frac{1}{M} \tag{2.32}$$

AC output voltage gain is given as $G_{ac} = \frac{1}{M\sqrt{2}}$

From (2.12) and (2.16), the ac output power (P_{oac}) and dc output power (P_{odc}) is governed by

$$P_{odc} = \frac{V_{odc}^2}{R_{odc}} = \frac{V_{idc}^2}{R_{odc}(1-D)^4} \tag{2.33}$$

$$P_{oac} = \frac{V_{oac}^2}{R_{oac}} = \frac{V_{opk}^2}{2R_{oac}} = \frac{M^2 V_{idc}^2}{2R_{oac}(1-D)^4} \tag{2.34}$$

From expression (2.33) and (2.34), it is clear that the value of P_{odc} depends only on D but P_{oac} depends on both M and D.

TABLE 2.1
CURRENT EXPRESSION OF DIFFERENT SWITCHES IN PROPOSED HIGH GAIN INVERTER

Operation Intervals	Conducting Switches	Current expression through switches				
		i_{s1}	i_{s2}	i_{s3}	i_{s4}	i_{sc}
Shoot-Through Interval	S_1, S_4, S_2, S_c	I_2	I_{oac}	0	$I_2 - I_{oac}$	I_1
	S_1, S_4, S_3, S_c	$I_2 + I_{oac}$	0	$-I_{oac}$	I_2	I_1
	S_3, S_2, S_4, S_c	0	$I_2 + I_{oac}$	I_2	$-I_{oac}$	I_1
	S_3, S_2, S_1, S_c	I_{oac}	I_2	$I_2 - I_{oac}$	0	I_1
Power Interval	S_1, S_2	I_{oac}	I_{oac}	0	0	0
	S_3, S_4	0	0	$-I_{oac}$	$-I_{oac}$	0
Zero Interval	S_1, S_3	I_{oac}	0	$-I_{oac}$	0	0
	S_2, S_4	0	I_{oac}	0	$-I_{oac}$	0

2.2.6 Switch Stress and Current Expressions

It can be observed from Fig. 2.1 that the maximum input voltage to the inverter bridge will be dc output voltage V_{odc}. The switching stress will be designed in consideration of the maximum voltage appearing across the switches. Therefore, the switching stresses of the inverter switches and control switch will be V_{odc} and V_{c1}, respectively.

The maximum current through D_a, D_b is I_1, I_2, respectively during non-shoot-through duty cycle and currents will be zero during shoot-through duty cycle. Table 2.1 shows the current details of different switches in the shoot-through duty cycle (DT_s) and non-shoot-through interval ($(1-D)T_s$).

2.3 Small Signal Analysis of Proposed Hybrid Inverter

The simplified equivalent circuit of the proposed hybrid inverter is shown in Fig. 2.5. The small signal ac variation is denoted as ($\tilde{}$). Lower cases correspond to the instantaneous value, and upper cases correspond to the steady state value. In this simplified circuit, the inverter H-bridge network is represented as a single switch (S_i)

with a resistive load R_i connected in parallel to it [87]. Using state space averaging method, following differential equations are obtained.

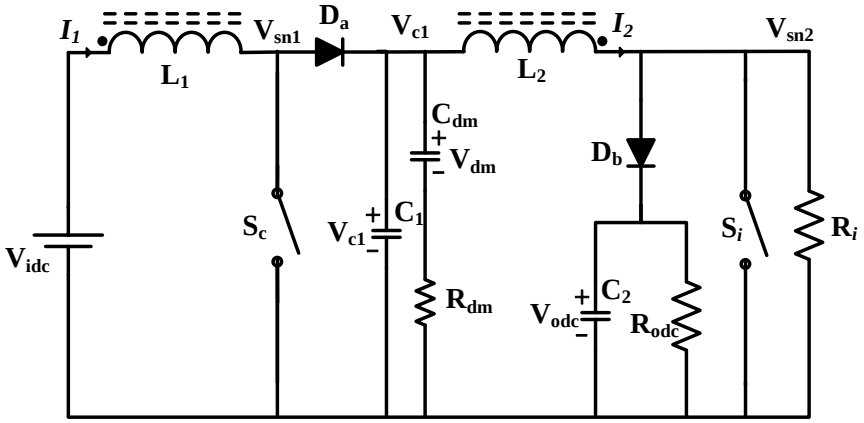


Fig. 2.5. Simplified circuit diagram of the proposed hybrid inverter.

$$\frac{d\tilde{\imath}_1}{dt} = \frac{M_i(\tilde{v}_{c1}+(d-1)\tilde{v}_{odc})+L_2(\tilde{v}_{idc}+(d-1)\tilde{v}_{c1})}{(L_1L_2-M_i^2)} \tag{2.35}$$

$$\frac{d\tilde{\imath}_2}{dt} = \frac{L_1(\tilde{v}_{c1}+(d-1)\tilde{v}_{odc})+ M_i(\tilde{v}_{idc}+(d-1)\tilde{v}_{c1})}{(L_1L_2-M_i^2)} \tag{2.36}$$

$$\frac{d\tilde{v}_{c1}}{dt} = \frac{\tilde{v}_{dm}-\tilde{v}_{c1}}{R_{dm}C_1} - \frac{(d-1)\tilde{\imath}_1}{C_1} - \frac{\tilde{\imath}_2}{C_1} \tag{2.37}$$

$$\frac{d\tilde{v}_{odc}}{dt} = \frac{(1-d)\tilde{\imath}_2}{C_2} - \frac{\tilde{v}_{odc}}{C_2}\left(\frac{1}{R_{odc}} + \frac{(1-d)}{R_i}\right) \tag{2.38}$$

$$\frac{d\tilde{v}_{dm}}{dt} = -\frac{\tilde{v}_{dm}-\tilde{v}_{c1}}{R_{dm}C_{dm}} \tag{2.39}$$

where M_i is a mutual inductance between L_1 and L_2. Perturbation and linearization of above equation leads to following state space model.

$$\frac{d}{dt}\begin{bmatrix}\hat{\imath}_1\\ \hat{\imath}_2\\ \hat{v}_{c1}\\ \hat{v}_{odc}\\ \hat{v}_{dm}\end{bmatrix} = [A]\times\begin{bmatrix}\hat{\imath}_1\\ \hat{\imath}_2\\ \hat{v}_{c1}\\ \hat{v}_{odc}\\ \hat{v}_{dm}\end{bmatrix} + [B]^T \times [\widehat{v_{idc}}] + [F]^T \times [\hat{d}]$$

Where,

$$[A]=\begin{bmatrix} 0 & 0 & \frac{M_i+DL_2-L_2}{L_1L_2-M_i^2} & \frac{D\,M_i-M_i}{L_1L_2-M_i^2} & 0 \\ 0 & 0 & \frac{L_1+D\,M_i-M_i}{L_1L_2-M_i^2} & \frac{DL_1-L_1}{L_1L_2-M_i^2} & 0 \\ \frac{1-D}{C_1} & \frac{-1}{C_1} & \frac{-1}{R_{dm}C_1} & 0 & \frac{1}{R_{dm}C_1} \\ 0 & \frac{1-D}{C_2} & 0 & \frac{-1}{C_2}\left(\frac{1}{R_{odc}}+\frac{(1-D)}{R_i}\right) & 0 \\ 0 & 0 & \frac{1}{R_{dm}C_{dm}} & 0 & \frac{-1}{R_{dm}C_{dm}} \end{bmatrix},$$

$$[B]=\left[\frac{L_2}{L_1L_2-M_i^2} \quad \frac{M_i}{L_1L_2-M_i^2} \quad 0 \quad 0 \quad 0\right],$$

$$[F]=\begin{bmatrix} \frac{L_2V_{c1}+M_iV_{odc}}{L_1L_2-M_i^2} & \frac{M_iV_{c1}+L_1V_{odc}}{L_1L_2-M_i^2} & \frac{-I_{L_1}}{C_1} & \frac{-I_{L_2}}{C_2} & 0 \end{bmatrix}$$

From above, the open loop control-to-output transfer function for the proposed hybrid inverter is deduced as follows:

$$\frac{\hat{v}_o}{\hat{d}}=[0 \quad 0 \quad 0 \quad 1 \quad 0][sI-A]^{-1}[F]$$

$$\frac{\widehat{V_0}}{\hat{d}}=\frac{A's^4+B's^3+C's^2+D's+E'}{A''s^5+B''s^4+C''s^3+D''s^2+E''s+F''} \tag{2.40}$$

The values of coefficients $A'-E'$ and $A''-F''$ of (2.40) are given in the Appendix C. Fig. 2.6 shows the Bode plots analysis of the proposed hybrid inverter. As shown in Fig. 2.6, gain plot and phase plot varies with coefficient of coupling (k) between the L_1 and L_2. It is found from the Fig 2.6, that the open loop control-to-output transfer function does not have RHP zero for quadratic boost operation. This validates that the converter is a minimum phase system. As the system becomes a minimum phase, the controller design becomes simpler.

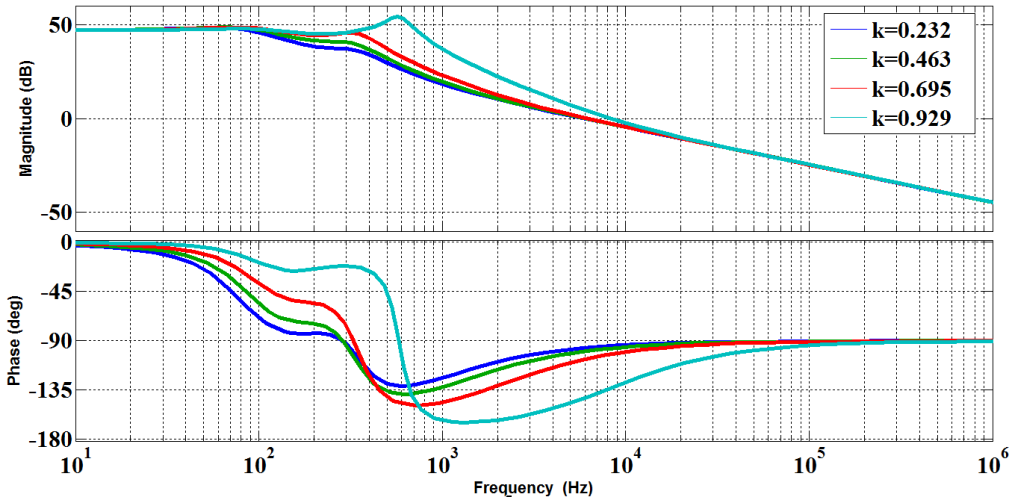


Fig. 2.6. Bode plot (gain and phase) of control-to-output transfer function. Parameters: $V_{idc} = 24$ V, $L_1 = 1800\mu$H, $L_2 = 2500\mu$H, $C_1 = 100\mu$F, $C_2 = 200\mu$F, $C_{dm} = 470\mu$F, $R_{dm} = 5\Omega$, $f_{tg} = 10$kHz

2.4 Hybrid PWM Control Technique

Conventional ZSI PWM has inherent shoot-through state but has higher switching losses [[106]-[110]. The power interval and shoot-through interval are required in every switching cycle for simultaneous ac and dc output. The hybrid PWM techniques have less switching losses and also have inherent shoot-through ability [83]-[84].

Fig. 2.7 (a) shows the model of the PWM logic circuit for the proposed hybrid inverter. In this analog model, V_{ref} and $-V_{ref}$ are the reference sinusoidal signals of 50 Hz frequency whereas V_{mref} and $-V_{mref}$ are the peak values of reference sinusoidal waveforms. Both the sinusoidal voltages are equal in magnitude and frequency but are out of phase by 180^0. A carrier triangular frequency waveform is mentioned as V_{tc} with a peak value of $V_{ptc.}$ Two shoot-through voltages are used for the generating shoot-through pulses. Both shoot-through voltages (V_{sth} *and* $-V_{sth}$) are equal in magnitude. Four OR gates, two AND gates and one NAND gate are used to design analog model of hybrid PWM generation. The genearation of control signals for $V_{ref}>0$ and $V_{ref}<0$ are shown in Figs. 2.7 (b) and (c), respectively.

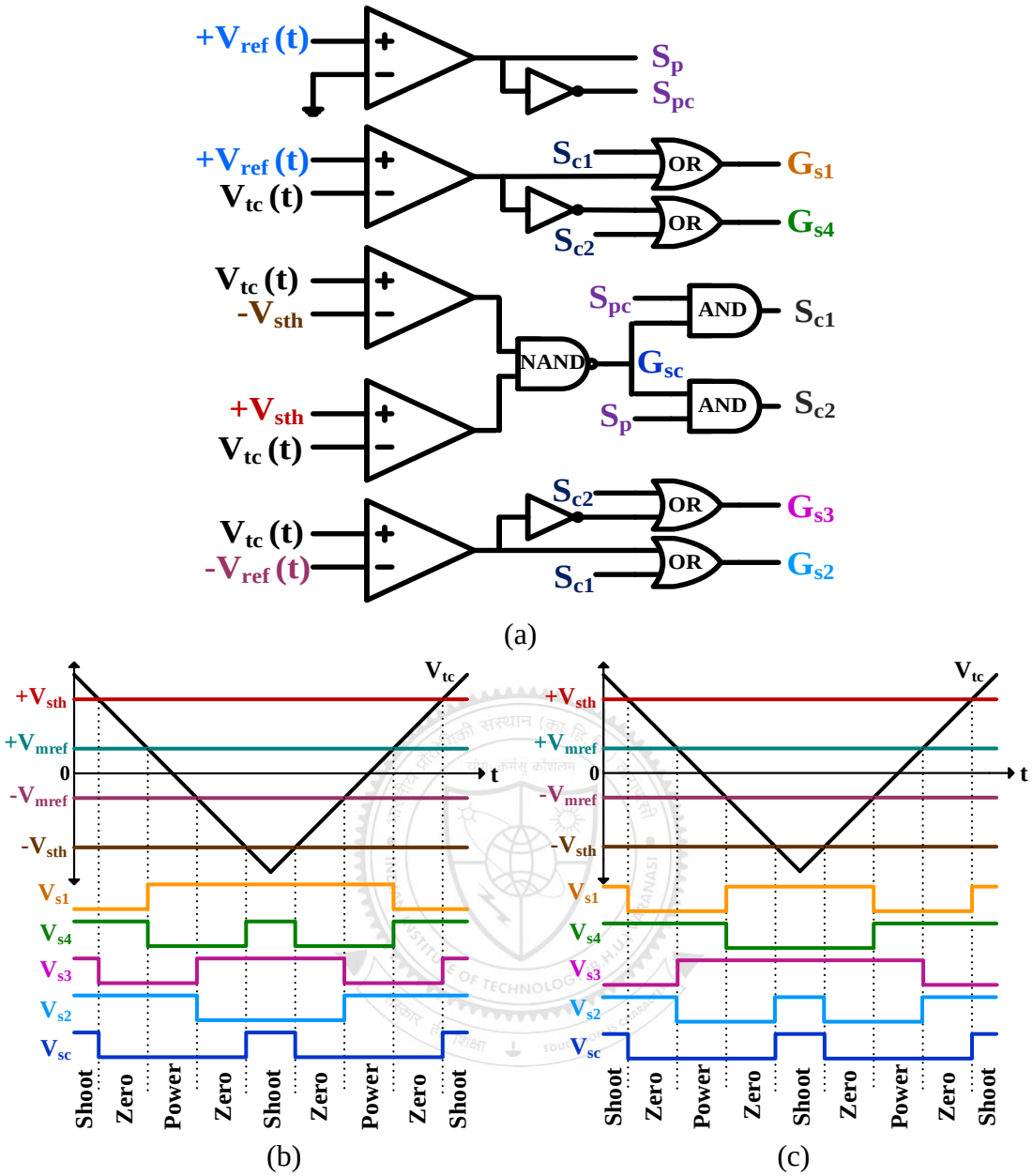


Fig. 2.7. PWM logic for proposed hybrid inverter (a) analog model of PWM logic, (b) generation of control signals when $V_{ref} > 0$, (c) generation of control signals when $V_{ref} < 0$.

TABLE 2.2
CONDUCTING SWITCHES IN DIFFERENT STATES

Switching States	$V_{ref} > 0$	$V_{ref} < 0$
	Conducting Switches	
Shoot-Through	$G_{s3}G_{s2}G_{s4}G_{sc}$ $G_{s1}G_{s4}G_{s3}G_{sc}$	$G_{s1}G_{s4}G_{s2}G_{sc}$ $G_{s3}G_{s2}G_{s1}G_{sc}$
Power	$G_{s1}G_{s2}$	$G_{s3}G_{s4}$
Zero	$G_{s4}G_{s2}$ $G_{s1}G_{s3}$	$G_{s4}G_{s2}$ $G_{s1}G_{s3}$

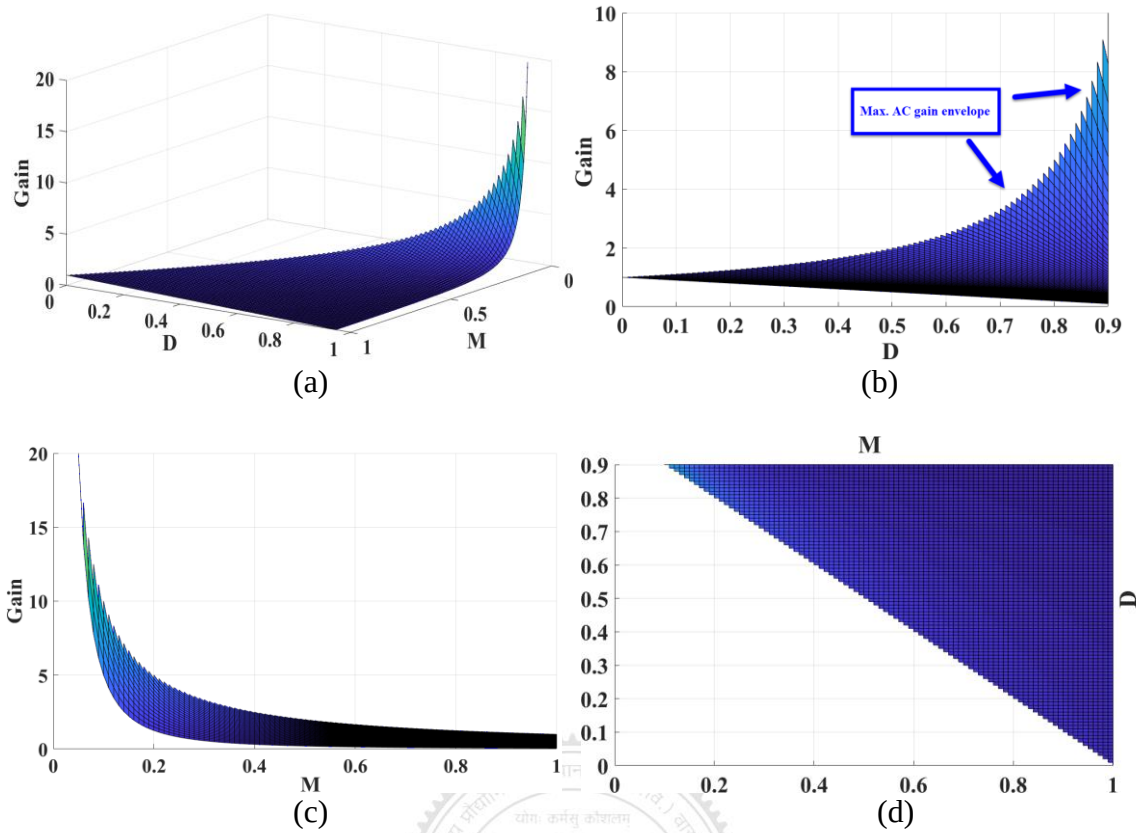


Fig. 2.8. Analysis of proposed hybrid inverter (a) Variation of ac voltage gain with modulation index (M) and shoot-through duty cycle (D), (b) ac voltage gain with shoot-through duty cycle (D), (c) ac voltage gain with modulation index (M), (d) Operating region for M and D.

The conducting switches of proposed hybrid inverter for different references during shoot-through, power and zero intervals are listed in Table 2.2. In one switching interval of triangular carrier waveform, the shoot-through interval occurs twice in alternative legs. During power interval, the switches $G_{s1,}G_{s2}$ will operate for $V_{ref} > 0$ whereas $G_{s3,}G_{s4}$ will operate for $V_{ref} < 0$. Therefore, both D and M are responsible for simultaneous ac and dc operation. The PWM control technique constraints will lead to the following inequality.

$$D + M < 1$$

The maximum ac output voltage will be obtained when $M = 1 - D$. Fig. 2.8 gives three dimensional plots of the change in the voltage gain with respect to different values of D and M for the proposed hybrid inverter.

2.5 Simulation Studies

Simulation studies are performed in order to test the performance of the proposed inverter. The parameters with their attributes are listed in the Table 2.3.

TABLE 2.3
LISTS OF PARAMETERS WITH THEIR ATTRIBUTES FOR HIGH GAIN INVERTER

Prototype Specification	
Parameters	**Attributes**
Coupled Inductor	L_1 = 1.8 mH, L_2 =2.5 mH
Coefficient of Coupling	k = 0.929
Damping Network	$C_{dm,}$= 470 µF, R_{dm} = 5 Ω
Capacitance	C_1 =100 µF, C_2 =200 µF
Carrier Frequency	f_{tg}=10 kHz
Fundamental Frequency	50 Hz

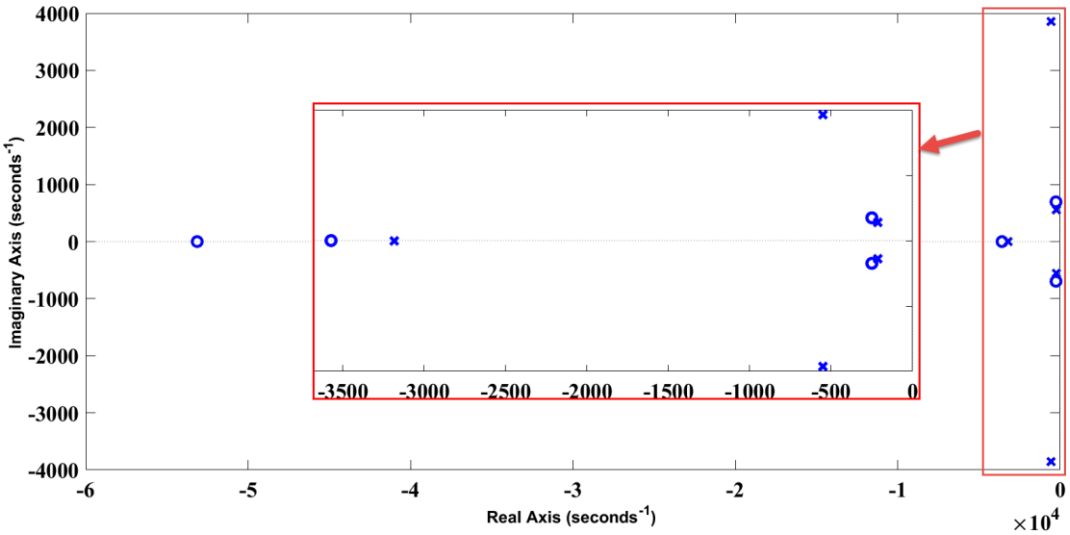


Fig. 2.9. Pole-zero plot of control to output transfer function for the proposed hybrid inverter.

2.5.1 Minimum Phase Property of Proposed Hybrid Inverter

The pole zero plot of the proposed hybrid inverter is shown in Fig. 2.9 for the parameters shown in Table 2.3. It can be observed from Fig. 2.9 that the proposed hybrid inverter has total four zeros and five poles out of which two real zero, one real pole, one complex zero pair and two complex pole pairs in control-to-output transfer function as shown in Fig. 2.9. Further, it is also evident from the Fig. 2.9 that all the zeros exist in the left half of plane. Thus, Fig. 2.9 verifies that the hybrid inverter does

not display any RHPZ in the control-to-output transfer function thereby giving a minimum phase system.

Fig. 2.10 shows the variation in the location of the poles and zeros by varying the different parameters such as coefficient of coupling *k*, duty ratio *D* and load resistances. Fig. 2.10 (a) shows that when *k* is varied from 0.232 to 0.929 the locations of poles and zero changes but the location of complex zero is not much affected. It can be observed from Fig. 2.10 (a) that all the zeros exist in the left half plane. Fig. 2.10 (b) shows the pole zero location by keeping k=0.929 and varying the L_1 from 1mH to 2.5 mH along with change in L_2 from 1.5 mH to 3 mH and keeping others parameters constants. It is evident from Fig. 2.10 (b) that by increasing the values of inductors (L_1 and L_2), the zeros shifts towards origin and complex zeros are modulated towards the origin. Pole zero locations with the change in shoot-through duty cycle (D) from 0.4 to 0.7 keeping other parameters constants is also investigated. From Fig. 2.10 (c), it is clear that zeros are shifting towards origin when D are increased from 0.4 to 0.7. It is also verified from Fig. 2.10 (c) that all the zeros appear in the left half plane up to D = 0.7. Thus, up to D = 0.7 there is no RHPZ in the proposed hybrid inverter. Fig. 2.10 (d) shows change in the locations of poles and zeros with the variations in the loads. AC load is changed by varying its load resistance from 20 Ω to 5 Ω and DC load resistance changes with 200 Ω to 50 Ω. The analysis shown in Fig. 2.10 (d) confirms that the zeros in light load, as well as for high load, do not get much affected. Result shown in Fig. 2.9 and Figs 2.10 (a), (b), (c) and (d) confirm that the proposed hybrid inverter does not display any RHPZ and therefore, it gives a minimum phase system. It is also verified from results in the Fig. 2.10 that the zeros lie down in the left half plane irrespective of the changes in the different parameters such as coefficient of coupling *k*, duty ratio *D* and load resistances. This confirms rugged minimum phase behavior of the proposed inverter.

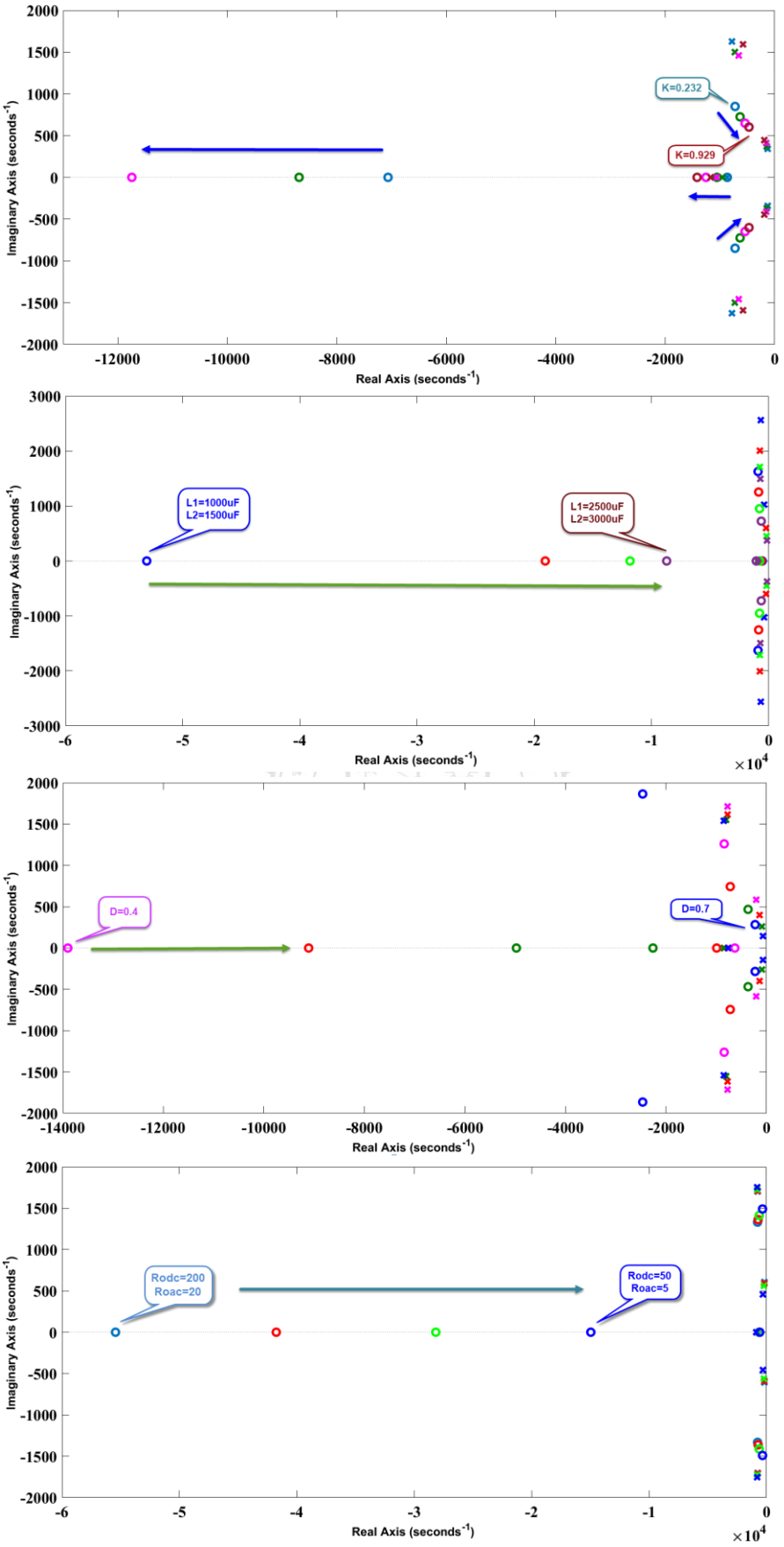
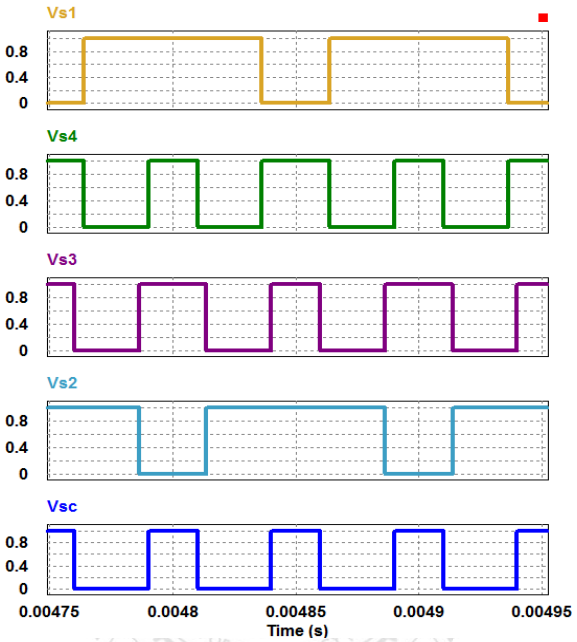


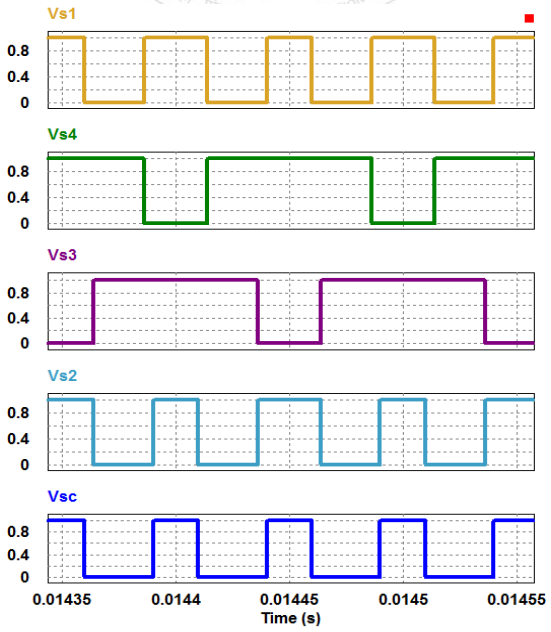
Fig. 2.10. Verification of RHPZ (a) effect of k, (b) effect of coupled inductances, (c) effect of D, (d) effect of loads R_{odc} and R_{oac}.

2.5.2 PWM for High Gain Inverter

Figs. 2.11 (a) and (b) shows the simulation results of the gating signal given to the switches of the proposed hybrid inverter when $V_{ref} > 0$ and $V_{ref} < 0$, respectively. The PWM waveform is validated for $D = 0.4$ and $M = 0.5$. The PWM waveform shows that for each reference voltages the shoot-through is inserted in each leg.

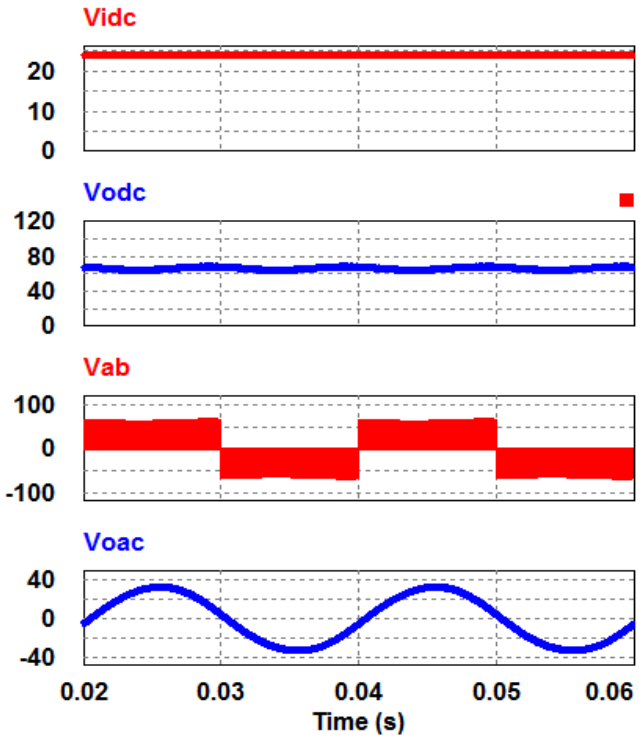


(a)

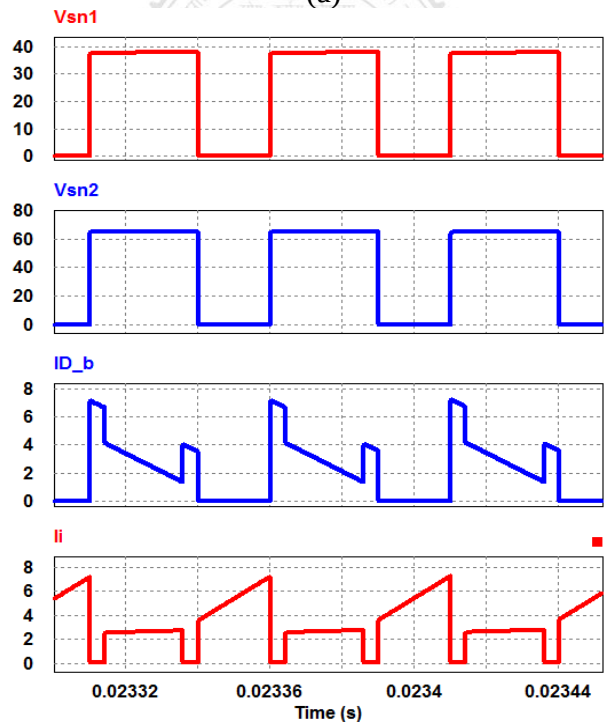


(b)

Fig. 2.11 Simulation verification of PWM for the proposed hybrid inverter (a) when $V_{ref} > 0$, (b) when $V_{ref} < 0$.



(a)



(b)

Fig. 2.12. Simulation validation for proposed hybrid inverter for duty ratio D = 0.4 and modulation index M = 0.5 (a) steady state operation results, (b) switching waveforms.

2.5.3 Steady-State Operation

The proposed hybrid inverter is verified through simulation on a 200 W prototype and the results are shown in Figs. 2.12. Fig. 2.12 (a) shows the steady state simulation verification of the proposed hybrid inverter for input voltage V_{idc} =24 V. It can be seen from Fig. 2.12 (a) that for V_{idc} =24 V proposed hybrid inverter gives dc output voltage V_{odc}= 66.6V and the AC output voltage V_{oac}= 65.2V (peak-peak) for duty ratio D = 0.4 and modulation index M = 0.5. Switching waveforms V_{sn1}, V_{sn2}, I_{Db}, and I_i for the same D and M are shown in Fig. 2.12 (b). Thus, results in Figs. 2.12 confirm that the proposed high gain inverter gives high gain in less duty cycle and have ability to operate in wide duty cycle. It is important to mention that for single-phase system, both high frequency ripples as well as low frequency ripples (double line frequency) are present. This characteristic is appearing due to low frequency component existing in the current drawn by the single -phase inverter bridge as shown in Fig. 2.12 and Fig. 2.13.

2.5.4 Duty Cycle Variation

The proposed minimum phase high gain inverter is also validated with sudden shoot-through cycle variation. The performance of duty cycle variation is observed in both the ac and dc loads. The shoot-through duty cycle is suddenly varied from D = 0.4 to D = 0.5 and vice-versa as shown in Fig. 2.13. During duty cycle variation, the modulation index (M) is kept constant as 0.5. From Fig. 2.13(a), it is clear that during step-up change in duty cycle, the dc output voltage changes from 66.6V to 96V and ac output voltage changes from 65.2V (peak-peak) to 88V (peak-peak) smoothly. Also, from the Fig. 2.13(b), it is clear that during step-down change in duty cycle, dc output voltage changes from 96V to 66.6V and ac output voltage changes from 88V (peak-peak) to 65.2V (peak-peak) smoothly. From Fig. 2.13 it is clear that during the step-up duty cycle change, the dip in the output voltage is not observed as compared to the

conventional non-minimum phase boost derived converters. Hence, the RHP zero is completely eliminated from the proposed converter.

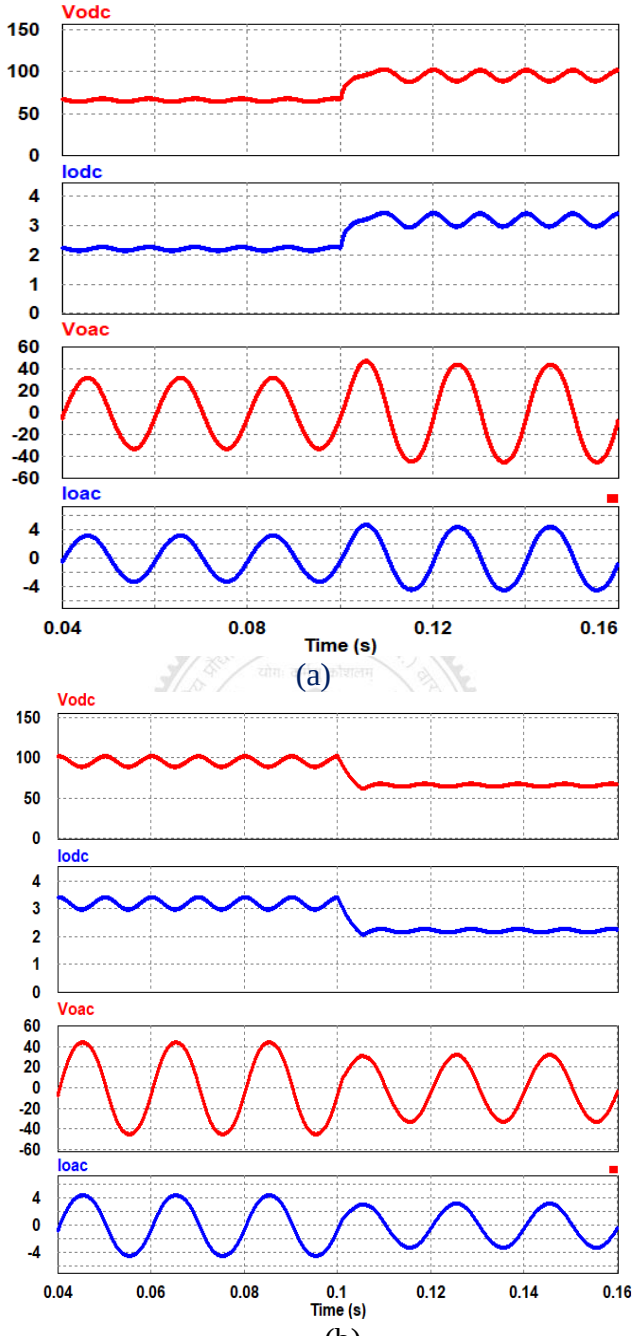


Fig. 2.13. Duty cycle variation of proposed hybrid inverter (a) Step-up shoot-through duty cycle variation, (b) Step-down shoot-through duty cycle variation.

2.6 Conclusion

A high gain minimum phase quadratic boost hybrid inverter which is having no RHPZ is presented. The high gain hybrid inverter is developed by coupling the filter inductors

of a quadratic boost converter with an insertion of damping network in the circuit and replacing load side main switch of the quadratic boost converter by the H-bridge inverter. By doing so, the proposed inverter is capable of giving simultaneous ac and dc output with no RHPZ. The no RHPZ property is verified using pole and zero plots with variation in different parameters. Due to the quadratic behaviour of the proposed hybrid converter, high gain is achieved on low operating shoot-through duty cycle. Simulation studies are performed to test the performance of the proposed inverter.