Chapter 8

Non-Zero DCM in Buck-Boost Derived Hybrid Converter

8.1 Introduction

For both DC and AC output, recently reported topologies derived from Z-source converter have special feature of multipurpose usage i.e. standalone AC/DC output or simultaneous AC and DC output. Though various topologies discussed earlier may be modified as hybrid output converter, they have some limitations. The Z-source hybrid converter usually becomes unstable in case of DC load, if there is unbalanced effective load appearing across the two capacitors. The SBI [51], due to presence of single capacitor, has no instability problem. To reduce the number of elements in boosting network of ZSI, boost derived hybrid converter (BDHC) is proposed as a potential candidate [131]. Likewise, the current fed switched inverter for hybrid output is presented in [130], which has higher gain as compared to SBI and BDHC. One common aspect about all the above mentioned hybrid converters is the inherent creation of higher dc output voltage than input, while Buck-Boost operation at the inverter end. Few of the applications such as mobile phone, Laptop chargers, LEDs etc. require DC output voltage lower than the input. The concept of buck and boost operation at the DC terminal is also appropriate for motor drive [137], [138]. To fill up the gap, here a Buck-Boost hybrid converter(BBDHC) which has the capability of Buck-Boost DC output voltage along with buck operation of AC output voltage. This chapter also analyses the effects and mitigation of NZ-DCM in the proposed BBDHC. From the analytical study, it is proven that converter does not operates satisfactorily

during NZ-DCM. In addition, standalone AC operation is not possible in BBDHC. These limitations of BBDHC addressed in this chapter and their corresponding remedy is also given so that proposed converter can be applied for wide variation of load change and in standalone AC operation. In addition to these, MBBDHC is modeled by state space averaging technique and its closed loop control is designed. The performance of the closed loop MBBDHC is evaluated under transient load and reference input variations.

The major contribution of this chapter is to propose and validate a Buck-Boost derived hybrid converter(BBDHC) and its modification with their control strategies. For proof of concept, open loop study is presented in this chapter. Modified Buck-Boost derived hybrid converter(MBBDHC) converter in totality has the following advantages:

1) Buck-Boost operation is possible at DC terminal.

2) Immune to EMI.

3) No dead time is required.

4) Positive Buck-Boost output DC voltage.

5) Single stage conversion.

6) Standalone DC operation.

7) Standalone AC operation.

8.2 Evolution of MBBDHC

Evolution of the proposed converter started with the analysis of non inverting Buck-Boost converter(NIBBC) reported in 2004 [139]. The NIBBC is used for the Step-up/Step-down the DC input voltage. Though NIBBC has discontinuous input current, this can be avoided by using input filter [140]. The NIBBC is comprised of two active switches, two passive switch and one set of inductor and capacitor as shown in Fig-8.1a. The purpose of having two switches, unlike the conventional Buck-Boost converter, is to make output positive. Moreover, NIBBC offers the advantage of common ground as compared to the conventional Buck-Boost converter. However, NIBBC is useful for DC application. To make it acceptable for AC application, NIBBC is cascaded with the inverter. This restricts its use only in AC application. To produce both DC and AC output from the same converter a hybrid cascaded Buck-Boost converter can be used. Though this converter can supply the DC and AC load simultaneously, it has few drawbacks: 1) Double stage

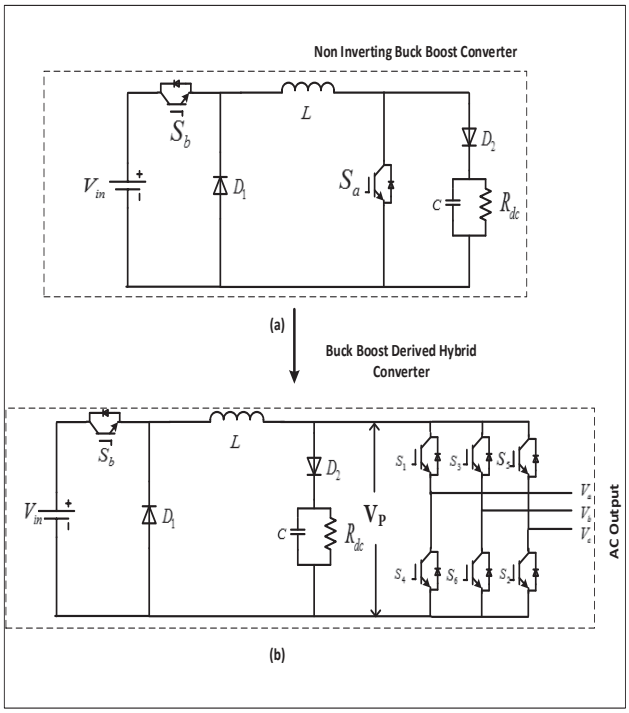


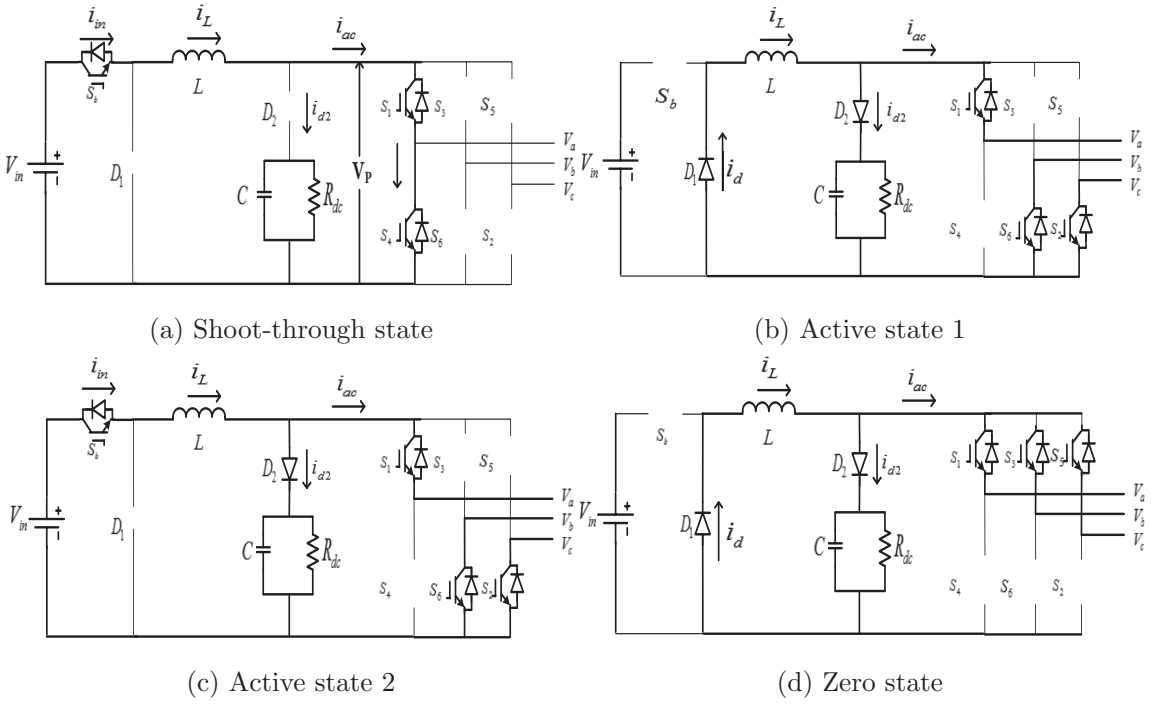
Figure 8.1: Evolution of Buck-Boost derived hybrid converter

conversion 2) One Extra switch is used for boost operation of the converter. 3) Inverter subjected to EMI problem which causes sudden short circuit of source voltage. This over stresses the power electronic devices. 4) Require dead time in between the switches of the same leg to avoid false triggering of the switches which further requires complex circuitry for dead time compensation [49].

The proposed Buck-Boost derived hybrid converter (BBDHC), is shown in Fig-8.1b. This mitigate the limitation of the hybrid cascaded Buck-Boost converter. The proposed BBDHC is obtained by replacing the Switch S_a with a single/three phase inverter. In this paper, three phase AC load is considered. The modified converter(MBBDHC) can serve as Buck-Boost DC and Buck AC converter, and supply simultaneous AC and DC load.

8.2.1 Operation of MBBDHC

Although for BBDHC, three operating modes exist - Buck , Boost and Buck-Boost, but in this chapter only Buck-Boost mode is considered. During Buck-Boost operation, the switch S_1 and S_4 are turned ON and OFF, simultaneously. Charging of the inductor takes place through switches while discharging through the diode. To charge the inductor, the



(a) Shoot-through state

(b) Active state 1

(c) Active state 2

(d) Zero state

Figure 8.2: Operating modes:Buck-Boost derived hybrid converter

two switches of the same leg, from any of the three leg of the inverter, need to be turned ON at the same time. Four states are present during its operation.

Shoot-through state

Shoot-through is characterized by turning ON both the switches of the same leg simultaneously, as shown in Fig-8.2a. The gate signals are set such that a short-circuit path is created through the inverter leg. Concurrently, the switch S_b is also turned ON to charge the inductor through the short-circuit path. This turns OFF the diode D_2 disconnecting the DC load from the supply.

Active State 1

During this state, shoot-through is removed and switch S_b is turned OFF. This brings inverter into its normal operation. The inductor changes its polarity to discharge letting the diode D_1 forward biased. During this period inductor current acquire path of DC and AC load through diode D_1. In this period the input source is isolated from the load, as shown in Fig-8.2b.

Active state 2

During this period, shown in Fig-8.2c, the switch S_b is turned ON, the source feeds both DC and AC load. If S_b remains turned ON till the next shoot-through pulse, it behaves as a boost converter. For achieving Buck-Boost operation, the duty cycle of S_b should be less than the active period of the inverter.

Zero state

During zero state, the AC load is isolated from the Buck-Boost circuit and only DC load is served. In this state either upper half or lower half of the inverter switch is turned ON simultaneously as shown in Fig-8.2d.

8.2.2 Steady state analysis

For steady state analysis, it is assumed that diodes and switches have zero forward voltage drop. Also, the various elements including power devices, inductor and capacitor are lossless. Inductor current and voltage profile are indicated in Fig-8.3. During charging of the inductor, the voltage across the inductor is

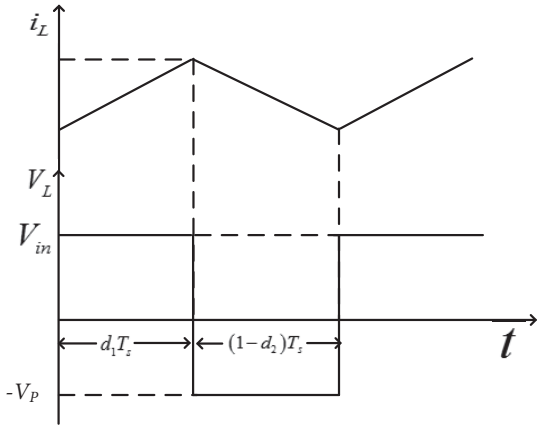


Figure 8.3: Inductor current and voltage profile

$$V_L = V_{in} \tag{8.1}$$

and for the freewheeling period

$$V_L = -V_P \tag{8.2}$$

Averaging over a duty cycle, the inductor voltage is zero; so

$$\begin{aligned} & d_1 V_{in} + (1 - d_2)(-V_P) = 0 \\ & i.e.\ V_P = \tfrac{d_1}{1-d_2} V_{in} \\ & i.e.\ V_P = G_{DC} V_{in} \end{aligned} \tag{8.3}$$

where d_1 is duty cycle of switch S_b and d_2 corresponds to shoot-through period. The duty cycle d_1 and d_2 can be varied in the range $0 < d_1, d_2 < 1$. The variation in duty cycle is given as

$$\begin{aligned} & d_1 > d_2 \ for\ Boost\ operation \\ & d_1 = d_2 \ for\ Buck - Boost\ operation \end{aligned} \tag{8.4}$$

As in this chapter only Buck-Boost operation is taken into consideration so d_1=d_2 is always taken and used vice-versa.

For AC gain of the converter, the input to the inverter is DC link voltage(V_P), rather than the input source voltage(V_{in}). The inverter is supplied by the boosted voltage and its operation is governed by modulation index(m) as per the load requirement. The three phase peak inverter output voltage for conventional VSI is

$$v_{ac} = \frac{m V_{in}}{2} \tag{8.5}$$

For the proposed converter it gets modified to

$$v_{ac} = \frac{m d_1}{2(1 - d_2)} V_{in} i.e.\ v_{ac} = G_{AC} V_{in} \tag{8.6}$$

where m can vary in the range $0 < m < 1$. The magnitude of the output is governed by their respective controlling variables i.e., the DC output is decided by the duty cycles, while inverter output depends both on duty cycles and modulation index. This condition is defined as

$$\begin{aligned} & V_P = f(d_1, d_2) \\ & v_{ac} = f(d_1, d_2, m) \end{aligned} \tag{8.7}$$

Though, this converter has the flexibility of controlling the modulation index and duty cycle independently, the range is restricted. This is defined as

$$m + d_2 \leq 1 \tag{8.8}$$

The plot for DC gain for fixed modulation index equal to zero is shown in Fig-8.4. DC gain is reduced when modulation index is increased to satisfy Equ-(8.8). AC gain of

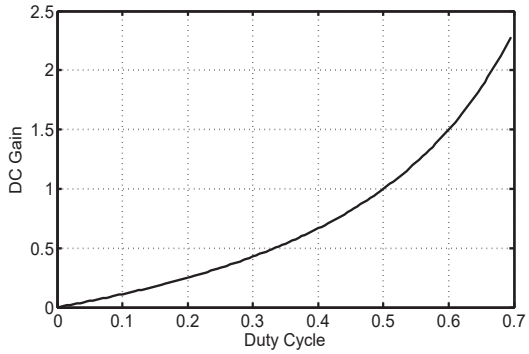


Figure 8.4: DC gain of the converter for m=1

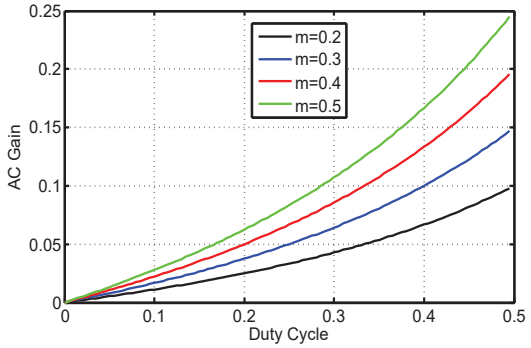


Figure 8.5: AC gain of the converter for duty cycle < 0.5

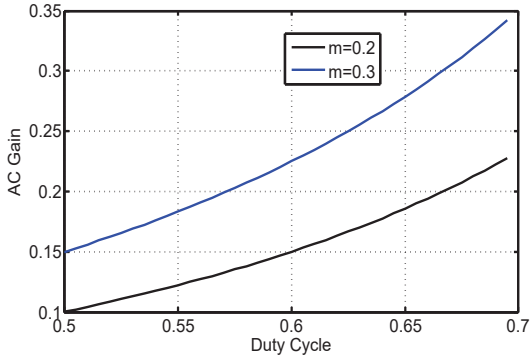


Figure 8.6: AC gain of the converter for duty cycle > 0.5

the converter for duty cycle less than 0.5 and greater than 0.5 is shown in Fig-8.5 and Fig-8.6, respectively. Similar to DC gain, Equ-(8.8) is satisfied for calculating the AC gain.

The DC power in terms of the DC load resistance (R_{dc}) is given as

$$P_{dc} = \frac{{d_1}^2 {V_{in}}^2}{(1-d_2)^2 R_{dc}} \tag{8.9}$$

and AC power equation in terms of AC load resistance (R_{ac}), where R_{ac} is per phase resistance, is given as

$$P_{ac} = \frac{m^2 {d_1}^2 {V_{in}}^2}{4(1-d_2)^2 R_{ac}} \tag{8.10}$$

8.3 Condition for NZ-DCM and effects

The two modes CCM and NZ-DCM of the proposed converter are recognized in terms of the inductor current. If the initial value of current reaches zero before the end of OFF period then converter enters into DCM condition. To avoid this DCM, the inductor is designed to have sufficient value. However, under high load condition, DCM also occurs with non-zero inductor current. The NZ-DCM is observed when inductor current saturates at AC load current, due to which DC link voltage is distorted as indicated in Fig-8.8b.

During the charging period of the inductor, the input current

$$I_{in} = I_L \tag{8.11}$$

while for discharging period, the input current

$$I_{in} = 0 \tag{8.12}$$

Average input current over a complete cycle is given by

$$I_{in} = d_2 I_L \tag{8.13}$$

From power balance theory, the input DC power must be equal to summation of DC and AC output power delivered.

$$V_{in} I_{in} = V_{dc} I_{dc} + 3 V_{ac} I_{ac} \cos\varphi \tag{8.14}$$

From equ.-(8.13), (8.14) translates into

$$I_L = \frac{V_{dc} I_{dc} + 3 V_{ac} I_{ac} \cos\varphi}{d_2 V_{in}} \tag{8.15}$$

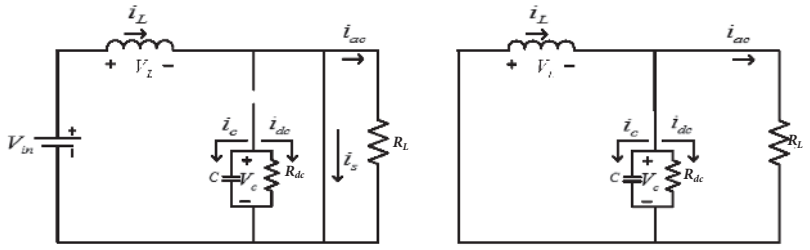


Figure 8.7: Equivalent circuit for BBDHC

For CCM, the diode (D_2) present in the load path must conduct all the time. To ensure this, the current in the inductor must be greater than the sum of AC and DC load current, or voltage across the diode (ideal) must be greater than zero i.e. from Fig-8.7;

$$V_{d2} > 0$$
$$i_L > i_{d2} + i_{ac}$$
$$i_L - i_{ac} > 0$$

where i_L and i_{ac} are instantaneous quantity. Replacing i_L in terms of peak to peak ripple(ΔI_L) and average value(I_L) of inductor current, results in

$$I_L - \frac{\Delta I_L}{2} - i_{ac} > 0 \tag{8.16}$$

From Equ.-(8.15), this condition results in

$$I_{dc} = C_L > \sqrt{2}(1-d_2)I_{ac} - \frac{3M}{2\sqrt{2}} I_{ac}\cos\phi + \frac{d_2(1-d_2)V_{in}}{2f_sL} = C_R \tag{8.17}$$

All the values of current and voltage are in rms. Any variation in the constant terms C_L and C_R that violates the above condition results in NZ-DCM. For e.g., the term C_R is completely dependent on shoot-through duty cycle. In case of high load condition, the inductor current saturates at AC load current. Hence constant inductor current for a small period results in inductor voltage

$$V_L = L\frac{di_L}{dt} = 0$$

Applying KVL during discharging period

$$V_L + V_{d2} + V_c + V_{D1} = 0 \tag{8.18}$$

Since V_L is zero, the voltage across the diode D_2, $V_{d2} = -V_c - V_{D1}$. The diode(D_2) gets reverse biased and does not satisfy the condition for CCM. This brings the converter into

NZ-DCM. The profile of inductor current and DC link voltage is shown in Fig-8.8b. The inductor current is saturated at AC load current. The diode D_2 becomes reverse biased i.e diode current become zero. Although the converter works under NZ-DCM, but it injects high voltage ripples in DC and AC output voltages.

For standalone AC operation, the condition for the continuous operation of converter becomes invalid because of zero DC current. This reverse biases the diode(D_2), resulting in inadvertent operation. These two issues are addressed in the next section.

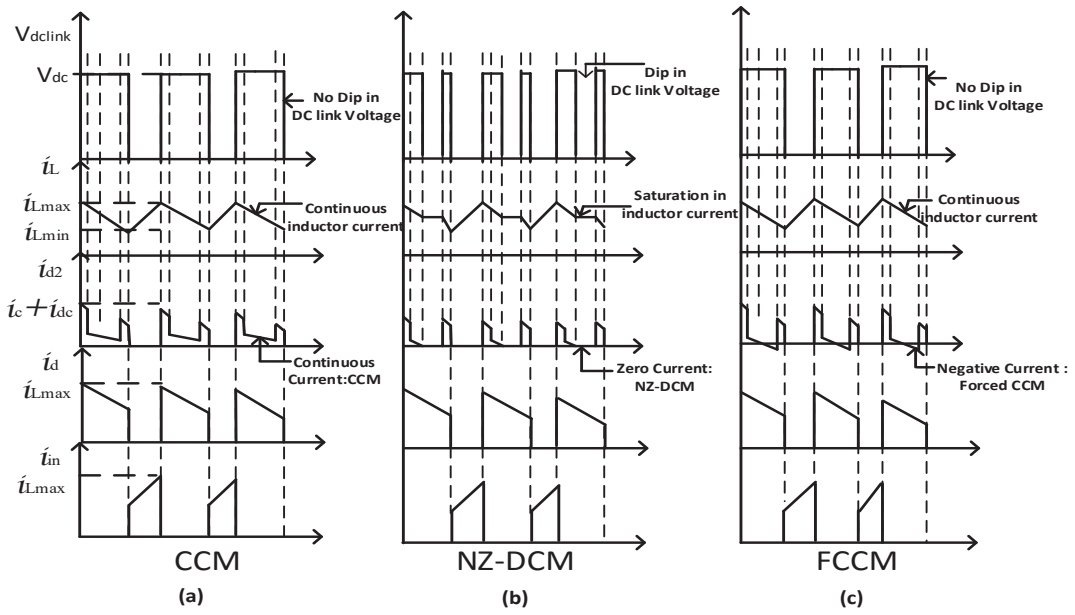


Figure 8.8: Operating modes of BBDHC/MBBDHC

8.4 NZ-DCM mitigation: Modified BBDHC

To overcome the issues of ripple injection in DC link voltage, an alternative path is provided to supply extra current to the load, through the capacitor. This mode is known as forced continuous current mode (FCCM). During FCCM, capacitor current is directed towards the AC load apart from DC load. For this, a switch antiparallel across the diode is placed. In addition to the operating states of BBDHC discussed in section 8.2, the modified version consist of an extra state-FCCM, which would appear during NZ-DCM and standalone AC operation. Fig-8.9 shows the Modified BBDHC in which an antiparallel switch is placed with the diode. As the DCM or standalone AC operation is

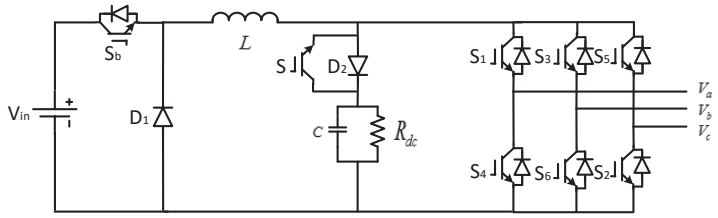


Figure 8.9: Modified Buck-Boost derived hybrid converter

about to happen, the switch S comes in picture, letting the current to flow in opposite direction. During FCCM, the switch S in MBBDHC is controlled by the complemented shoot-through pulses(NST shown in Fig-8.12). Under NZ-DCM, the switch S turns ON and allows the current to flow through it. The capacitor supply its energy to the DC link, suppressing the ripple voltage. Similarly, during AC standalone operation the antiparallel switch conducts and stabilizes the standalone operation. Fig-8.8c indicates the FCCM operation which has no dip in DC link voltage, triangular inductor current and negative diode current. Therefore, the modified BBDHC has potential to supply AC or DC and simultaneous AC and DC load. Though extra switch is required in MBBDHC, but it is only required in wide load variation else with reduced number of switches BBDHC operate satisfactorily if load variation is restricted.

8.5 Design of MBBDHC controller

8.5.1 DC voltage controller

For DC voltage controller design, inverter with AC load is assumed equivalent to resistance R_L. During ST, the DC capacitor is supplying the power to DC load and inductor is charging through inverter leg. During NST, the DC and AC are supplied by the source along with inductor. State space averaging technique is considered for modeling of Buck-Boost converter.

During ST, state equations are given as

$$\begin{aligned} V_L &= L\frac{di_L}{dt} = V_{in} \\ C\frac{dV_c}{dt} &= -\frac{V_c}{R_{dc}} \end{aligned} \tag{8.19}$$

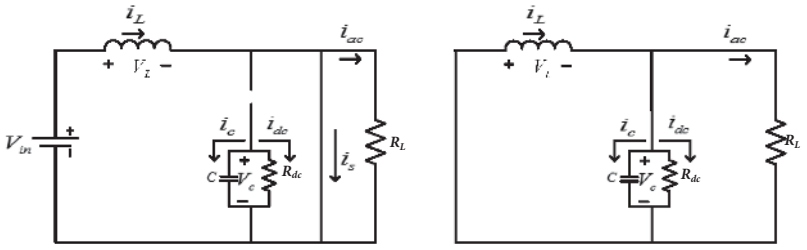


Figure 8.10: Equivalent circuit for DC loop a) ST state b) NST state

During NST, state equations are given as

$$\begin{aligned} L\frac{di_L}{dt} &= -V_c \\ C\frac{dV_c}{dt} &= i_L - \frac{V_c}{R_L} \end{aligned} \tag{8.20}$$

$$\begin{aligned} \frac{di_L}{dt} &= \frac{dV_{in}}{L} - \frac{(1-d)V_c}{L} \\ \frac{dV_c}{dt} &= -\frac{dV_c}{R_{dc}C} + \frac{(1-d)}{C}\left[i_L - \frac{V_c}{R_L}\right] \end{aligned} \tag{8.21}$$

$$V_{dc} = V_c \tag{8.22}$$

In state space form, Equ-(8.21) and Equ-(8.22) are written as

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \tag{8.23}$$

where $x = [i_L \quad V_c]^T$, $u = [V_{in} \quad 0]^T$ and $y = V_{dc}$. After perturbing the control variables around their steady state operating point as

$$\begin{cases} \langle v_{in}(t)\rangle_{Ts} = V_{in} + \hat{v}_{in} \\ \langle v_c(t)\rangle_{Ts} = V_C + \hat{v}_c \\ \langle i_L(t)\rangle_{Ts} = I_L + \hat{i}_L \\ d(t) = D + \hat{d} \end{cases} \tag{8.24}$$

Equ-(8.23) is given as

$$\begin{aligned} \frac{d\hat{i}_L}{dt} &= \frac{1}{L}\left[-\hat{v}_c(1-d) + \hat{v}_{in}d + (V_{in}+V_c)\hat{d}\right] \\ \frac{d\hat{v}_c}{dt} &= \frac{1}{C}\left[\hat{i}_L(1-d) - \hat{v}_c\left(\frac{d}{R_{dc}} + \frac{1-d}{R_L}\right) - \hat{d}\left(\frac{V_c}{R_{dc}} + I_L - \frac{V_c}{R_L}\right)\right] \end{aligned} \tag{8.25}$$

After setting the value of $\hat{v}_{in} = 0$ and $\hat{i}_L = 0$ and solving the above equation, control to output transfer function is given as

$$\frac{\hat{v}_c}{\hat{d}} = \frac{V_i\left(R_{dc} - \frac{D}{(1-D)^2}Ls\right)}{(CLR_{dc})\,s^2 + \left[\frac{R_{dc}}{R_L}(1-D)+1\right]Ls + (1-D)^2R_{dc}} \tag{8.26}$$

To make system stable in closed loop, a type III compensator is designed. The gain margin and phase margin for the system are considered 20 dB and 60° respectively. The designed compensator is given by

$$G_c(s) = \frac{16e^{-10}s^2 + 9e^{-5}s + 1}{3.37e^{-7}s^3 + 3e^{-3}s^2 + s} \tag{8.27}$$

8.5.2 AC voltage controller

In order to ensure better performance in terms of steady state error and transient performance, decoupled control method based on synchronous reference frame or d-q theory is considered. To design AC voltage controller, transfer function of the AC load is required. For transfer function calculation, the equivalent circuit for AC load on per phase basis is shown in Fig-8.11.

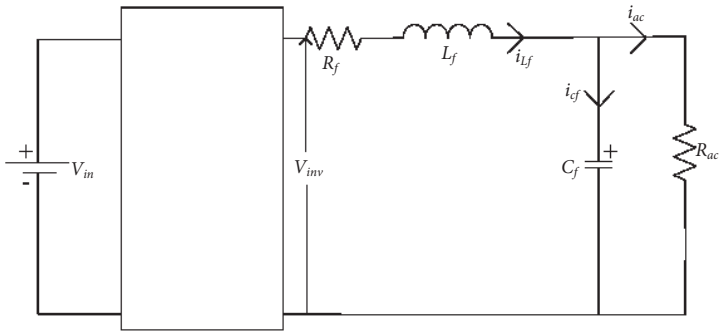


Figure 8.11: Equivalent circuit for AC load

The dynamics is given as

$$\frac{di_{Lf}}{dt} = \frac{R_f}{L_f} i_{Lf} + \frac{1}{L_f}(V_{inv} - V_{ac}) \tag{8.28}$$

$$\frac{dV_{ac}}{dt} = \frac{1}{C_f} i_{Lf} - \frac{V_{ac}}{R_{ac}C_f} \tag{8.29}$$

These quantities are non linear in nature. To make them linear, *d-q* transformation is performed on Equ-(8.28) and Equ-(8.29), which are transformed to

$$\begin{bmatrix} \dot{I}_d \\ \dot{I}_q \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & \omega \\ -\omega & -\frac{R_f}{L_f} \end{bmatrix} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} V_{inv} - V_d \\ V_{inv} - V_q \end{bmatrix} \tag{8.30}$$

$$\begin{bmatrix} \dot{V}_d \\ \dot{V}_q \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_{ac}C_f} & \omega \\ -\omega & -\frac{1}{R_{ac}C_f} \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{8.31}$$

Laplace transformation of the above equations become

$$\frac{I_d}{\chi_{id}(s)} = \frac{I_q}{\chi_{iq}(s)} = \frac{1}{sL_f + R_f} \tag{8.32}$$

$$\frac{V_d}{\chi_{Vd}} = \frac{V_q}{\chi_{Vq}} = \frac{R_{ac}}{sR_{ac}C_f + L} \tag{8.33}$$

where,

$\chi_{id}(s) = V_{inv} - V_d + \omega L_f I_q$, $\chi_{Vd}(s) = I_d + \omega C_f V_q$

$\chi_{iq}(s) = V_{inv} - V_q - \omega L_f I_d$, $\chi_{Vq}(s) = I_q - \omega C_f V_d$

Equ-(8.32) and Equ-(8.33) represent the open loop transfer function for current and voltage loop respectively. Similar to DC loop, to stabilize the AC controller, compensators for voltage and current loop are required. PI controllers are designed to serve the purpose. For voltage controller, P=3, I=1604 while for current controller, P=0.46 and I=1604 are considered to achieve 60° PM.

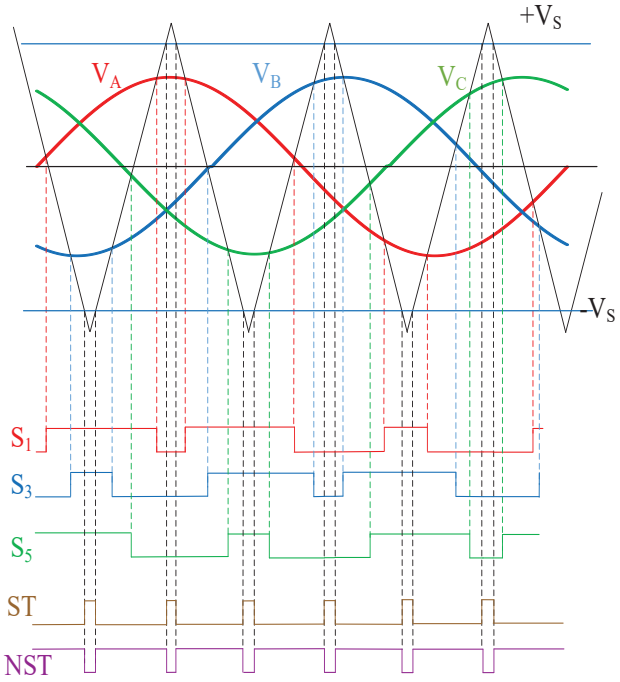


Figure 8.12: Control of proposed converter

8.6 Control of proposed converter

The control strategy of proposed hybrid converter is different than cascaded Buck-Boost inverter. This control method is derived from the control method applied to Z-source inverter. For controlling the Z-source inverter, several modulation strategies like constant boost control, maximum boost control, modified SVPWM and simple boost control are available. However, except simple boost control, other schemes cannot meet independent control requirement of hybrid converter. Therefore, a simple boost strategy is chosen by authors. In this scheme, three sinusoidal pulses (V_A, V_B, V_C) shifted by 120° from each other are compared to triangular carrier wave as shown in Fig-8.12. The generated pulses S_1, S_3, S_5 have active states and zero states. The modulation index of the converter is controlled by varying the magnitude of the sinusoidal waveform. To achieve the Buck-Boost operation using inverter switches, some part of zero state is utilized. For this, two equal but opposite constant values($\pm V_s$) are compared against the same triangular carrier. The generated pulses are placed in such a way that it occupies the zero states of the inverter, as shown in Fig-8.12. These pulses serve as shoot-through(ST) pulses. For $d_1 = d_2$, ST pulses is given to the switch S_b together with inverter. For pulling the converter into FCCM, a non shoot through(NST) pulse complimentary to ST is generated which controls switch S. The width of these pulses controls the duty cycle of the converter. Though the modulation index and duty cycle are independently varied, the duty ratio is dependent on the period of zero state. The increase in modulation index(m) decreases the period of zero states, correspondingly decreasing duration of duty cycle(d_2) as per inequality Equ-(8.34).

$$m + d_2 \leq 1 \tag{8.34}$$

8.7 Design of passive component, stress analysis and comparison among different topology

To validate the effects and mitigate NZ-DCM, experimentally, 478 W prototype for proof of concept designed and implemented.

8.7.1 Selection of inductor for Buck-Boost stage

In case of three phase balanced load, total AC power is written as $P_{ac} = 3V_{ac}I_{ac}cos\phi$ which does not contain any low frequency ripple. So, the converter is designed as per the inductor current value having only high frequency ripple. The average inductor current for the converter is

$$I_L = \frac{V_{dc}I_{dc} + 3V_{ac}I_{ac}\cos\phi}{d_2 V_{in}} \tag{8.35}$$

The inductor current is calculated for output DC voltage V_{dc}=135 V, AC output voltage V_{ac}=27 V, and input voltage is 90 V. From Equ-(8.35), the inductor current I_L is 8.85 A. Peak to peak ripple current is taken as $\Delta I = 0.7I_L$. For switching frequency of 10 kHz, the value of inductor is calculated as

$$L = \frac{V_{in}d_2}{f_s \Delta I_L} \tag{8.36}$$

The inductor value as per the Equ-(8.36) is 1.3 mH while in this chapter 1.12 mH inductor is used.

8.7.2 Selection of capacitor for Buck-Boost stage

The capacitor is designed as per 1% ripple voltage in the output DC voltage. It is assumed that ESR and ESL is negligible, so the capacitor ripple is given as

$$\Delta V = \frac{I_o(1 - d_2)}{f_s C} \tag{8.37}$$

where I_o is the average output current including both DC and AC load. For V_{dc}=135 V and V_{ac}=27 V, the value of the current is around 5.73 A. From Equ-(8.37), the value of the capacitor is 100 μF. The specification of the hybrid converter is enlisted in Table-8.1.

8.7.3 Switch stress analysis

Inverter switches are subjected to the Buck-Boost voltage generated at the DC terminal. So the maximum voltage stress under which the switches operate, is equal to V_{dc}. Similarly, diode D_2 is also stressed unto voltage V_{dc}. The switch at the input side(S_b) is turned ON during shoot through while turned OFF during non-shoot through state. Thus the voltage is equal to V_{in}. Similarly, Diode D_1 is also experience voltage V_{in}.

Table 8.1: Specification of the converter

Parameter	**Rating**
AC output Power P_{AC}	$219Watt$
DC output Power P_{DC}	$259Watt$
Input Voltage V_{in}	$90V$
Inductance L	$1.12mH$
capacitance C	100 μF
DC output voltage V_{dc}	135 V
AC output voltage V_{ac}	27 V
Peak AC load	5.38 A
DC load	1.92 A
Switching Frequency f_s	$10kHz$
Filter Inductance L_f	$560\mu H$
Filter Capacitance C_f	$10\mu F$

The current stress in proposed converter is different from the cascaded Buck-Boost converter. The current through the inverter switches is equal to inductor current during shoot through while it is equal to the AC load current (i_a,or i_b, or i_c) during non shoot through period. So the maximum current(i_{inv}) which flows through the inverter switch is

$$i_{inv} = i_{L\max} + |i_{ap}| or\ |i_{bp}| or\ |i_{cp}| \tag{8.38}$$

where, subscript p denotes the peak value of corresponding phase current. $i_{L\max}$ is defined as

$$i_{L\max} = \frac{\Delta I}{2} + I_L \tag{8.39}$$

The diode D_1 is turned ON during the non-shoot through state, hence current through D_1 is i_{Lmax}. The diode D_2 is supplying the DC load with capacitance connected across it thus the current through D_2 is $i_{dc} + i_c$. Comprehensive switch stress in different modes is presented in Table-8.2.

Table 8.2: Stress analysis of proposed converter

	Max Voltage Across Switch	**Max Current through Switch**
Inverter Switches	$\frac{d_1 V_{in}}{1-d_2}$	$\|i_{ap}\| or \ \|i_{bp}\|$ or $\|i_{cp}\| + i_{Lmax}$
Switch(S_b)	V_{in}	i_{Lmax}
Diode (D_1)	V_{in}	i_{Lmax}
Diode (D_2)	$\frac{d_1 V_{in}}{1-d_2}$	$i_{dc} + i_c$

8.7.4 Comparison among different topology

The proposed MBBDHC is compared with cascaded Buck Boost VSI and cascaded Buck Boost hybrid converter. Comparison is done on the basis of different parameters of the converter as listed in Table-8.3. Comparison between number of switches, DC and AC gain, modulation index, dual output capability and power conversion stage is obvious from the Table-8.3. Dead time compensation is not required because inverter itself uses the switches as shoot through, so there is no problem of short circuit at inverter end. This property makes the system immune to EMI.

For capacitor, capacitor performance is affected by two type of fault namely sudden short circuit and long time degradation of capacitor. But BBDHC/MBBDHC has inherent protection to these problems. Moreover, in case of cascaded configuration capacitor has to supply both load current i.e. ($i_c = i_{dc} + i_{ac}$) while in BBDHC/MBBDHC capacitor only supply dc load current (i.e. ($i_c = i_{dc}$)) during shoot through state. This causes higher lower loss and lower temperature rise in the converter. These overall analysis lead to high life time of capacitor in case of BBDHC/MBBDHC.

As compared to existing boost topology(BDHC, SBI, L-ZSI), due to absence of NZ-DCM, the proposed MBBDHC is quite superior when operated under wide load variation. Moreover, BDHC, SBI and L-ZSI do not operate satisfactorily in standalone AC mode while MBBDHC does. Unlike the existing boosted topology, the MBBDHC renders output at DC terminal in Buck and Boost mode. A comprehensive comparison is presented in Table-8.4.

Table 8.3: Comparison of proposed converter with existing converter

	Cascaded Buck Boost VSI	**Cascaded Buck Boost Hybrid**	**Proposed Hybrid Converter**
No. of switches	10	10	9
DC gain	$\frac{d_1}{1-d_2}$	$\frac{d_1}{1-d_2}$	$\frac{d_1}{1-d_2}$
Peak AC voltage	$\frac{mV_{in}d_1}{1-d_2}$	$\frac{mV_{in}d_1}{1-d_2}$	$\frac{mV_{in}d_1}{1-d_2}$
Modulation index	$0 \leq m \leq 1$	$0 \leq m \leq 1$	$0 \leq m \leq 1-d_2$
Dual output	No	Yes	Yes
Dead time	Yes	Yes	No
Max degree of freedom	2	2	2
EMI immunity	No	No	Yes
Power conversion stage	Two	Two	One
Capacitor life time	Poor	Poor	High

Table 8.4: Comparison of proposed converter with existing Boost converter

	BDHC	**SBI**	**L-ZSI**	**MBBDHC**
DC gain	$\frac{1}{1-d}$	$\frac{1}{1-2d}$	$\frac{1+d}{1-d}$	$\frac{d}{1-d}$
Peak AC voltage	$\frac{mV_{in}1}{1-d}$	$\frac{mV_{in}1}{1-2d}$	$\frac{mV_{in}1+d}{1-d}$	$\frac{mV_{in}d}{1-d}$
Modulation index	$0 \leq m \leq 1-d$	$0 \leq m \leq 1-d$	$0 \leq m \leq 1-d$	$0 \leq m \leq 1-d$
Dual output	Yes	Yes	Yes	Yes
Dead time	No	No	No	No
Max degree of freedom	2	2	2	2
EMI immunity	Yes	Yes	Yes	Yes
Power conversion stage	One	One	One	One
Capacitor life time	High	High	High	High
Buck voltage at DC terminal	No	No	No	Yes
NZ-DCM	Yes	Yes	Yes	No
Standalone AC	No	Yes(restricted range)	No	Yes

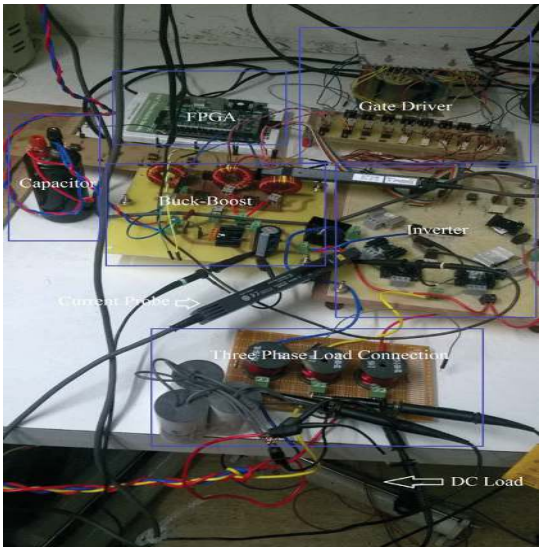


Figure 8.13: Experimental setup for MBBDHC

8.8 Result analysis

For analyzing the performance of the proposed converter in different operating region, the converter is simulated on MATLAB/Simulink platform and validated on hardware. The experimental setup is shown in Fig-8.13. The converter is designed for 478 W power rating. The DC and AC output is 259 W and 219 W respectively. The components used in experimentation are enlisted in Table-8.5. The spikes in the experimental voltage and current is due to switching of antiparallel switch S, stray inductance and parasitic capacitances.

Table 8.5: Components used in experiment

S.N.	Component	Number and Manufacturer	Rating
1.	MOSFET	SIHG32N50D Vishay Siliconix	550 V, 30 A
2.	IGBT	IRG4BC40FPbF IOR Corp.	600 V, 27 A
3.	Diode (D_a)	ISL9R1560G2 Fairchild	600 V, 15 A
4.	Gate Drive IC	HCPL3120 Avago Technology	30 V, 2.5 A
5.	Inductor	Coilcraft	1.12 mH
6.	Capacitor	Kemet	100 μF

8.8.1 Open loop analysis

Boost operation under CCM

For boost operation, converter is operated at $d_2 = 0.6$ and modulation index $m = 0.39$. The output DC voltage is around 135 V while AC voltage is 27 V. Peak AC load is kept at 5.38 A while DC load is equal to 1.92 A. Fig-8.14 and Fig-8.15 present results corresponding to this mode. Under this condition the term C_L is 1.93 while C_R is around 1.49 i.e $C_L > C_R$. This confirms that the converter is operating under CCM which is further verified by noticing the inductor current behaviour.

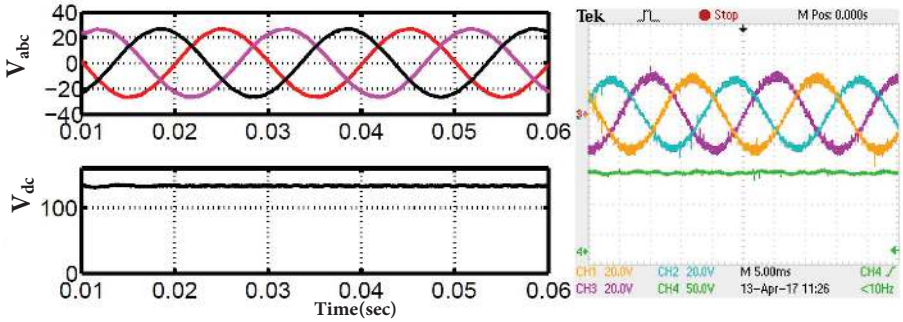


Figure 8.14: CCM of BBDHC: a) AC voltage b) Capacitor voltage $[Ch1 : 10V/div, Ch2 : 10V/div, Ch3 : 10V/div, Ch4 : 50V/div]$

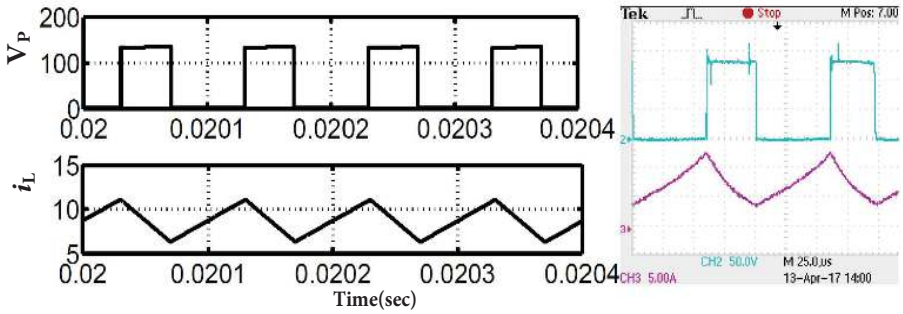


Figure 8.15: CCM of BBDHC: a) DC link voltage b) Inductor current $[Ch2 : 50V/div, Ch3 : 5A/div]$

NZ-DCM in BBDHC

During this mode, the converter is operated at lower duty cycle and peak AC load current is 2.1 A while DC load is decreased to 0.5 A. Duty cycle is kept at 0.28 and modulation

index is 0.675. C_L for this case is 0.5 while C_R is 1.26 which violates the condition stated by Equ-(8.17). Fig-8.16 and Fig-8.17 shows the corresponding results. The output DC voltage observed is 50 V which is higher than expected 35 V. A dip in the DC link voltage and saturation in inductor current confirm the NZ-DCM operation. AC voltage is lower than the expected while the THD in AC voltage increased to 10 % which is quite high.

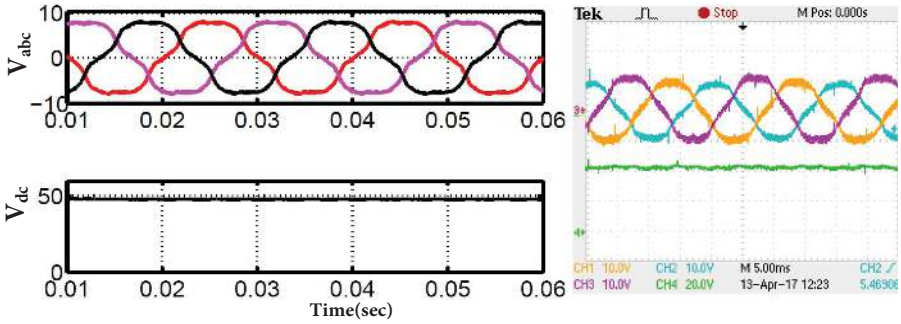


Figure 8.16: DCM of BBDHC: a) AC voltage b) Capacitor voltage $[Ch1 : 10V/div, Ch2 : 10V/div, Ch3 : 10V/div, Ch4 : 20V/div]$

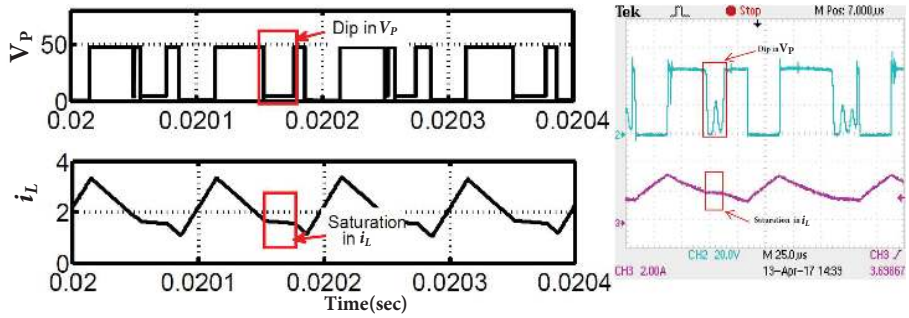


Figure 8.17: DCM of BBDHC: a) DC link voltage b) Inductor current $[Ch2 : 20V/div, Ch3 : 2A/div]$

FCCM in BBDHC

For FCCM, the antiparallel switch S is triggered. Fig-8.18 and Fig-8.19 shows the results for this mode. The inductor current is triangular in nature. Moreover, the THD in AC voltage is reduced to 2%. Besides this the DC voltage is observed around 35 V which is same as expected theoretical value.

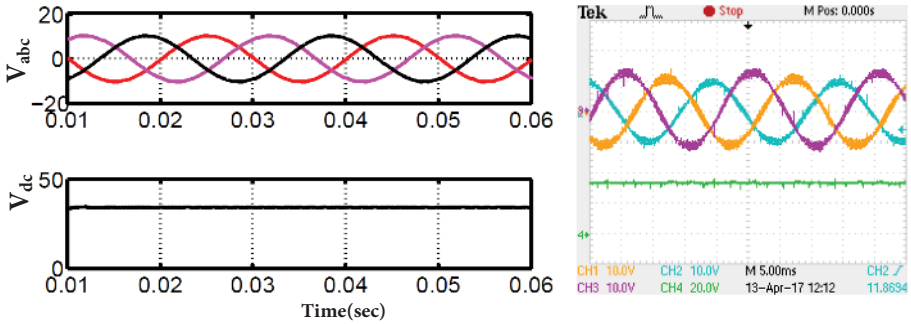


Figure 8.18: FCCM of BBDHC: a) AC voltage b) Capacitor voltage [$Ch1 : 10V/div, Ch2 : 10V/div, Ch3 : 10V/div, Ch4 : 20V/div$]

Stand alone AC operation

Stand alone AC operation is required when DC load is switched off but AC load needs to operate. This operation is not possible in BDHC [131] and proposed BBDHC. To attain the standalone AC, MBBDHC is used. In standalone AC operation diode fails to conduct so, a current path is provided by the antiparallel switch S which is to be turned ON during NST period. Fig-8.20 and Fig-8.21 show the AC voltage and inductor current for m=0.39 and d_2=0.6. Peak AC load is equal to 5.38 A while DC load is taken as zero.

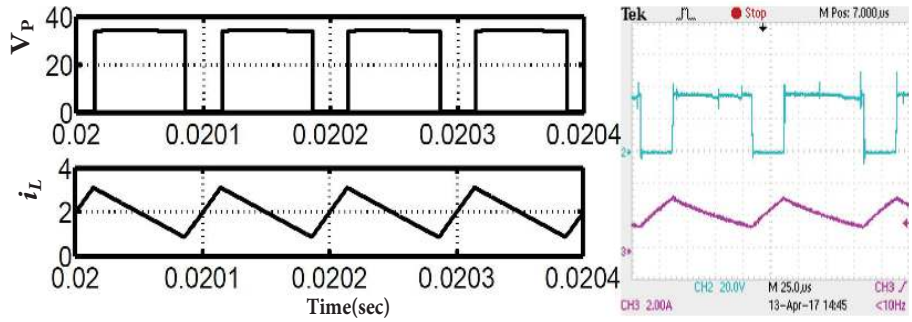


Figure 8.19: FCCM of BBDHC: a) DC link voltage b) Inductor current [$Ch2 : 20V/div, Ch3 : 2A/div$]

DC stand alone operation

For stand alone DC operation, the AC load is disconnected. Results corresponding to this mode is shown in Fig-8.22 and Fig-8.23. The DC standalone operation is performed at $d_2 = 0.6$. The inductor current and voltage profile confirm CCM during standalone DC operation. The average DC current is 1.92 A while AC current is equal to zero.

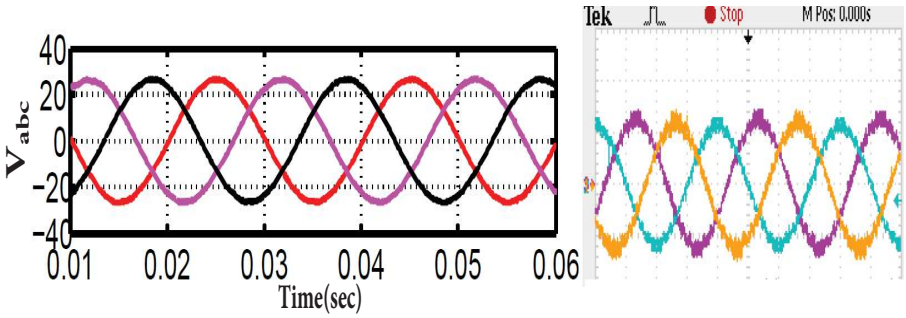


Figure 8.20: Standalone AC: AC voltage $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div]$

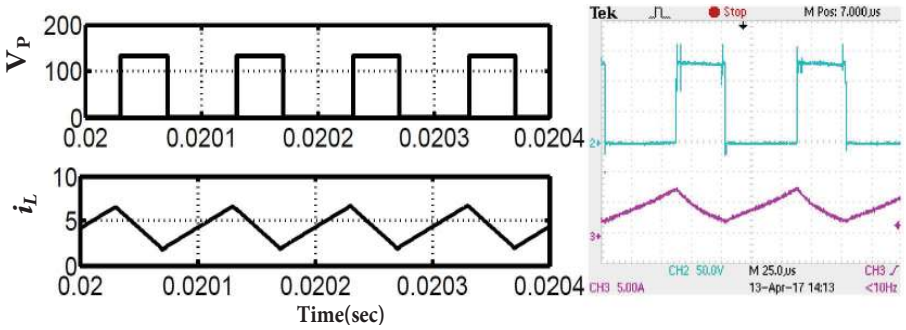


Figure 8.21: Standalone AC: a) DC link voltage b) Inductor Current $[Ch2 : 50V/div, Ch3 : 5A/div]$

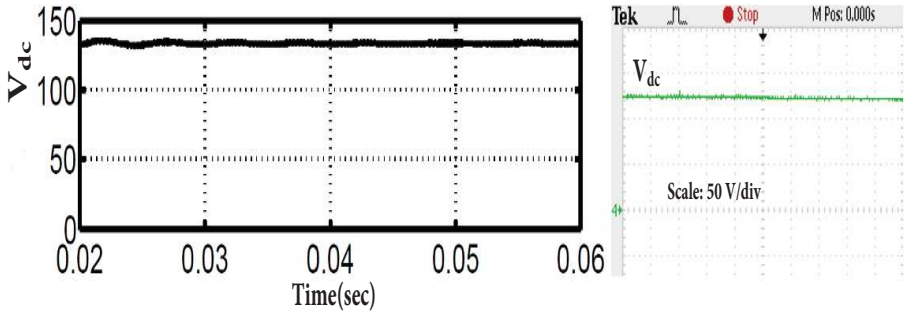


Figure 8.22: Standalone DC: Voltage across capacitor C $[Ch4 : 50V/div]$

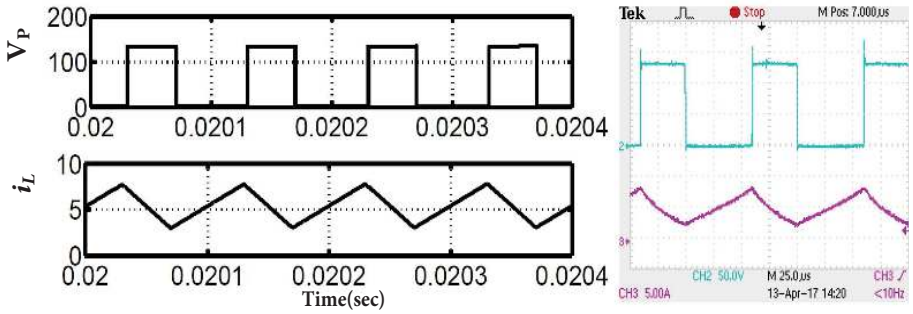


Figure 8.23: Standalone DC: a) DC link voltage b) Inductor Current [$Ch2 : 50V/div, Ch3 : 5A/div$]

8.8.2 Closed loop analysis

To validate the transient performance and cross regulation between DC and AC controller, closed loop analysis is done for MBBDHC. The variation in DC and AC voltage is done such that the constraint given by Equ-(8.34) must not violate. For exhaustive analysis, four different cases are considered.

Behaviour under AC load change

To evaluate the performance of the converter in this case, 30% step change in load is initiated at $t = 0.12s$. The AC load current in increased from 2 A to 2.8 A as shown in Fig-8.24b. The AC voltage remains constant after a small disturbance at $t = 0.12s$, shown in Fig-8.24a. Moreover, DC voltage and DC current is not affected by change in load, shown in Fig-8.24c and Fig-8.24d. Therefore, DC controller robust to change in AC load.

AC voltage tracking

To ensure the rugged performance of the AC controller, the converter is subjected to step change in reference input. At $t = 0.12$, reference input voltage is changed from the 17 V to 25 V as shown in Fig-8.25a. The controller is able to maintain the reference voltage with excellent transient and steady state response. As soon as, the AC voltage is changed, AC load current also changes as the controller is running in voltage control mode as shown in Fig-8.25b. Moreover, the DC voltage and current maintain constant value throughout whole period, shown in Fig-8.25c and Fig-8.25d.

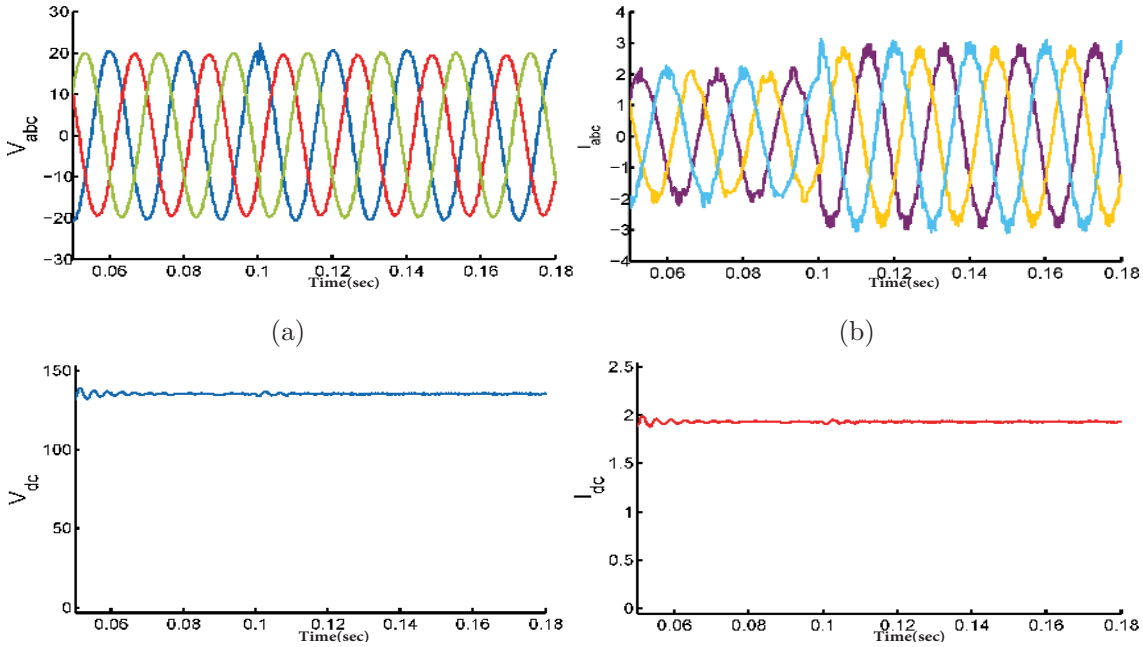


Figure 8.24: Behaviour under AC load change

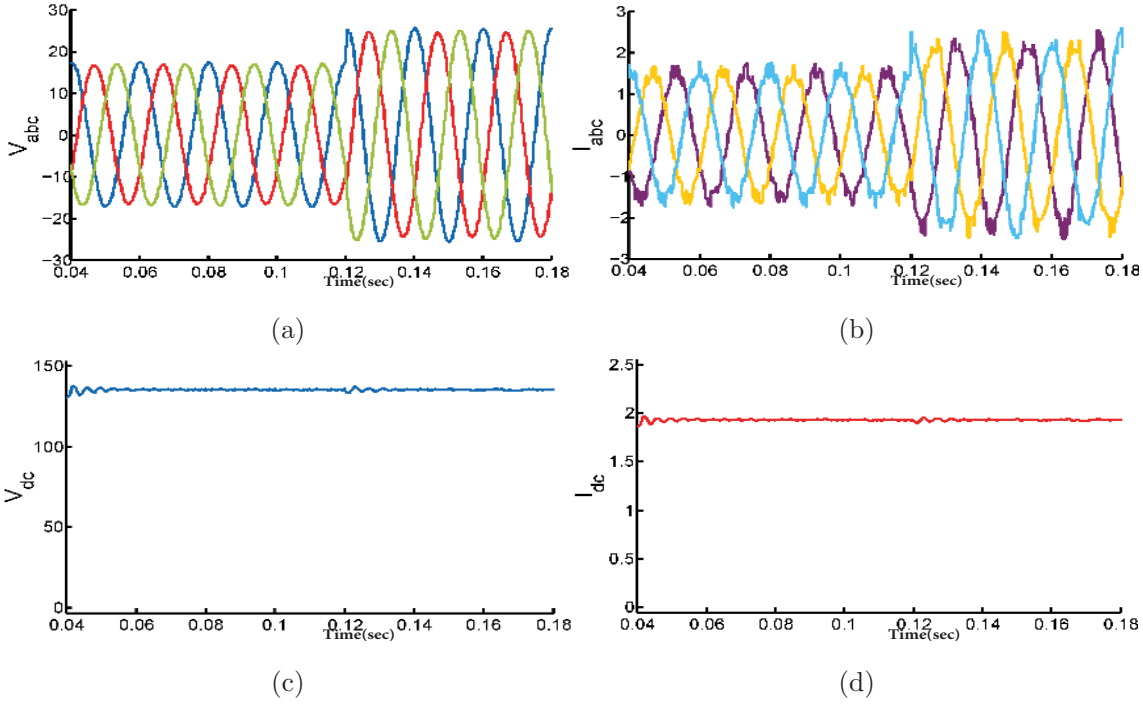


Figure 8.25: Behaviour under AC voltage tracking

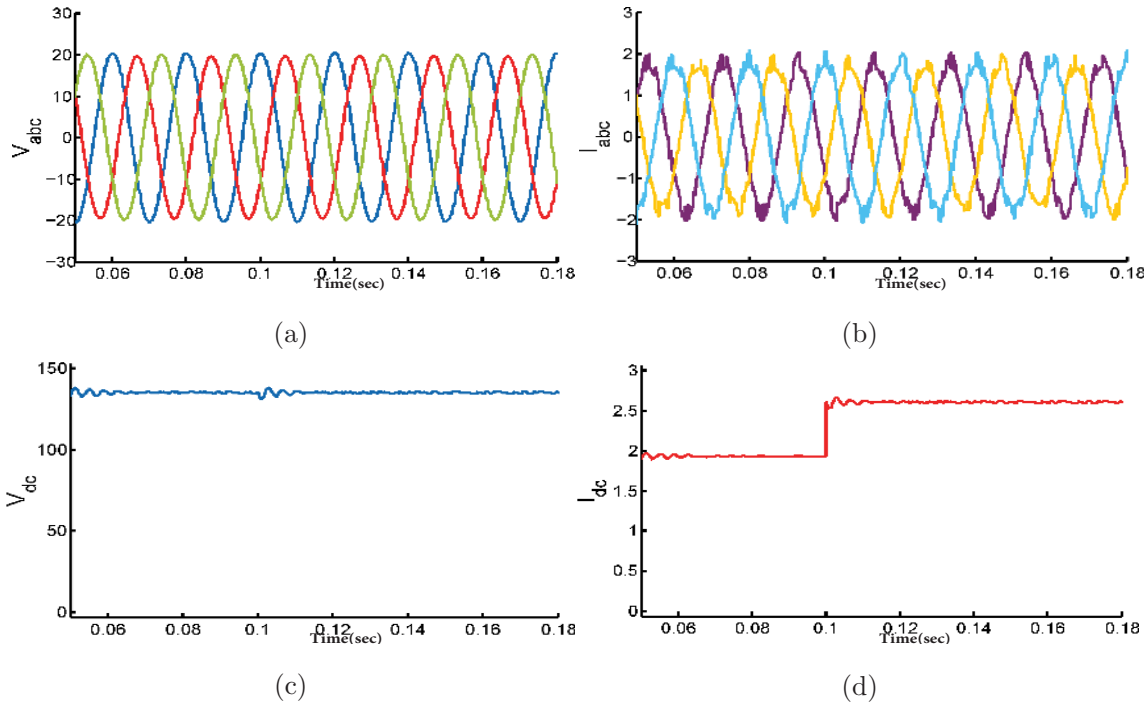


Figure 8.26: Behaviour under DC load change

Behaviour under DC load change

In this case, the controllers ability under DC load change is evaluated. A sudden increase in load is applied at $t = 0.1s$. Due to this, a sharp increase in load current from 1.92 A to 2.65 A is observed as shown in Fig-8.26d. After a initial transient, DC voltage stabilizes to its steady state value as shown in Fig-8.26c. Furthermore, change in DC load does not affect the AC voltage and current as shown in Fig-8.26a and Fig-8.26b.

DC voltage tracking

To validate the robustness of DC voltage controller under reference voltage tracking, a change in reference input voltage is provided at $t = 0.1s$. The DC voltage is changed from 110 V to 135 V instantly as shown in Fig-8.27c. The DC controller is adopts maintain reference voltage after 0.01s which indicates that controller is prone to change in DC load voltage. However, AC voltage controller is not affected by DC changes as shown in Fig-8.27a and Fig-8.27b.

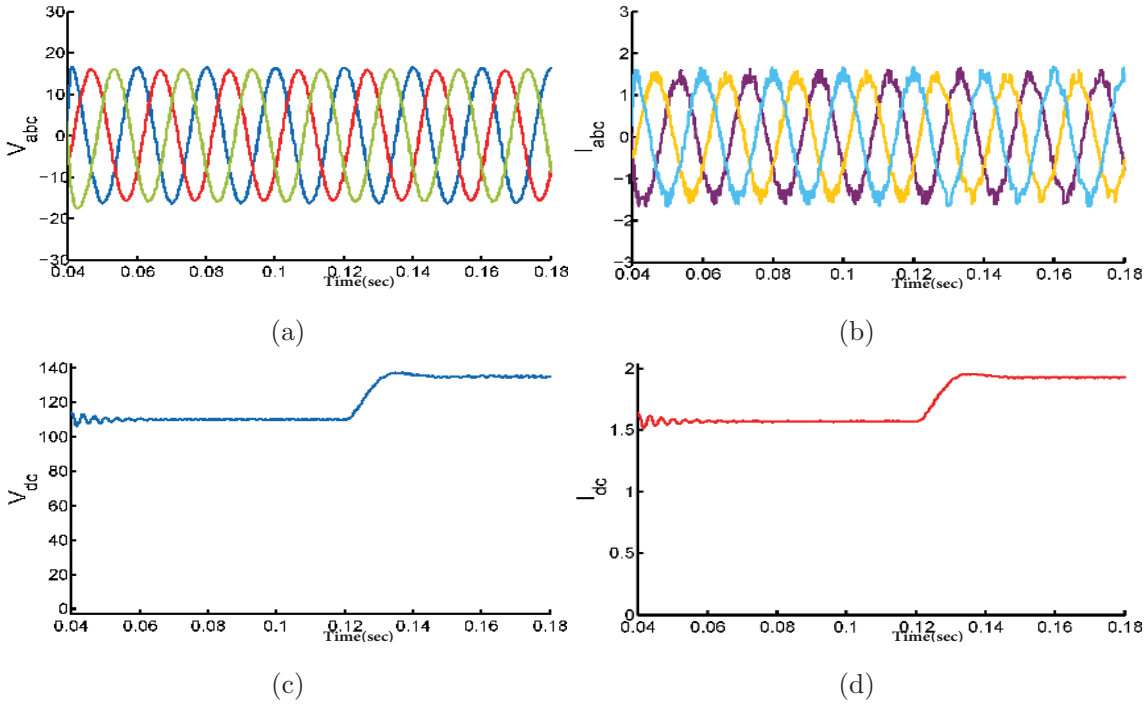


Figure 8.27: Behaviour under DC voltage tracking

8.9 Conclusion

The MBBDHC is proposed in this chapter which is inherently immune to shoot through and dead time problems. As compared to conventional cascaded Buck-Boost converter, the proposed converter provides hybrid output without any extra active switch. The converter CCM and NZ-DCM analysis is done under wide load variation. The term $C_L > C_R$ validated the analytical analysis for CCM operation. On the other hand, $C_L < C_R$ violates the condition for CCM leading to NZ-DCM operation. Operation under NZ-DCM resulted in large THD(10%) along with aberrant voltage at DC terminal. The THD is lowered to 2% by pushing the converter into FFCM. Moreover, during FFCM, the DC voltage is in agreement with the expected value and stable standalone AC operation is achieved. Furthermore, the cross regulation and transient performance of the AC and DC controller are established by changing both the loads and reference input.