Chapter 6

Modified Boost Derived Hybrid Converter

6.1 Introduction

For hybrid (AC and DC) output, the cascaded boost inverter require additional switch and large DC link capacitor, resulting in large sized converter with reduced efficiency [48]. Though replacement of VSI by ZSI seems immediate solution, extra passive elements complicate the design and size of the converter. Switched boost converter for DC and AC load is proposed in [51], [130] but it suffers from increased number of passive and active elements. An interesting solution is reported in the form of boost derived hybrid converter (BDHC) [131] that integrates ZSI within a boost converter. Unlike cascaded boost inverter, BDHC renders output in a single stage. It is immune to EMI and also relieves the current stress on DC link capacitor. However, it suffers from two limitation

1) Unstable standalone AC mode

2) Aberrant behaviour during NZ-DCM

The DCM of conventional boost converter is different than the NZ-DCM of BDHC. Due to the combined effect of low duty ratio and higher AC load current(i_{ac} is assumed constant), the inductor current acquires chopped current phenomenon in BDHC, as shown in Fig 6.1. This mode is termed as non zero discontinuous current mode (NZ-DCM). Unlike conventional boost converter the inductor current does not reach zero, instead it saturates at the load current.

To address the limitations of BDHC, this chapter investigates BDHC operating

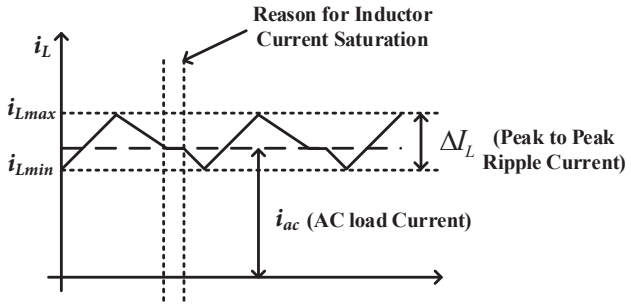


Figure 6.1: NZ-DCM of inductor current

boundary conditions under NZ-DCM and standalone AC mode [126]. This investigation is supported by using analytical results and experimental observations. The effect of DCM is analyzed by calculating the THD and ripple voltage. Besides, to mitigate the issues identified in BDHC modified-BDHC (MBDHC) is proposed. The performance of MBDHC and BDHC are compared to understand their pros and cons. In addition, the efficiency is estimated for MBDHC and compared to BDHC and cascaded boost inverter. Following are the advantages of MBDHC

1) Possess the benefits of ZSI i.e. immune to shoot-through problem and boost the output voltage.

2) Supply simultaneous AC and DC load

3) Operate under CCM hence no input filter requirement

4) AC standalone operation is possible

5) DC standalone operation is inherently present.

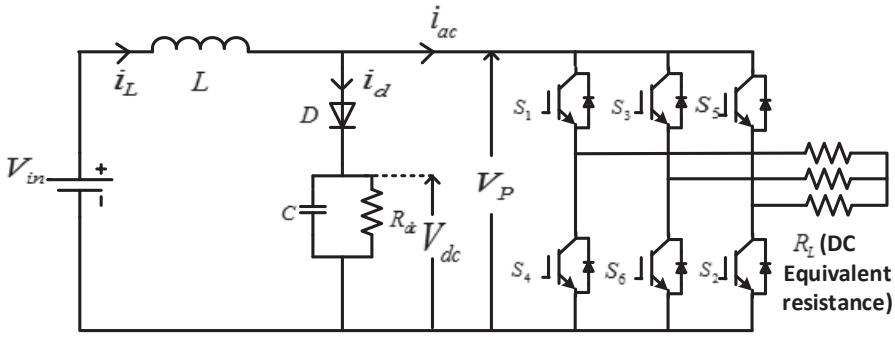


Figure 6.2: Boost derived hybrid converter

6.2 BDHC: Operating modes and limitation

6.2.1 Operation

The output of conventional BDHC, as shown in Fig 6.2, is comprised of a three phase AC load having DC equivalent load resistance R_L and a DC load resistance (R_{dc}). Symbols i_L, i_d, i_{ac}, V_P and V_{dc} are inductor current, diode current, equivalent ac current, DC link voltage and DC load voltage, respectively. The three operating modes of the converter, namely shoot-through, active and zero are decided by the switching pattern of the three phase inverter integrated within BDHC.

Shoot-through State

In this mode, the two switches of the same leg are turned ON concurrently(Fig 6.3). The diode D becomes reversed biased, disconnecting the DC load from the source. The inductor L is energised by the source voltage via shoot-through path. Shoot through time is equal to the duty cycle(d).

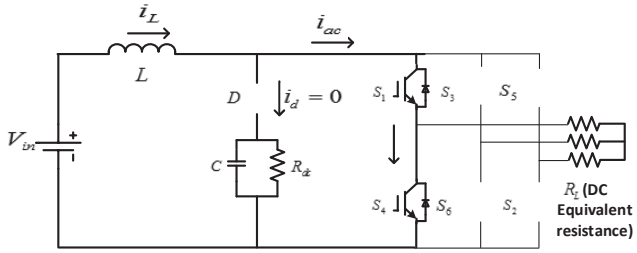


Figure 6.3: Shoot-through mode

Active state

During this mode, the inverter is switched to non-zero state, similar like a classical VSI. The inductor flips the voltage polarity (due to negative $\frac{di_L}{dt}$), making the diode forward biased and bringing DC load into the circuit. The inductor transfer its energy to the AC load (through the three phase inverter) and to the DC load (through the diode), as shown in Fig 6.4.

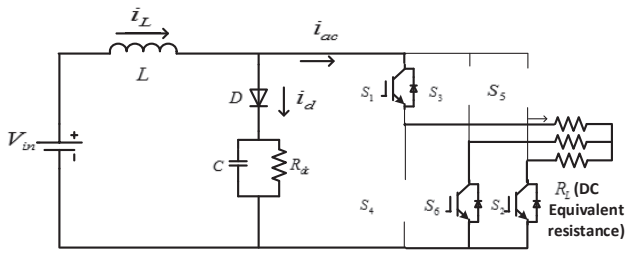


Figure 6.4: Active mode

Zero state

The inverter switches disconnect AC load from DC link in this mode. Diode D is forward biased which permits the inductor energy transfer to capacitor C. The diode across the switches allow inductive AC load current to freewheel.

Only equivalent DC current from the source is supplied during zero state as i_{ac}=0. The AC load maintains its continuous operation through freewheeling diodes present in the converter.

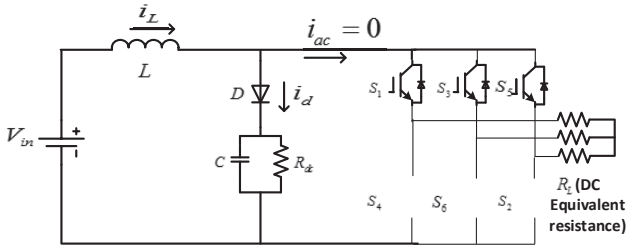


Figure 6.5: Zero mode

The effect of these three states are combined for deriving DC and AC output voltage. Averaging the inductor voltage over a switching period, and equating it to zero.

$$dV_{in} + (1-d)(V_{in} - V_P) = 0 \tag{6.1}$$

$$V_P = \frac{1}{1-d} V_{in} \tag{6.2}$$

For modulation index m, AC gain in terms of phase voltage is given as

$$v_{ac} = \frac{m}{2} V_P \tag{6.3}$$

6.2.2 Steady state analysis

For theoretical analysis, the inverter fed AC load is modeled as a constant current source. The active and passive components are considered to be ideal. To avoid zero current DCM, sufficient value of inductor is taken.

The total input current(I_{in}) over a period is given as

$$I_{in} = I_L \tag{6.4}$$

where I_L is average current through inductor.

As per the power balance theory

$$InputPower(P_{in}) = DCPower(P_{dc}) + ACPower(P_{ac}) \tag{6.5}$$

Thus

$$V_{in}I_{in} = V_{dc}I_{dc} + 3V_{ac}I_{ac}cos\varphi \tag{6.6}$$

where V_{ac} and I_{ac} are rms value of ac phase voltage and current.

Substituting I_{in} from Equ-(6.4) into Equ-(6.6), I_L can be expressed as

$$I_L = \frac{V_{dc}I_{dc} + 3V_{ac}I_{ac}cos\varphi}{V_{in}} \tag{6.7}$$

During shoot through peak-peak ripple current

$$\Delta I_L = \frac{dV_{in}}{f_s L} \tag{6.8}$$

where f_s is switching frequency at boost stage.

For supplying simultaneous DC load and AC load, the input current must be greater than zero and diode must be forward biased i.e.

$$\begin{aligned} i_{Lmin} - i_{ac} &> 0 \\ (I_L - \tfrac{\Delta I_L}{2}) - i_{ac} &> 0 \end{aligned} \tag{6.9}$$

where i_{ac} is peak value of AC load current. From Equ-(6.7), Equ-(6.8) and Equ-(6.9),

$$\frac{V_{dc}I_{dc} + 3V_{ac}I_{ac}cos\varphi}{V_{in}} - \frac{V_{in}d}{2f_s L} - i_{ac} > 0 \tag{6.10}$$

Replacing peak current by rms value ($i_{ac} = \sqrt{2} * I_{ac}$) and rearranging Equ-(6.10), Equ-(6.11) is obtained

$$I_{dc} > \sqrt{2}(1-d)I_{ac} - \frac{3m}{2\sqrt{2}}I_{ac}\cos\phi + \frac{d(1-d)V_{in}}{2f_s L} \tag{6.11}$$

$$\xi > \chi \tag{6.12}$$

where ξ=I_{dc}, $\chi = \sqrt{2}(1-d)I_{ac} - \frac{3m}{2\sqrt{2}}I_{ac}\cos\phi + \frac{d(1-d)V_{in}}{f_s L}$

For continuous current mode(CCM) in case of simultaneous DC and AC load, Equ-(6.12) must be satisfied, else it may lead to inadvertent operation of the converter.

There are two distinct cases under which BDHC fails to operate satisfactorily.

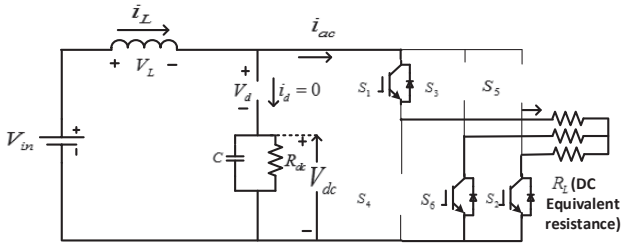


Figure 6.6: NZ-DCM mode

NZ-DCM during simultaneous AC and DC loads

During high load or low power factor AC load conditions, the current drawn by the load is high. The inductor current saturates to equivalent AC current(i_{ac}) drawn from the converter i.e. $i_L = i_{ac}$. This results in constant inductor current which is termed as NZ-DCM. Applying KVL in Fig-6.6 and equating average voltage across the inductor to zero

$$\begin{aligned} V_{in} - V_L - V_d - V_{dc} &= 0 \\ V_d &= V_{in} - V_{dc} \end{aligned} \tag{6.13}$$

Since the voltage across dc load is higher than the input voltage i.e. $V_{dc} > V_{in}$, V_d becomes negative, causing the diode to reverse bias thus the DC load is only connected to the capacitor i.e. $i_d = 0$. If NZ-DCM lasts for sufficiently long period, the capacitor fails to maintain constant voltage which results in dc voltage dips and eventually distorts the AC voltage. Though, this case pertaining to NZ-DCM can be addressed by incorporating huge size of inductor along with extremely high switching frequency. These solutions are not feasible as the required inductor is of the order of henry.

Standalone AC load

During standalone AC mode, the DC load is disconnected from the circuit and only diode and capacitor in series remain connected. The inductor in series with the switched load,

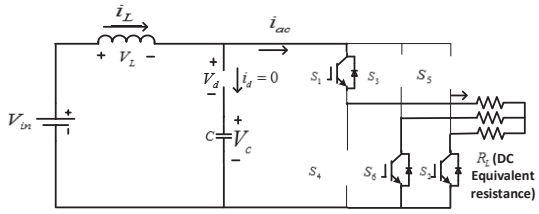


Figure 6.7: Standalone AC mode

create huge spikes across the switches which may even damage the switches. To overcome this a snubber circuit is recommended to clamp the switching noise [132] . The diode and capacitor of BDHC serve as the snubber circuit. However, for proper operation of snubber, the diode must remain turned on. Since DC load current is zero, Equ-(6.12) is no more valid. During discharging period of the inductor(NST), the sum of voltage across the inductor and input becomes less than the capacitor voltage i.e. $V_L + V_{in} \leq V_c$ resulting in reverse biased condition of diode, as shown in Fig-6.7. Hence stable AC standalone operation is not possible for a conventional BDHC.

To overcome these limitations of BDHC, a suitable modification is proposed.

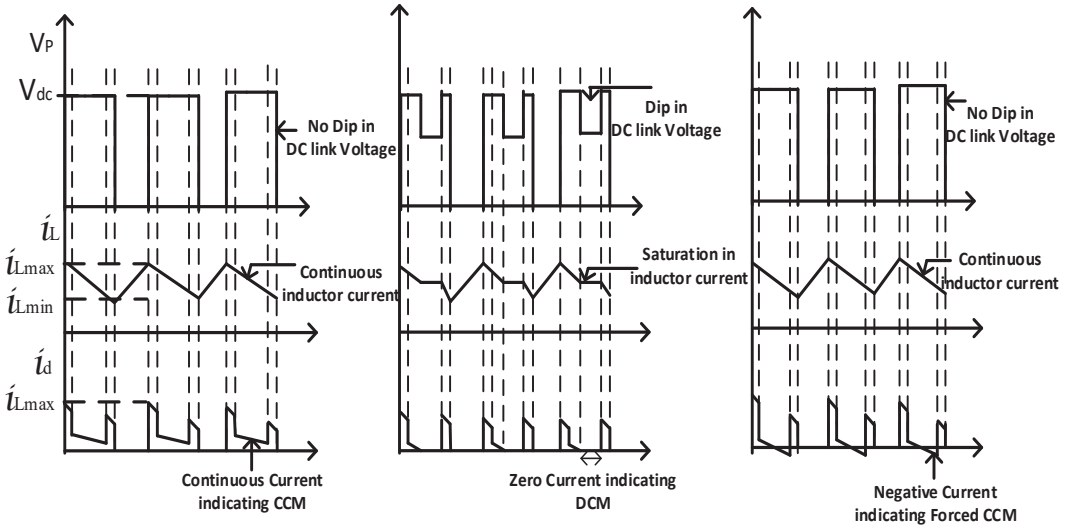


Figure 6.8: a) CCM of BDHC b) DCM of BDHC c) FCCM of MBDHC

6.3 Modified BDHC and its control

In a conventional BDHC during NZ-DCM, i_L saturates at the level of AC load current due to overcharging of the capacitor, as shown in Fig-6.8. In the proposed modified converter as shown in Fig-6.9, an antiparallel switch is connected across the diode. To release the energy stored by the overcharged capacitor, the switch S is turned-on in complement to the shoot-through mode. Part of energy is transferred from the capacitor to the AC load. Consequently, this switch S connects the DC load to the source. This redeems the NZ-DCM with FCCM and removes the dip in the dc link voltage.

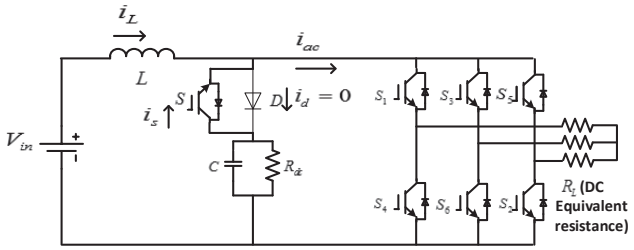


Figure 6.9: Modified boost derived hybrid converter

In case of standalone AC operation, the switch S placed antiparallel across the diode is turned on to divert part of energy to the AC load, allowing smooth AC standalone operation. The MBDHC has four operating states. The first three states namely, shoot-through, active and zero state are similar to that of conventional BDHC. The replacement of NZ-DCM by FCCM creates the fourth operating state -*Forced active state*. During NZ-DCM the inductor current saturates at the AC load current, as shown in Fig-6.8-b, resulting in zero diode current. To bring to its normal operation, an antiparallel switch across the diode is turned on such that the capacitor voltage become less than the sum of source and inductor voltage i.e $V_c \leq V_L + V_{in}$. The current through the diode path is transferred through the antiparallel switch indicated by i_s which is opposite to diode current i_d in Fig-6.9, so the current is negative in Fig-6.8-c during the NZ-DCM period.

The control signals are created in a manner such that NZ-DCM is replaced by FCCM. For impedance source converter, several modulation techniques have been proposed earlier [105], [133], [113]. However, these techniques lack independent control of m and d. For the work presented in this chapter, simple boost control strategy is opted. The triangular carrier wave is compared with the three phase sinusoidal waveform and two constant val-

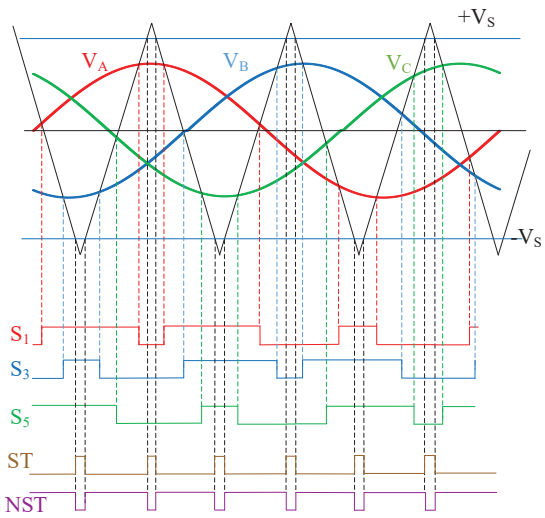


Figure 6.10: Control pulses for the MBDHC

ues (which is equal to duty cycle) having equal and opposite magnitude. The frequency of sine wave is 50 Hz and carrier frequency is 5 kHz. Fig-6.10 shows the pulses for inverter switches along with shoot-through (ST) pulse, which is to be multiplexed with all the switching signals of the inverter. The ST pulses which are responsible for boosting are created at 10 kHz while inverter operates at 5 kHz. This is due to the fact that ST is generated by comparing two constant values(V_s and $-V_s$). For antiparallel switch across the diode, non shoot through pulse (NST) is utilised. No dead time is required between ST and NST for converter operation. Although duty cycle and modulation index are controlled independently but range is restricted. The necessary condition that must be satisfied to operate the converter is

$$m + d \leq 1 \tag{6.14}$$

Similar to BDHC, this is the main limitation of the proposed MBDHC. Since MBDHC has one extra switch so the overall losses of the converter could be slightly higher than BDHC. The effect of the extra switch on MBDHC efficiency is discussed in the next section.

6.4 Comparative efficiency analysis

For analyzing the efficiency of MBDHC as compared to BDHC and cascaded boost inverter topologies, the converters are modeled in their corresponding operating modes. The DC

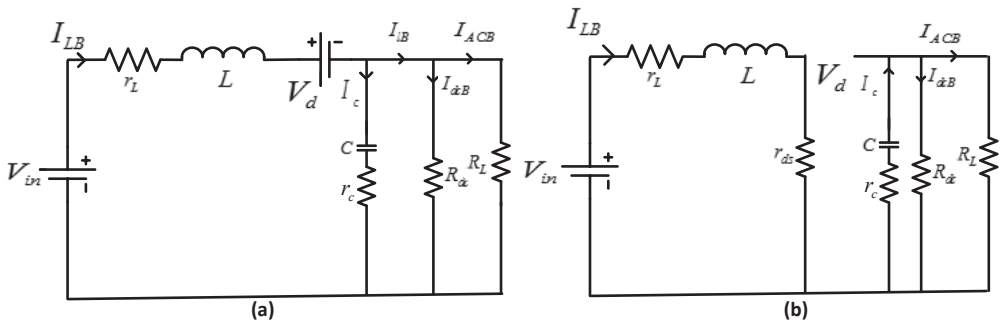


Figure 6.11: Boost+Inverter a) Non shoot-through period b) Shoot-through period

load is represented by resistive load (R_{dc}), while capacitance is represented in terms of its ESR (r_c) and capacitance (C). The diode is replaced by its equivalent circuit having diode resistance $r_d = 0$ and forward voltage drop V_d and MOSFET is replaced by on state resistance r_{ds}. The inductor is represented by resistance(r_L) in series with the inductance(L), while the three phase AC load, based on equivalent power relation, is modeled as DC load having resistance (R_L).

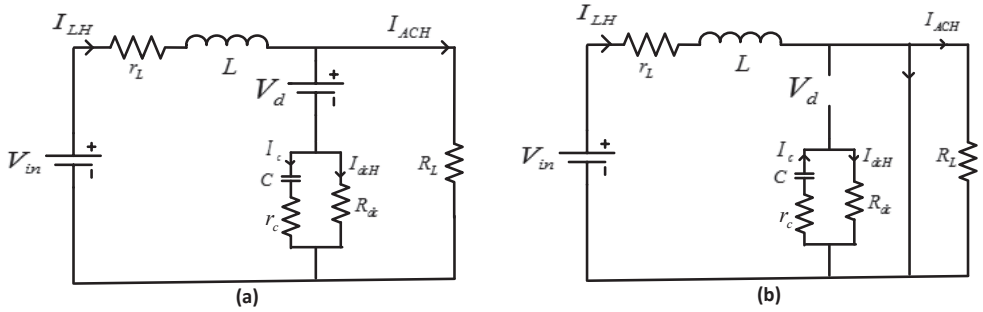


Figure 6.12: BDHC a) Non shoot-through Period b) Shoot-through period

6.4.1 Cascaded boost inverter

From Fig-6.11 during non shoot-through period(κ) , the power loss equation is given as

$$P_{nst} = \kappa^2 \left[{I_{LB}}^2 r_L + (I_{LB} - I_{lB})^2 r_c \right] + \kappa V_d I_{LB} \tag{6.15}$$

and during shoot-through period(d)

$$P_{st} = d^2 {I_{LB}}^2 r_L + d^2 (I_{dcB} + I_{ACB})^2 r_c + d^2 {I_{LB}}^2 r_{ds} \tag{6.16}$$

6.4.2 BDHC

From Fig-6.12b non-shoot through state, power loss equation is termed as

$$\begin{aligned} P_{nst} = \kappa^2 \left[{I_{LH}}^2 r_L + (I_{LH} - I_{ACH} - I_{dcH})^2 r_c \right] \\ + \kappa V_d \left[I_{LH} - I_{ACH} \right] \end{aligned} \tag{6.17}$$

and for shoot through state

$$P_{st} = d^2 {I_{LH}}^2 r_L + d^2 {I_{dcH}}^2 r_c \tag{6.18}$$

6.4.3 MBDHC

The equivalent circuit of MBDHC is similar to that of BDHC. However, due to the presence of antiparallel switch across the diode the conduction can take place through the diode or antiparallel switch, depending on the load and duty cycle. From simulation study it is found that the conduction period of the antiparallel switch and diode are in proportion of 70:30. During non shoot-through period

$$\begin{aligned} P_{nst} = \kappa^2 \left[{I_{LH}}^2 r_L + (I_{LH} - I_{ACH} - I_{dcH})^2 r_c \right] \\ + 0.7\kappa V_d \left[I_{LH} - I_{ACH} \right] + (0.3\kappa)^2 (I_{ACH} - I_{LH})^2 r_{ds} \end{aligned} \tag{6.19}$$

During shoot-through period

$$P_{st} = d^2 {I_{LH}}^2 r_L + d^2 {I_{dcH}}^2 r_c \tag{6.20}$$

For comparative analysis, the generalized form of efficiency for cascaded boost inverter/BDHC/MBDHC is given as

$$\begin{aligned} \eta = \frac{P_{out}}{P_{in}} = \frac{P_{dc} + P_{ac}}{P_{st} + P_{nst} + P_{dc} + P_{ac}} \\ = \frac{1}{1 + M_{pu}} \end{aligned} \tag{6.21}$$

where

$$\begin{aligned} M_{pu} = A \left(\frac{1}{R_{dc}} + \frac{1}{R_L} \right) + B \left(\frac{1}{R_{dc}} + \frac{1}{R_L} \right) + C \frac{1}{V_{in}} \\ + E \left(\frac{1}{R_{dc}} + \frac{1}{R_L} \right) \end{aligned}$$

Table 6.1: Loss factors

	A	B	C	E
Cascaded Boost Inverter	$\frac{d^2+(1-d)}{(1-d)^2}^2 r_L$	$2d^2 r_c$	$(1-d)V_d$	$\frac{d^2}{(1-d)^2} r_{ds}$
BDHC	$\frac{d^2+(1-d)}{(1-d)^2}^2 r_L$	$d^2\left(1+\left(\frac{I_{dc}}{I_{ac}+I_{dc}}\right)^2\right) r_c$	$(1-d)\left(\frac{I_{dc}+dI_{ac}}{I_{dc}+I_{ac}}\right) V_d$	0
MBDHC	$\frac{d^2+(1-d)}{(1-d)^2}^2 r_L$	$d^2\left(1+\left(\frac{I_{dc}}{I_{ac}+I_{dc}}\right)^2\right) r_c$	$0.7(1-d)\left(\frac{I_{dc}+dI_{ac}}{I_{dc}+I_{ac}}\right) V_d$	$0.09\left(\frac{I_{dc}+dI_{ac}}{I_{dc}+I_{ac}}\right)^2 r_{ds}$

where the terms A, B, C and E are dependent on duty cycle. These terms are different for cascaded boost inverter, BDHC and MBDHC which are presented in Table-6.1. The value of variables corresponding to components used in the circuit is chosen from their data sheet and given as r_c=1.57 Ω, r_L=1.8 Ω, V_d=2 V and r_{ds}=0.75 Ω. From the analysis based on Fig-6.13, it is found that the term A is equal in all the cases. The term B is same for BDHC and MBDHC and is lower than its counterpart cascaded boost inverter. For the term C, BDHC has comparative smaller value than cascaded boost inverter and even MBDHC has smaller value than BDHC for duty cycle cycle variation because diode conducts only for around 70% of duty. In case of term E, BDHC has zero value and MBDHC has very small value compared to cascaded boost inverter. Therefore, the efficiency of BDHC is higher than cascaded boost inverter. On the other hand, MBDHC contribute 30% lower loss in case of factor C while it has almost same amount of the increment in losses for factor E. This signifies, efficiency of BDHC and MBDHC is almost comparable which obviously depends on the switch and diode resistances. So, the presented solution is best fit to replace the existing converter for supplying dual output application.

6.5 Design of passive component and stress analysis

To validate the effects and mitigate NZ-DCM experimentally, a 635 W prototype for proof of concept is designed and implemented. The specification of the hybrid converter is enlisted in Table-6.2.

6.5.1 Selection of inductor for boost stage

In case of three phase balanced load, total ac power is written as $P_{ac} = 3V_{ac}I_{ac}cos\phi$ which does not contain any low frequency ripple. The average inductor current for the converter

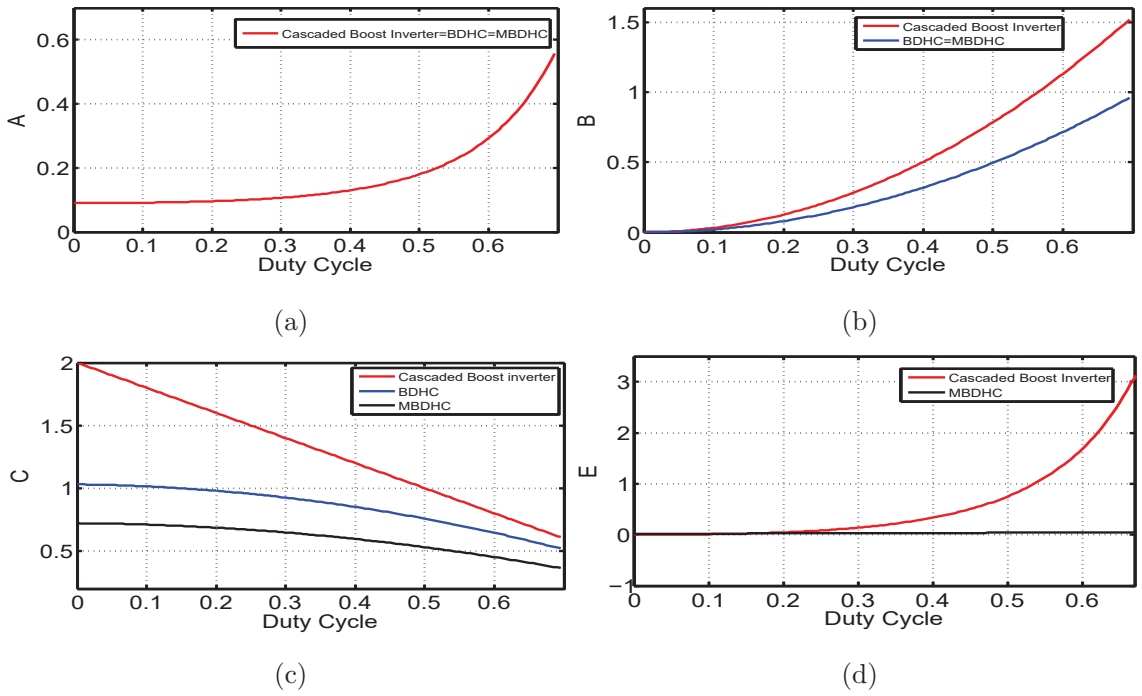


Figure 6.13: Loss factor variation with duty cycle

Table 6.2: MBDHC specification

Parameter	**Rating**
Total output Power P	635 W
AC output Power P_{AC}	269 W
DC output Power P_{DC}	366 W
Inductance L	1.12 mH
capacitance C	100 μF
AC load	10 Ω(4 A)
DC load	40 Ω(3 A)
AC Filter Inductance(L_f)	0.5 mH
AC Filter Capacitance(C_f)	10 μF
Input VoltageV_{in}	85 V
Carrier frequency	5 kHz

is

$$I_L = \frac{V_{dc}I_{dc} + 3V_{ac}I_{ac}\cos\phi}{V_{in}} \tag{6.22}$$

The inductor current is calculated for input voltage V_{in}=85 V, d=0.3 and m=0.675. From Equ-(6.22), the inductor current I_L is 7.47 A. Peak to peak ripple current is taken as $\Delta I_L = 0.3I_L$. For switching frequency of 10 kHz for boost stage, the value of inductor is calculated as

$$L = \frac{V_{in}d}{f_s \Delta I_L} \tag{6.23}$$

The inductor value as per the Equ-(6.23) is 1.14 mH while in this paper 1.12 mH inductor is used. The design of L plays an important role in NZ-DCM phenomenon. The Equ-(6.11) can be arranged as

$$\frac{1}{R_{dc}} + \frac{3m^2}{8R_{ac}} = J > \frac{m(1-d)}{2R_{ac}} + \frac{d(1-d)^2}{2f_sL} = J_{crit} \tag{6.24}$$

such that variables and constant terms can be separated. R_{ac} is per phase resistance. For fixed loading condition that is for fixed J, the effect of L with variation in duty cycle can be plotted. For better explanation, effect of L on the NZ-DCM is plotted in Fig-6.14. As the inductor increases, J_{crit} starts decreasing. This shifts the intersection point of J and J_{crit} towards left as shown in Fig-6.14. This means that NZ-DCM occurs at more lower duty when L is increased.

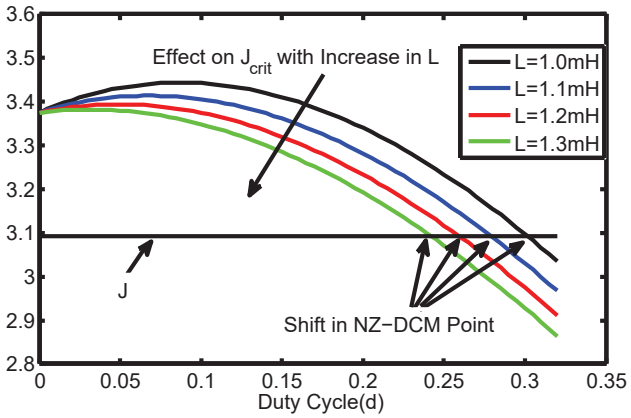


Figure 6.14: NZ-DCM shift with increase in L

6.5.2 Selection of capacitor for boost stage

The capacitor is designed as per ripple voltage in the output DC voltage. It is assumed that effective series resistance and effective series inductance is negligible, so the capacitor ripple is given as

$$\Delta V = \frac{I_o d}{f_s C} \tag{6.25}$$

where I_o is the average output current. For d=0.3 and m=0.675, the value of the output current(I_o) is 7 A. From Equ-(6.25), the value of the capacitor is 100 μF.

6.5.3 Switch stress analysis

Inverter switches are subjected to the boost voltage generated at the DC terminal. So the maximum voltage stress under which the switches operate, is equal to V_P. Similarly, diode D and antiparallel switch S is also stressed up to voltage V_P.

Table 6.3: Stress analysis of proposed converter

	Max Voltage Across Switch	**Max Current through Switch**
Inverter switches	$\frac{V_{in}}{1-d}$	$\|i_{ap}\| or\ \|i_{bp}\| or\ \|i_{cp}\| + i_{Lmax}$
Switch(S)	$\frac{V_{in}}{1-d}$	i_{Lmax}
Diode (D)	$\frac{V_{in}}{1-d}$	i_{Lmax}

The current stress in proposed converter is different from the cascaded boost inverter. The current through the inverter switches is equal to inductor current during shoot through while it is equal to the AC load current (i_a,or i_b, or i_c) during non shoot through period. So the maximum current(i_{inv}) which flows through the inverter switch is

$$i_{inv} = i_{L\max} + |i_{ap}| or\ |i_{bp}| or\ |i_{cp}| \tag{6.26}$$

where, subscript p denotes the peak value of corresponding current. $i_{L\max}$ is defined as

$$i_{L\max} = \frac{\Delta I_L}{2} + I_{Lavg} \tag{6.27}$$

The diode D is supplying the DC load with capacitance connected across it thus the current through D is i_d. Comprehensive switch stress in different modes is presented in Table-6.3. Moreover, comparative analysis among different topology is presented in Table-6.4.

Table 6.4: Comparison of proposed converter with existing converter

	Cascaded Boost VSI	**BDHC**	**MBDHC**
No. of switches	7	6	7
DC gain	$\frac{1}{1-d}$	$\frac{1}{1-d}$	$\frac{1}{1-d}$
Peak AC voltage	$\frac{mV_{in}}{1-d}$	$\frac{mV_{in}}{1-d}$	$\frac{mV_{in}}{1-d}$
Modulation index	$0 \leq m \leq 1$	$0 \leq m \leq 1$	$0 \leq m \leq 1-d$
Dual Output	Yes	Yes	Yes
Dead time	Yes	No	No
Max degree of freedom	2	2	2
NZ-DCM	Yes	Yes	No
Standalone AC	Possible	Not Possible	Possible
Capacitor life time	Very Poor	High	High
Efficiency	Moderate	High	High

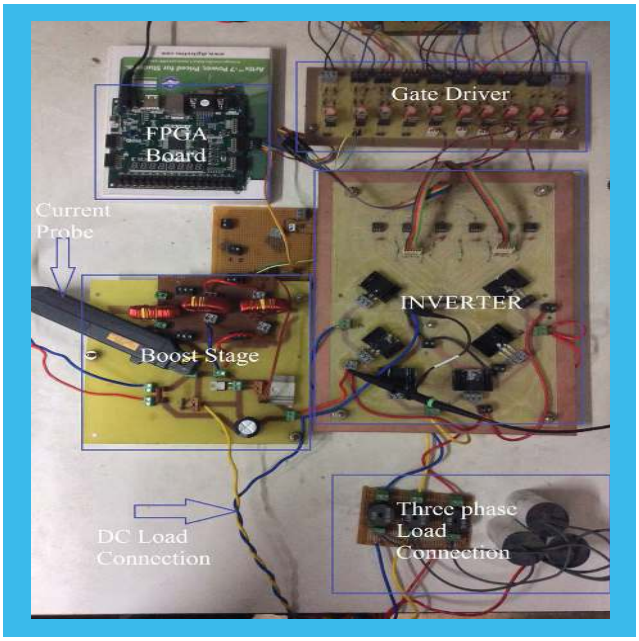


Figure 6.15: Experimental setup for MBDHC

6.6 Experimental results

For the specification enlisted in Table-6.2, a scaled down prototype of 635 W is designed and implemented to demonstrate the proof of concept as shown in Fig-6.15. Components used in the set up are listed in Table-6.5. For current measurement Agilent probe(N2782B) is used while for voltages measurement Tektronix make probes are used. The distribution among AC and DC power is 269 W AC and 366 W DC, respectively. Experimental results have voltage spikes during NZ-DCM/FCCM due to reverse recovery phenomenon of diode, parasitic circuit elements and switching of the antiparallel switch.

Table 6.5: Components used

Component	**Manufacturer**	**Model No.**	**Rating**
MOSFET	Semiconductor Tech.	STW10WK60Z	600V, 10A
Diode	Fairchild	ISL9R1560G2	600V, 15A
Capacitor	Multicomp	MCKSK400M101K32S	400V, 100μF
Inductor	Coilcraft	PCV-2-564-082	7A, 560μH

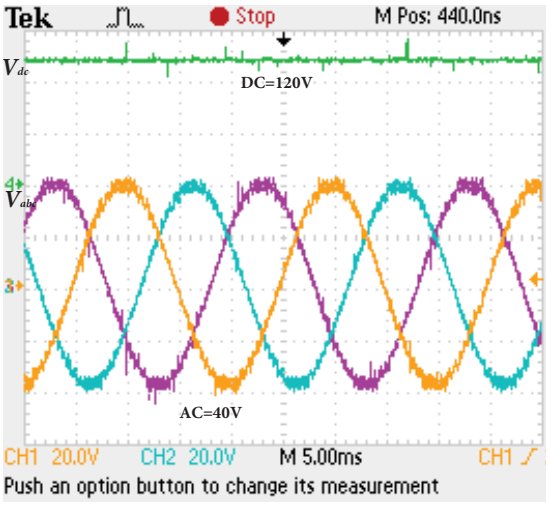


Figure 6.16: CCM of BDHC: DC and AC voltage [$Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div$]

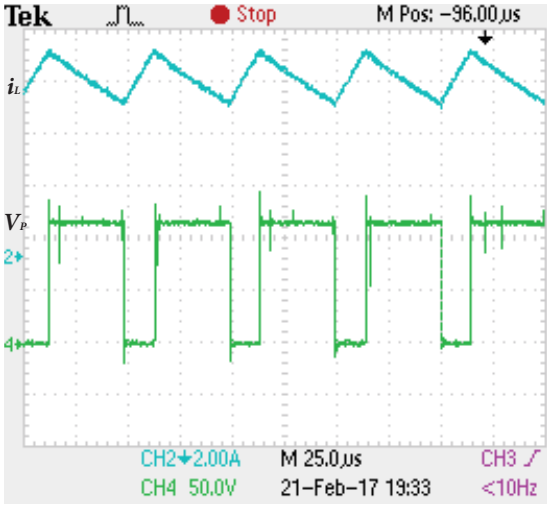


Figure 6.17: CCM of BDHC: DC link voltage and inductor current $[Ch2 : 2A/div, Ch4 : 50V/div]$

6.6.1 Simultaneous AC and DC load in CCM

To evaluate performance in this region, the DC load is 40 Ω and AC load per phase resistance is 10 Ω. The modulation index is 0.675 and duty cycle kept at 0.3. In this condition as per Equ-(6.12), $\xi > \chi$ (i.e. $3 > 2.28$), which is true. This ensures that condition for continuous conduction is valid. Fig-6.16 shows the results for simultaneous DC and AC output under CCM. The output voltage at DC link is stiff and AC voltage profile is smooth waveform. Moreover, DC and AC voltage is equal to theoretical value of 121 V and 40 V, respectively. The zoomed waveform for the dc link voltage and inductor current are shown in Fig-6.17. The inductor current is triangular in nature and no voltage dip is observed in DC link voltage. Moreover, THD in AC voltage is lower. Hence, in CCM, the converter performance is better in terms of voltage stress across capacitor and switch, efficiency and THD.

6.6.2 Simultaneous AC and DC load in NZ-DCM

To identify the inefficacy of BDHC to operate under NZ-DCM, the DC load is varied till 70 Ω while AC load is fixed at 10 Ω . This means that AC load in NZ-DCM becomes higher than the CCM. The duty cycle and modulation index are same as CCM. This makes $\xi < \chi$ (i.e. $1.72 < 2.28$), which is true. This violates the condition for CCM and pushes BDHC in NZ-DCM as indicated by the AC and DC output voltage profile in

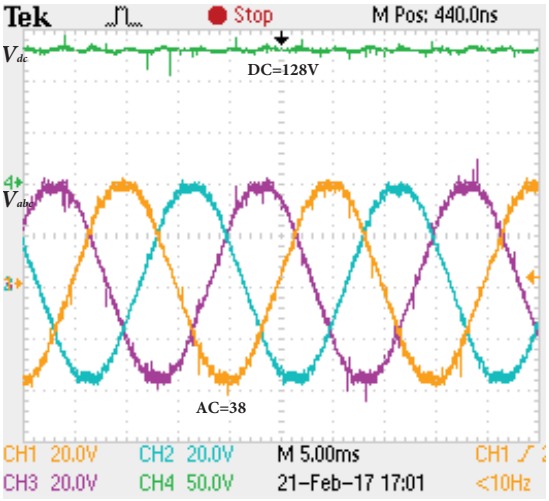


Figure 6.18: NZ-DCM of BDHC: DC and AC voltage $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

Fig-6.18. Significant distortion in the voltage would result in adverse effect on load. The DC ripple voltage becomes high and AC waveform starts deteriorating. Moreover, the DC mean voltage becomes higher than the expected i.e. 128 V while AC voltage observes a dip in peak voltage i.e. 38 V. Likewise from Fig-6.19, it is seen that inductor current saturate for a small time and this effect is propagated to the dc link voltage, indicated by dip in DC link voltage. This effect further worsens at lower duty cycle. Therefore, it is not suitable to operate converter in NZ-DCM when operated under lower duty cycle due to high voltage stress, higher THD and lower efficiency. .

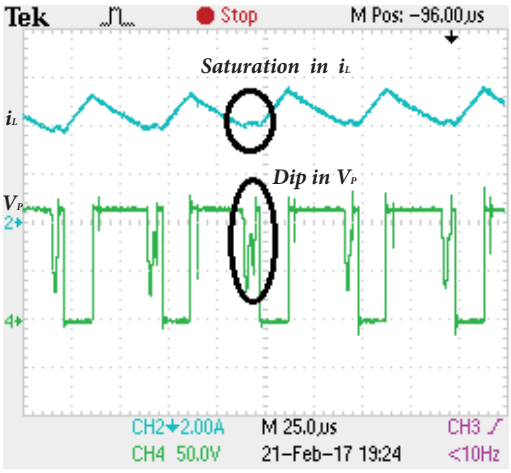


Figure 6.19: NZ-DCM of BDHC: DC link voltage and inductor current $[Ch2 : 2A/div, Ch4 : 50V/div]$

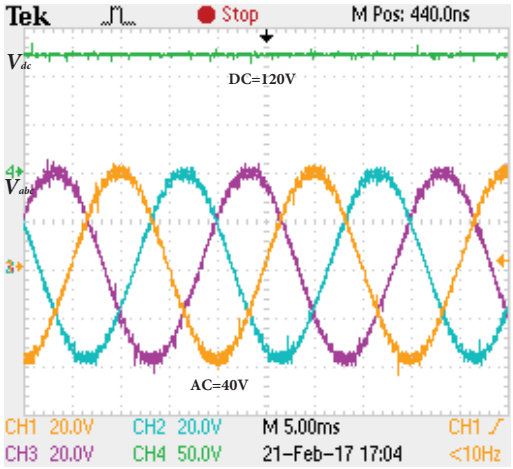


Figure 6.20: FCCM of MBDHC: DC and AC voltage $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

6.6.3 Modified BDHC for simultaneous AC and DC voltage in FCCM

This mode is achieved by connecting an antiparallel switch across the diode. The turn ON of switch S redeem NZ-DCM to FCCM. The DC voltage has less amount of ripple, as shown in Fig-6.20, and returns to its normal value i.e.120 V. Moreover, AC voltage becomes equal to expected value. In Fig-6.21, it is noticeable that the inductor current is continuous in nature and no voltage dip is observed in DC link voltage. The voltage stress across the capacitor and inverter switch is reduced. Furthermore, THD is also reduced. Therefore, in FCCM, the behaviour of the converter is similar to CCM.

In case of simultaneous AC and DC load, the THD as a function of duty ratio is shown in Fig-6.22a and corresponding ripple voltage is presented in Fig-6.23a. For BDHC, both THD and ripple voltage is quite significant during DCM (12% THD and 25% ripple for $d = 0.2$). The proposed MBDHC or FCCM improves the THD (shown in Fig-6.22b) and output ripple voltage (1.2% THD and 1.8% ripple for $d = 0.2$) (Fig-6.23b) to an extent which is very less as compared to the THD and ripple output voltage introduced by the conventional BDHC under NZ-DCM.

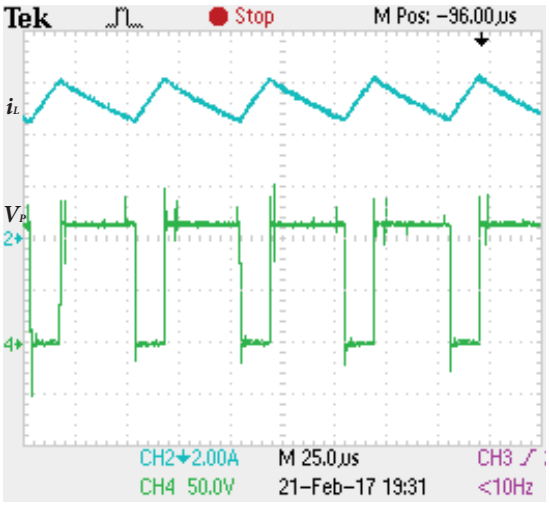
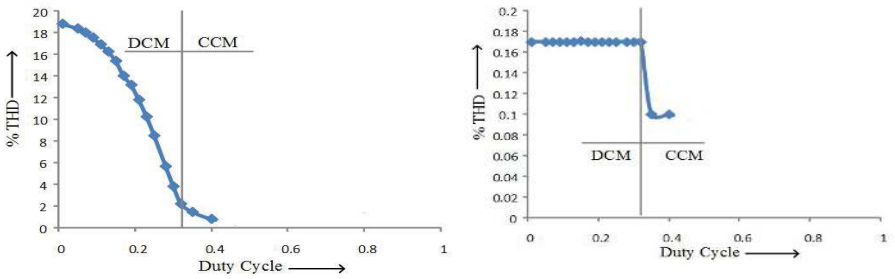
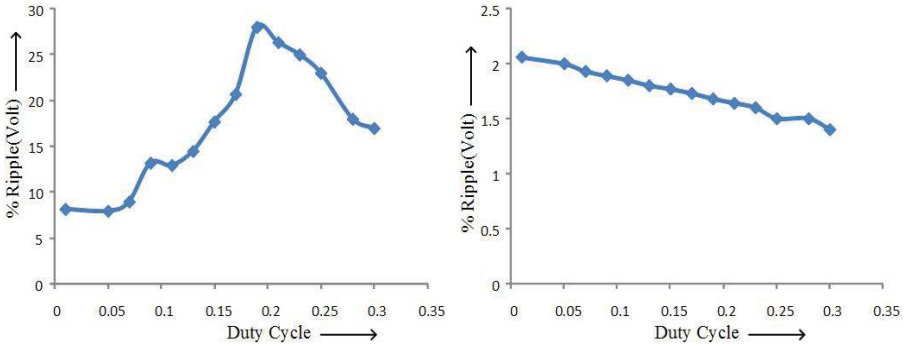


Figure 6.21: FCCM of MBDHC: DC link voltage and inductor current $[Ch2 : 2A/div, Ch4 : 50V/div]$



(a) THD in DCM (b) THD in FCCM

Figure 6.22: THD variation in AC voltage with duty cycle $m = 0.6$



(a) Ripple in voltage for DCM (b) Ripple in Voltage for FCCM

Figure 6.23: Percent ripple in DC voltage at $m = 0.6$

6.6.4 AC standalone operation

For AC standalone operation, the DC load is disconnected, diode and capacitance remain in the circuit for conventional BDHC. The converter does not operate satisfactorily and output voltage is very less than the expected value. The dc link voltage consists high voltage spikes and the three phase voltage is totally distorted as shown in Fig-6.24 which means that quite THD is present in AC voltage. Moreover, high voltage spikes may damage the inverter switches. Therefore, this mode is not feasible in BDHC.

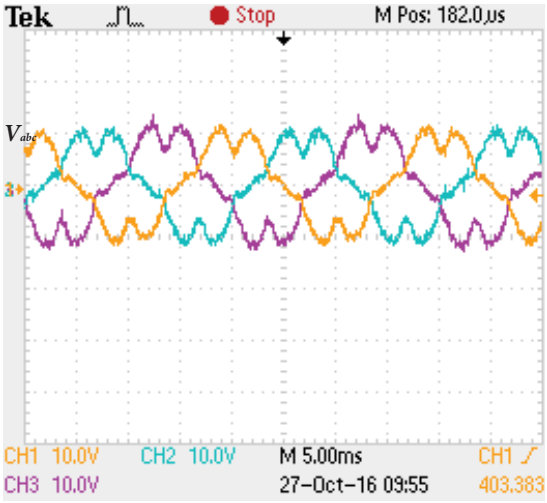


Figure 6.24: Unstable operation of BDHC for standalone AC load [$Ch1 : 10V/div, Ch2 : 10V/div, Ch3 : 10V/div$]

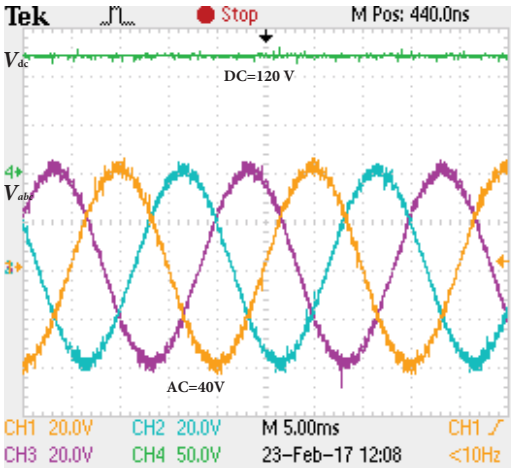


Figure 6.25: Standalone AC operation: DC and AC voltage [$Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div$]

Fig-6.25 presents the AC voltage and capacitor voltage for MBDHC. During standalone AC operation, it is observed that system is perfectly stable, which otherwise is not possible without having a complementary switch which has lower THD. Moreover, the DC voltage has no dips and inductor current profile is continuous in nature (Fig-6.26) along with lower voltage spikes. Therefore, MBDHC is suitable candidate for standalone operation.

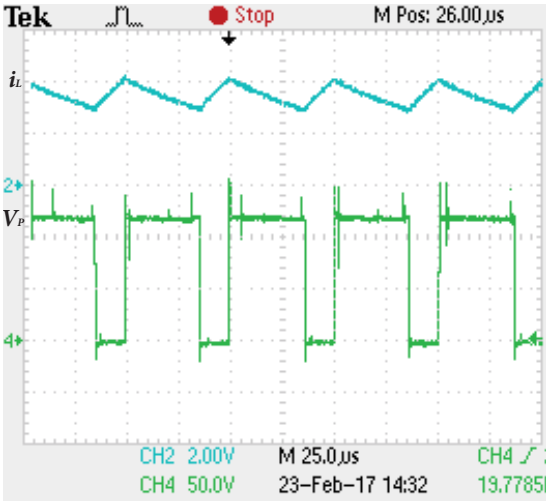


Figure 6.26: Standalone AC operation: DC link voltage and inductor current [$Ch2$: $2A/div, Ch4 : 50V/div$]

6.6.5 DC standalone operation

For this test, the AC load is disconnected and only switches of the inverter are used for the purpose of shoot-through. DC load voltage, DC link voltage and inductor current are observed to ensure the stability and CCM operation of the converter as shown in Fig-6.27. The inductor current is continuous in nature and DC link voltage has no distortion. This operation is similar to Boost converter. Therefore, a hybrid converter may be served as independent DC-DC boost converter.

6.6.6 Experimental efficiency

Experimental efficiency is conducted for the prototype. The measurement of AC and DC power is done using power analyser(YOKOGAWA-WT300E). Fig-6.28a shows the efficiency for variation in modulation index keeping duty cycle constant. Efficiency of

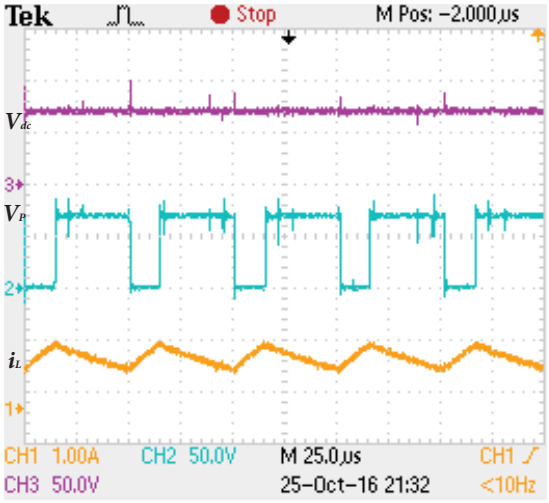
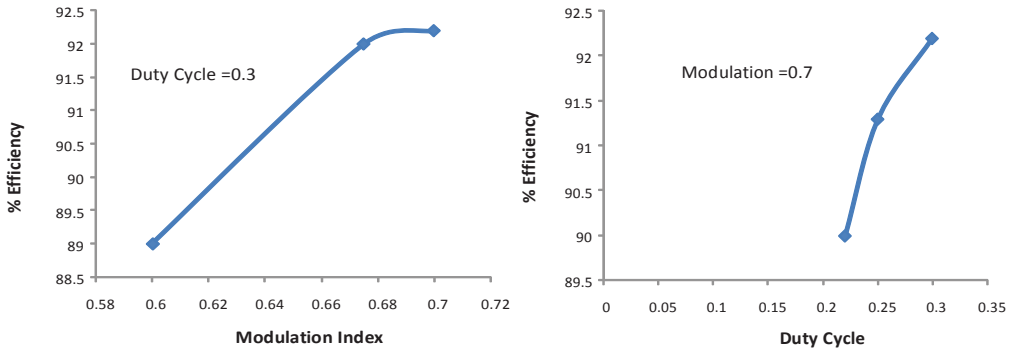


Figure 6.27: Experimental results for standalone DC operation $[Ch1 : 1A/div, Ch2 : 50V/div, Ch3 : 50V/div]$

the system depends on the losses present in the converter. Two kind of losses exists in the converter: fixed losses(due to inductor core and device switching loss), and variable loss (due to the parasitic resistance of capacitor and inductor, and switches on state resistance). At low power output, these losses contribute higher percentage as compared to high power output. At low modulation index, the losses were higher so efficiency is relatively low i.e. 89% at $m = 0.6$. With higher modulation index of $m = 0.7$, the efficiency is proved to be 92%.



(a) With modulation index (b) Variation with duty cycle

Figure 6.28: Experimental efficiency

Similarly, for constant modulation index of $m = 0.7$, the variation in efficiency is plotted with duty cycle as shown in Fig-6.28b. At low duty cycle efficiency is low while

it increases as duty cycle is increased.

6.7 Conclusion

Analytical study of the BDHC is presented in this paper. The derived boundary condition between CCM and NZ-DCM suggests that low duty ratio($d < 0.3$) combined with high AC load saturates the inductor current. This leads to aberrated operation of BDHC. It introduces huge dips in the DC link voltage, that further leads to poor ripple voltage and THD. The standalone AC operation becomes unstable for BDHC. To suppress the limitation of BDHC, an extra antiparallel switch across diode is connected. The MBDHC works well with the established simple boost control strategy improving the performance of the hybrid converter in terms of extended load variations and improved THD. Though the efficiency of MBDHC is lower than BDHC and better than cascaded boost inverter, the significant improvement in terms of THD and load variation are its strong figure of merits.

Modified BDHC can function properly in wider duty cycle variation, however, gain is limited. In the subsequent chapter, hybrid L-ZSI will be presented to increase the gain. The converter will be analyzed in DCM to enhance the gain of the converter. The proposal will be validated in experiment.