Chapter 3

Modified Switched Boost Inverter For wide Duty Cycle Operation

3.1 Introduction

The Z-source converter [56] since its inception is quiet popular in power electronic research community. A few of its salient features include single stage conversion, wide range of load regulation, no dead time requirement and immunity to EMI. The prime motive of the various derived topologies is the huge gain, reduced count of circuit elements and minimum stress [107]. Z-source converter has following operating states- active, shoot-through and zero. The profile of the inductor current during these states broadly define whether the converter operates in CCM or DCM. Unlike established CCM and DCM, a peculiar constant inductor current phenomenon occurs which is responsible for non-zero discontinuous mode (NZ-DCM) in the certain Z-source converter.

The converters containing NZ-DCM in their operation have a common feature, i.e., during active or zero states, a diode in series with a capacitor is connected parallel across the inverter. Due to a specific arrangement of circuit elements, NZ-DCM appears, keeping the inductor current almost constant up to the next zero state. The NZ-DCM creates the potential threat to stiff DC link voltage resulting in higher THD at AC load terminal. This effect further degrades the performance of the load. To demonstrate NZ-DCM, switched boost inverter(SBI) is selected which has aforementioned feature to have NZ-DCM. However, this theory can be extended to other Z-source converters.

The SBI is operated for high AC load current along with low duty cycle condition.

This combination of load and duty cycle, makes the inductor current to saturate at AC load current. This effect creates two level of voltage at VSI input that leads to distortion in AC voltage. Moreover, the voltage at DC link is much higher while peak AC output is lower than expected. To avoid undesirable condition in SBI, modified SBI is proposed which operates under wide range of varying load and duty cycle conditions. The main contributions of this work is to investigate:

1) Possible operating modes of SBI which was not reported earlier
2) Limitation of the converter
3) Impact of low duty cycle on converter performance
4) Solution to the existing problem for wide range of duty variation.

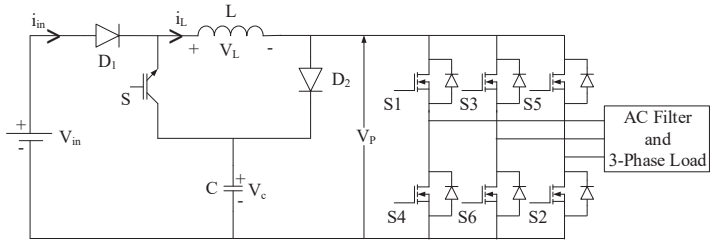


Figure 3.1: Conventional SBI topology

3.2 Operation of the SBI and its limitation

3.2.1 Operation

The conventional SBI configuration, as shown in Fig-3.1, consists only one capacitor and inductor. Unlike three states reported earlier [66], SBI has four states of operation. These states are explained in the following subsections.

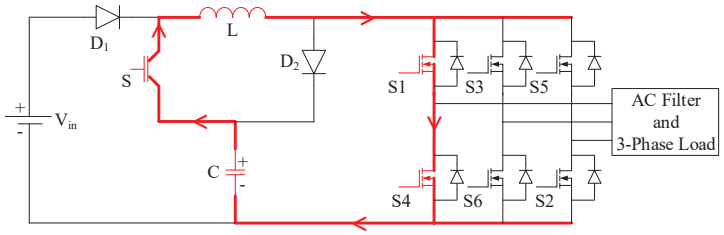


Figure 3.2: Shoot through state

Shoot through state

Shoot through state(ST) is brought into the circuit by applying the ST pulses to the switch S and one leg of the inverter(Fig-3.2). During this period, inductor current has positive slope. This causes the voltage across L (V_L) to become positive which makes D_2 reverse biased. Capacitor voltage(V_c) is higher than the input voltage(V_{in}), due to boosting nature of the converter, which reverse biases diode D_1. Moreover, the inductor is charged through the V_c instead of V_{in}. Therefore, SBI requires lower duty cycle as compared to conventional boost converter, to achieve the same gain. The ST period is equal to dT_s.

Active state 1

In active state 1 as shown in Fig-3.3, the switch S is turned off by applying non shoot through (NST) pulses. During this period inductor current slope is negative and V_L becomes negative. Thus, V_{in}-V_L is positive thereby diode D_1 is forward biased. The inductor freewheels through the load in series with the source. Moreover, $(V_L + V_{in})$ - V_c is positive letting the diode D_2 to be forward biased. Capacitor C is charged to V_L+ V_{in} through D_2. active state 1 duration is part of $(1-d)T_s$.

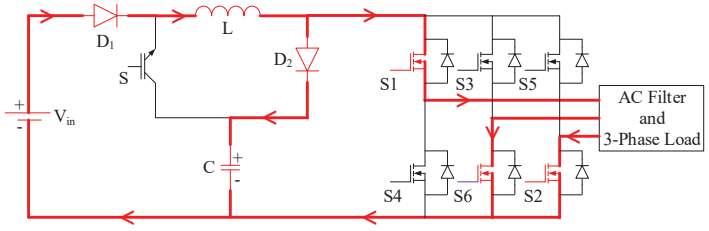


Figure 3.3: Active state 1

Zero state

Simultaneous turning on the upper half or lower half of inverter legs bring the converter into zero state, as shown in Fig-3.4. The load is separated from the source and voltage across the load is maintained by AC filter capacitor C_f. The source voltage is directly connected to the capacitor and load freewheels through the freewheeling diodes of the inverter. Duration corresponding to this state is governed by ST and active state .

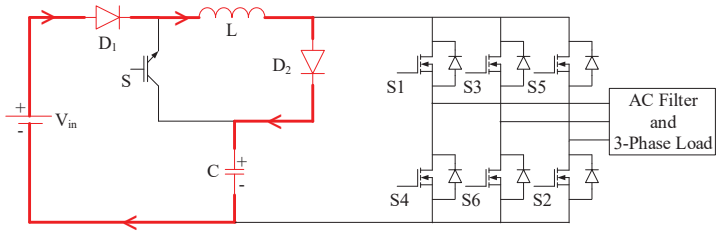


Figure 3.4: Zero state

Active state 2

This state comes soon after the active state 1. As soon as load current becomes equal to the inductor current, the converter enters into active state 2. In this mode, the inductor tries to saturate at the load current and becomes constant, instead of linearly decreasing. This state exhibits the zero voltage drop across the inductor($V_L = 0$) therefore voltage source is incapable to forward bias the diode D_2 i.e $V_{in} + V_L < V_c$. The diode D_2 is open circuited, restricting the flow of current into the capacitor C. This causes capacitor(C) terminal to be open circuited which let the inductor to be switched between the load and source at switching frequency leading to voltage spikes. Fig-3.5 shows this state, during which the diode D_2 and switch S is open circuited while diode D_1 conducts.

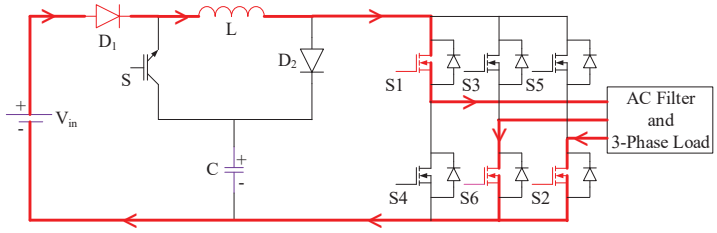


Figure 3.5: Active state 2

3.2.2 Steady state analysis

For analyzing the limitation of the existing converter, its steady state analysis is done. In this analysis, it is assumed that the inductor charges and discharges linearly. The relevant waveforms for its analysis are shown in Fig-3.6. G_s is pulse for the shoot through duration.

3.2.3 Inductor ripple current calculation:

From time 0 to T_1, the inductor charges through the capacitor voltage and corresponding equation is written as

$$V_c = L\frac{\Delta I_L}{T_1} \tag{3.1}$$

or

$$T_1 = \frac{L\Delta I_L}{V_c} \tag{3.2}$$

Similarly, from time T_1 to T_2, the inductor discharges i.e.

$$V_{in} - V_c = -L\frac{\Delta I_L}{T_2} \tag{3.3}$$

or

$$T_2 = -\frac{L\Delta I_L}{V_{in} - V_c} \tag{3.4}$$

where V_c is the voltage across capacitor and ΔI_L is peak to peak ripple current.

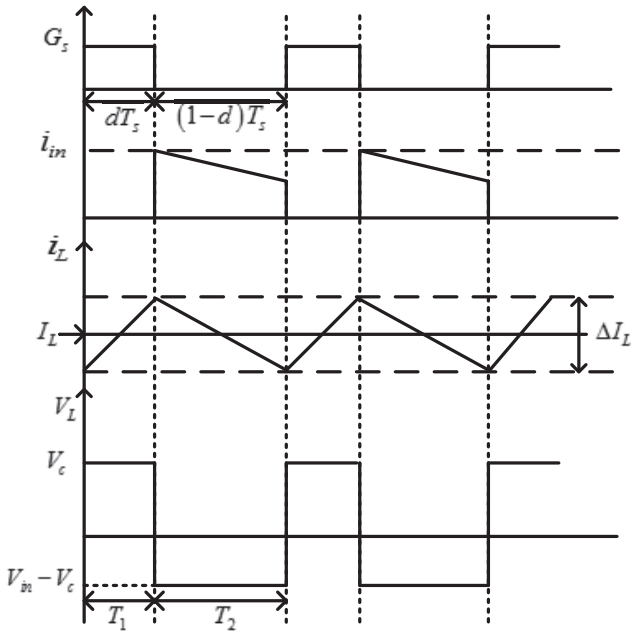


Figure 3.6: Steady state waveform

The peak to peak ripple current from both expressions must be equal and it can be written as

$$\Delta I_L = \frac{V_c T_1}{L} = \frac{(V_c - V_{in})T_2}{L} \tag{3.5}$$

this results in gain expression

$$\frac{V_c}{V_{in}} = \frac{1-d}{1-2d} \tag{3.6}$$

Therefore, DC link voltage of the converter is expressed as

$$V_P = V_c = \frac{1-d}{1-2d} V_{in} \tag{3.7}$$

For three phase inverter, peak AC voltage is given as

$$v_{ac} = \frac{mV_P}{2} \tag{3.8}$$

where m is the modulation index.

The switching period of the converter is given as

$$\begin{aligned} T_s &= T_1 + T_2 \\ &= \tfrac{L\Delta I_L}{V_c} + \tfrac{L\Delta I_L}{V_c - V_{in}} \end{aligned} \tag{3.9}$$

Thus, peak to peak ripple current given as

$$\Delta I_L = \frac{V_c(V_c - V_{in})}{f_s(2V_c - V_{in})L} \tag{3.10}$$

where f_s is switching frequency and given as $T_s = \frac{1}{f_s}$.

The current ripple in terms of duty cycle from Equ-(3.6) and Equ-(3.10) is written as

$$\Delta I_L = \frac{(1-d)d}{f_s(1-2d)L} V_{in} \tag{3.11}$$

where $0 < d < 0.5$

Equ-(3.11) suggests that I_L is dependent on the switching frequency(f_s) , boosting inductor(L) and duty cycle(d). For fixed input voltage, lower ripple current is achieved by either higher L or f_s or both. The inductor ripple current ΔI_L has a vital impact on the operation of the SBI, especially during low duty cycle operation.

3.2.4 Design of capacitor

VSI requires constant input voltage for its proper operation. Therefore, variation in input voltage is directly linked the output quality in terms of THD. During active states of the inverter, the capacitor acts as voltage source for the inverter. To produce constant voltage across capacitor, the voltage ripple should be minimum. The capacitor has to handle inductor current during shoot through period therefore maximum current through the capacitor is equal to I_L. Hence, the capacitor is designed based on the inductor current and calculated as

$$C\frac{\Delta V}{dT_s} = I_L \tag{3.12}$$

In this paper, voltage ripple is considered as 1% of capacitor voltage. As per Equ-(3.12), for d=0.25 and T_s=0.1 ms, the capacitance is given as 87 μF. Due to availability, 100 μF capacitor is used in this work.

3.2.5 Design of inductor

For calculation of L, average inductor current is required.

From Fig-3.6, input current is given as

$$\begin{aligned} i_{in} &= 0 \quad for \quad 0 < t < dT_s \\ i_{in} &= i_L \quad for \quad dT_s < t < T_s \end{aligned} \tag{3.13}$$

So, over a switching period, I_{in} is written as

$$I_{in} = (1-d)\, I_L \tag{3.14}$$

where I_{in} and I_L are average input and inductor current, respectively. From power balance theory

$$V_{in} I_{in} = 3 V_{ac} I_{ac} \cos\Phi \tag{3.15}$$

where V_{ac} and I_{ac} are rms quantities.

$$I_{in} = \frac{3 V_{ac} I_{ac} \cos\Phi}{V_{in}} \tag{3.16}$$

Substituting the value of I_{in} from Equ-(3.14) in Equ-(3.16)

$$I_L = \frac{3 V_{ac} I_{ac} \cos\Phi}{(1-d)\, V_{in}} \tag{3.17}$$

For V_{in} = 70 V and duty cycle of 0.25, using Equ-(3.17), I_L=7 A for 367.5 W rating of the converter. In this paper, ΔI_L is considered as ΔI_L=0.33I_L. So, from Equ-(3.11), L is equal to 1.12 mH. However, when duty cycle is changing, this value of inductor fails to keep ripple current constant. Hence, the effect of change in ΔI_L need to be addressed. This effect causes three modes of operation 1) CCM 2) NZ-DCM 3) DCM. The DCM occurs only when the inductance value is quite low such that inductor current reaches to zero, before next shoot through period. The designed inductor L=1.12 mH above is sufficient enough to avoid DCM. Remaining two modes are explained as follows:

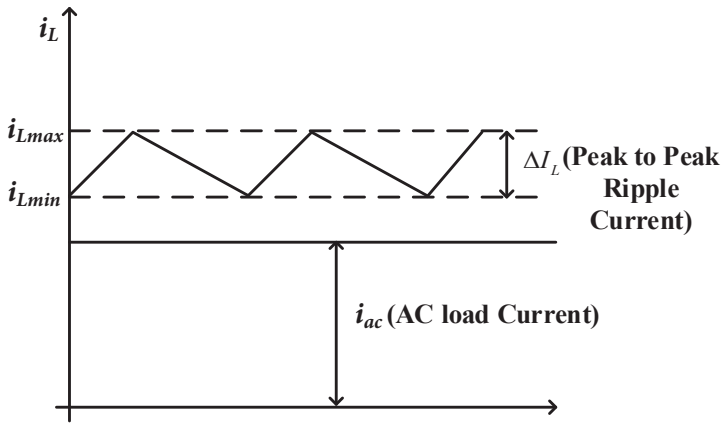


Figure 3.7: CCM for SBI

CCM analysis

In case of higher duty cycle operation, the current drawn from the source is large in magnitude during charging of the inductor, correspondingly ΔI_L(as per Equ-(3.11)) will be large. The nature of the current during CCM is shown in Fig-3.7. During this mode the boosted voltage serves as source for the inverter. Due to large inductor current at this duty cycle, the peak AC load current(i_{ac}) never intersects the inductor current i_L as shown in Fig-3.7. Therefore,

$$i_{L\,\min} - i_{ac} > 0 \tag{3.18}$$

or

$$I_L - \frac{\Delta I_L}{2} - i_{ac} > 0 \tag{3.19}$$

or

$$i_{ac} < \left(I_L - \frac{\Delta I_L}{2} \right) \tag{3.20}$$

If this relation holds, diode D_2 remains forward bias in the converter. That is capacitor C remains connected across the inverter maintaining constant voltage across it. Thus the profile of inductor current is triangular in nature.

NZ-DCM analysis

During low duty cycle operation, boosting of capacitor voltage V_c(as per Equ-(3.6)) is low. To boost this voltage, average inductor current falls according to Equ-(3.17). So, from Equ-(3.11) ΔI_L also decreases. For constant AC load resistance, AC load current

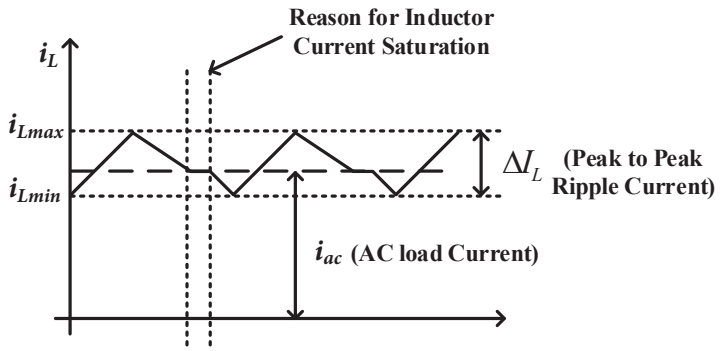


Figure 3.8: NZ-DCM for SBI

decreases correspondingly. At this point of operation, the fall in inductor current is higher than decrease in AC load current. Hence peak AC load current(i_{ac}) intersects inductor current(i_L). Due to this, during charging, i_L increases linearly while during discharging, instead linearly decreasing, i_L tries to saturate at i_{ac} as shown in Fig-3.8. Mathematically, it follows

$$i_{L\min} - i_{ac} < 0 \tag{3.21}$$

or

$$I_L - \frac{\Delta I_L}{2} - i_{ac} < 0 \tag{3.22}$$

By re-arranging

$$i_{ac} > \left(I_L - \frac{\Delta I_L}{2} \right) \tag{3.23}$$

As soon as Equ-(3.23) becomes valid, inductor current intersects the AC load current and tries to saturate at the level of load current. This produces zero voltage drop across the inductor i.e. $V_L = L\frac{di_L}{dt} = 0$. Since $V_c > V_{in}$, D_2 is reversed biased and hence capacitor C is un-clamped. The following adverse effects are created due to this mode:

1) Dip in DC link voltage reduces the peak AC load voltage

2) The capacitor voltage is higher than the expected due to un-clamping of capacitor: During NZ-DCM, the capacitor is disconnected and inductor current is constant in nature. Therefore, the voltage across inductor become zero during NZ-DCM. If the NZ-DCM period is represented by duty cycle d_1, then voltage across inductor during different interval is given as

$$\begin{aligned} V_L &= 0 && 0 \leq t < d_1 T_s \\ V_L &= V_c && 0 \leq t < dT_s \\ V_L &= V_{in} - V_{dc} && 0 \leq t \leq (1-d-d_1)\, T_s \end{aligned} \tag{3.24}$$

Applying averaging principle across inductor over a period results in

$$dV_c + (1-d-d_1)\,(V_c - V_{in}) = 0 \tag{3.25}$$

Simplifying the above equation, the average voltage across capacitor is

$$V_c = \frac{1-d-d_1}{1-2d-d_1} V_{in} \tag{3.26}$$

For analysis purpose, the voltage across capacitor in NZ-DCM is represented by V_{nzc} instead of V_c. Therefore, expression for voltage across capacitor is represented as

$$V_{nzc} = \frac{1-d-d_1}{1-2d-d_1} V_{in} \tag{3.27}$$

3) From Equ-(3.27), it is concluded that capacitor undergoes high voltage stress at lower duty cycle i.e higher capacitor rating is required.

4) Higher THD across AC load terminal

To overcome the above mentioned problem, it is required that average value of inductor current and inductor current ripple satisfy Equ-(3.20). For this, inductor and switching frequency are the two possible design parameters.

Effect of change in L or f_s on NZ-DCM:

To show the effect of L and f_s on NZ-DCM, Equ-(3.23) is transformed.

Peak AC load current

$$i_{ac} = \frac{mV_P}{2R_{ac}} \tag{3.28}$$

So using Equ-(3.11), Equ-(3.17) and Equ-(3.28), Equ-(3.23) is written as

$$\frac{mV_P}{2R_{ac}} > \frac{3V_{ac}I_{ac}\cos\Phi}{(1-d)\,V_{in}} - \frac{(1-d)\,d}{2f_s\,(1-2d)\,L} V_{in} \tag{3.29}$$

Substituting the value of V_P from Equ-(3.7) , $V_{ac} = \frac{mV_P}{2\sqrt{2}}$, and $I_{ac} = \frac{mV_P}{2\sqrt{2}R_{ac}}$, following expression is obtained

$$3m^2 < 4m\,(1-2d) + \frac{4d\,(1-2d)\,R_{ac}}{f_s L} \tag{3.30}$$

$$K < K_{crit} \tag{3.31}$$

where $K = 3m^2$ and $K_{crit} = 4m\,(1-2d) + \frac{4d(1-2d)R_{ac}}{f_s L}$

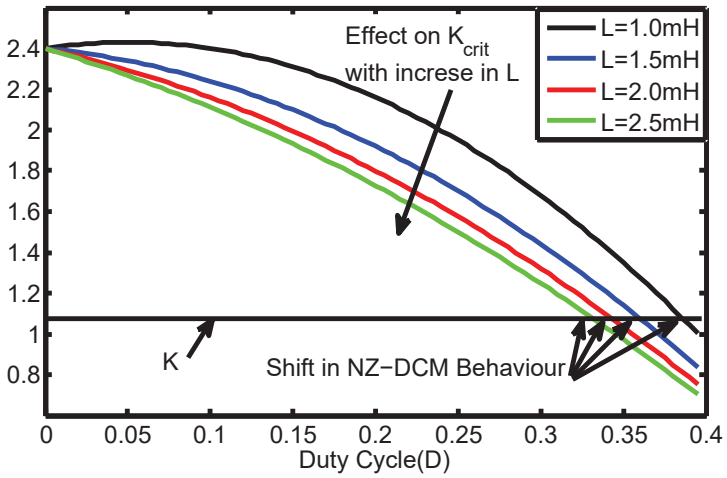


Figure 3.9: Shift in NZ-DCM with L variation

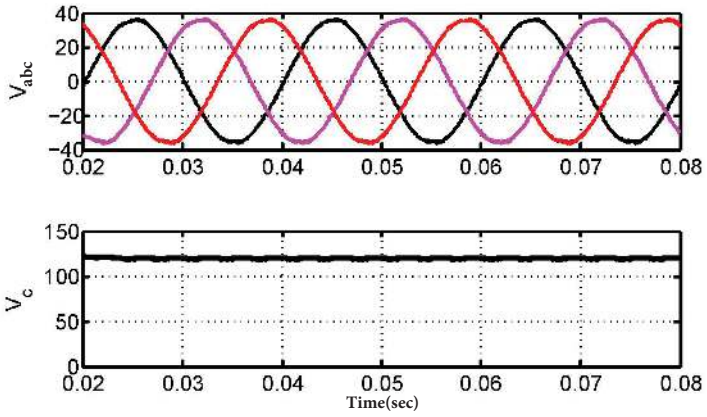


Figure 3.10: a) AC voltage b) DC voltage

With increase in L, the effect on K_{crit} is shown in Fig-3.9. As the K_{crit} move downwards, the intersection of K and K_{crit} shift towards left and hence NZ-DCM region also shifts left. This implies that for higher L, NZ-DCM occurs at relatively lower duty cycle. But for large change in L, very small shift in intersection point is observed. Therefore, to eliminate NZ-DCM, a high value of inductance is required. The inductance corresponding to the boundary condition between CCM and NZ-DCM is known as critical inductance(L_c) which is mathematically given as

$$L_c = \frac{4d\,(1-2d)\,R_{ac}}{[3m^2 - 4m\,(1-2d)]\,f_s} \tag{3.32}$$

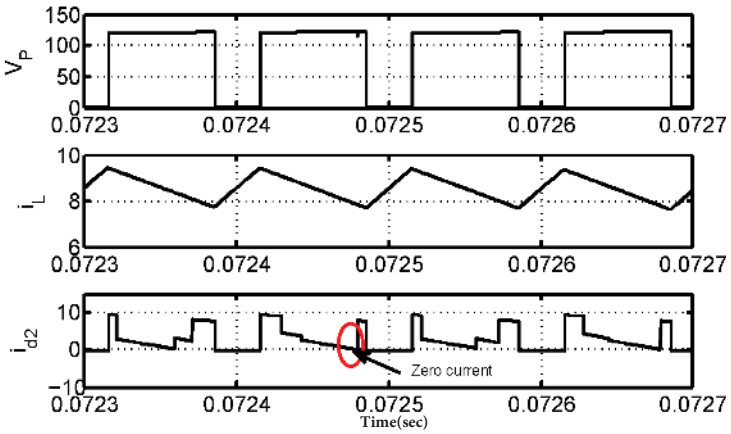


Figure 3.11: a) DC link voltage b) Inductor current c) Diode current

At d =0.3, m=0.6, R_{ac}=5 Ω /phase and f_s=10 kHz, the value of L_c is equal to 2 mH. The AC voltage and DC voltage are same as for CCM as shown in Fig-3.10. The inductor current is triangular in nature along with no dip in DC voltage. However, the diode current(D_2) touches zero value, as shown in Fig-3.11. This indicates that the converter is at the verge of CCM and NZ-DCM. Therefore, low duty cycle problem can be avoided at the cost of larger value of the inductor which is impractical from the view point of weight and size . In addition, it increases the cost of the converter. On the other hand, higher switching frequency converters require high speed power devices which in turn increases the cost of the converter. Due to these limitations, an alternative method was adopted to propose a new modification to the conventional SBI.

3.3 Proposed converter and its Operation

The proposed SBI configuration has one extra switch which is placed antiparallel across the diode D_2. This allows the flow of current through itself, thereby capacitor does not observe any discontinuous operation. The proposed modified topology for SBI(PSBI) is shown in Fig-3.12. The basic operation of the PSBI consists of various states as described in section-II. Shoot through state, active state 1 and zero state are similar to the conventional SBI. But the fourth state in the PSBI is completely different from the conventional SBI, and explained below

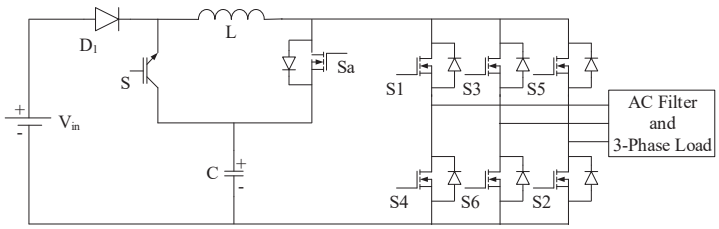


Figure 3.12: Proposed SBI configuration

3.3.1 Modified active state 2

This state is triggered only when the switch Sa is turned on by providing the non shoot through pulses. In conventional SBI, the diode D_2 and switch S are off during active state 2, inhibiting the flow of current into the capacitor, which was the reason for aberrant behaviour. In PSBI, the flow of the current through the capacitor path is assisted by the switch S_a. As soon as AC load current acquires the value equal to the inductor current($i_L = i_{ac}$), V_L becomes zero and capacitor voltage(V_c) acquires value higher than the input voltage(V_{in}). This reverses biases the diode D_2 and simultaneously forward biases the switch S_a. By applying the NST pulses, the switch S_a is turned on which assist the flow of current in the reverse direction. Capacitor supplies excessive stored energy back to the load through switch S_a and it is connected across the inverter. Thus constant voltage appears across inverter. The mode corresponding to this state is referred as forced continuous current mode(FCCM). The operation is depicted in Fig-3.13.

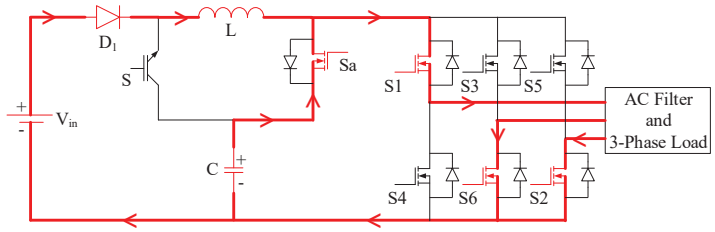


Figure 3.13: Modified active state 2

This modification results in the following advantages

1) Stiff DC link voltage

2) Capacitor voltage equal to the boosted voltage

3) Lower stress across the capacitor

4) Better performance of AC load in terms of THD

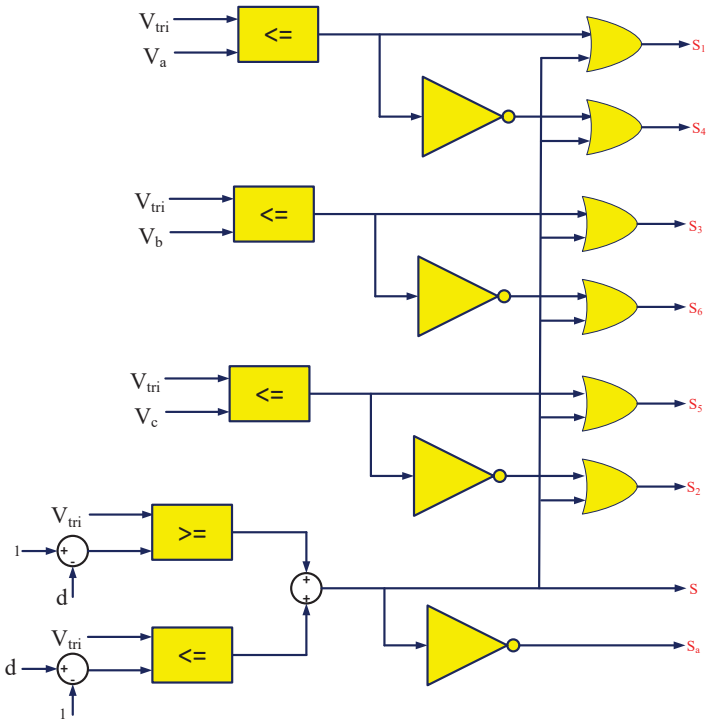


Figure 3.14: Logic diagram for control pulses

3.4 PWM control pulses of proposed converter

Control pulses of the proposed converter is derived from the simple boost control strategy [113]. The schematic of control logic for generation of pulses is presented in Fig-3.14. Moreover, the generated control pulses are shown in Fig-3.15. Generation of pulses is done in two steps: First, PWM for VSI is generated by comparing three phase sinusoidal pulses(V_a, V_b and V_c) with the triangular pulse(V_{tri}). The frequency of the triangular signal(f_s) must be very much higher than sinusoidal signal(f). The generated pulses have active and zero states. Secondly, for boost control, the generation of shoot through is done by comparing positive and negative DC quantities ($\pm V_s$), with the same triangular pulses as used for the three phase PWM inverter pulse generation. These shoot through pulses are placed in zero states of the inverter. The gate control signals for the converter are obtained using the following logical expression as

$$S_1 = G_1 \oplus ST, S_4 = \bar{G}_1 \oplus ST, S_3 = G_2 \oplus ST$$

$$S_6 = \bar{G}_2 \oplus ST, S_5 = G_3 \oplus ST, S_2 = \bar{G}_3 \oplus ST$$

Moreover, the switch S is controlled directly by shoot through(ST) pulses, while switch S_a is controlled by non shoot through(NST) pulses.

Mathematically, the triangular waveform is written as

$$V_{tri} = \begin{cases} -\frac{V_m}{T_s/4}\left(t - \frac{T_s}{4}\right) 0 < t < T_s/2 \\ \frac{V_m}{T_s/4}\left(t - \frac{3T_s}{4}\right) T_s/2 < t < T_s \end{cases} \tag{3.33}$$

From Fig-3.15, it is seen that

$$V_{tri}(t_1) = V_{tri}(t_2) = -V_s, t_2 - t_1 = \frac{dT_s}{2} \tag{3.34}$$

With the help of Equ-(3.33) and Equ-(3.34), following relations are deduced

$$t_1 = \frac{T_s}{2}\left(1 + \frac{V_s}{V_m}\right), t_2 = \frac{T_s}{2}\left(3 - \frac{V_s}{V_m}\right) \tag{3.35}$$

Replacing the values of t_1 and t_2 in Equ-(3.33), the expression for duty cycle is

$$d = 1 - \frac{V_s}{V_m} \tag{3.36}$$

Therefore, for duty cycle variation, either V_m or V_s is varied depending on the requirement.

Moreover, the control pulse generation is done such that the condition $m + d \leq 1$ should be maintained strictly otherwise it leads to false operation of the inverter.

Duty cycle in terms of DC gain of the converter is

$$D = \frac{1 - G_{DC}}{1 - 2G_{DC}} \tag{3.37}$$

and AC gain is written as

$$m = 2\sqrt{2}\frac{G_{AC}}{G_{DC}} \tag{3.38}$$

So , the DC and AC gain of the converter are adjusted such that the converter satisfies $\frac{G_{DC}^2}{1-2G_{DC}} + 2\sqrt{2}G_{AC} \leq 0$ condition.

3.5 Comparative analysis between SBI and PSBI

3.5.1 Inductor design

For SBI, the inductor design must be done such that inductor current profile remains triangular to avoid NZ-DCM. So, higher value of inductances is required in SBI(L=1.12mH).

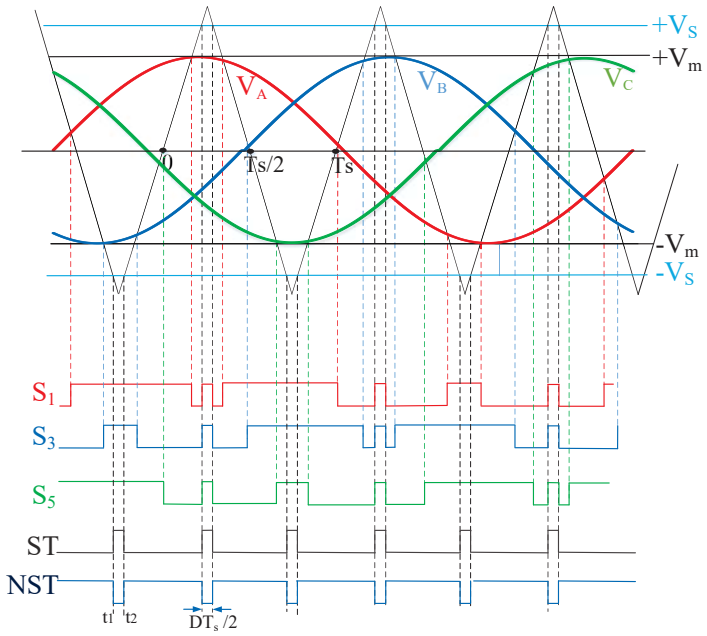


Figure 3.15: Control of proposed converter

Due to presence of antiparallel switch across diode D_2, this constraint is relaxed. As soon as inductor current tries to saturate, the antiparallel switch restores the CCM mode. So, a low value of inductance can be chosen in case of PSBI(L<1.12mH).

3.5.2 Efficiency analysis

To compare the efficiencies of the SBI and PSBI, each passive element and switch are replaced by their corresponding equivalent model. The inductor is represented by a series resistance r_L with the inductance L, capacitor is modelled as series resistance r_c with the capacitor C. Furthermore, both the diodes are replaced by forward voltage drop V_d and a series resistance r_d and switches are replaced by turn on resistance r_{ds} and on state voltage V_{ds}. The inverter is modelled as equivalent single phase circuit to make calculation easy. In Single phase circuit, inverter part is replaced by a resistance R_L.

Core losses

The SBI and PSBI are operated with same operating frequency, inductance value and magnetic cores. Therefore, inductor core losses will be same for both the cases. In this paper, two PCV-2-564-08 inductor coil are used. For operating frequency of 10 kHz,

inductor current 7 A and peak to peak ripple current of 33% of inductor current, the core loss(P_c) is equal to 3 W.

Shoot through state

During shoot through state, the power loss equation is written as

$$P_{st} = d^2 {I_L}^2 (r_c + r_{ds} + r_L) + d I_L V_{ds} \tag{3.39}$$

Equ-(3.39) is valid for both SBI and PSBI as shoot through is identical for both the

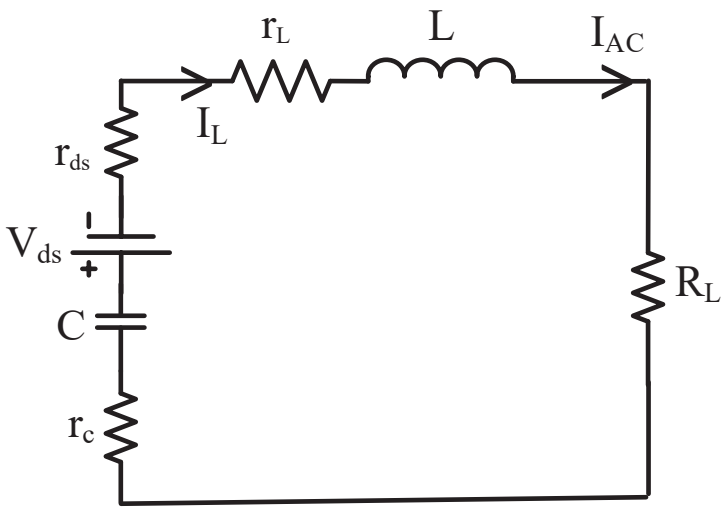


Figure 3.16: Equivalent circuit in shoot through state for SBI/PSBI

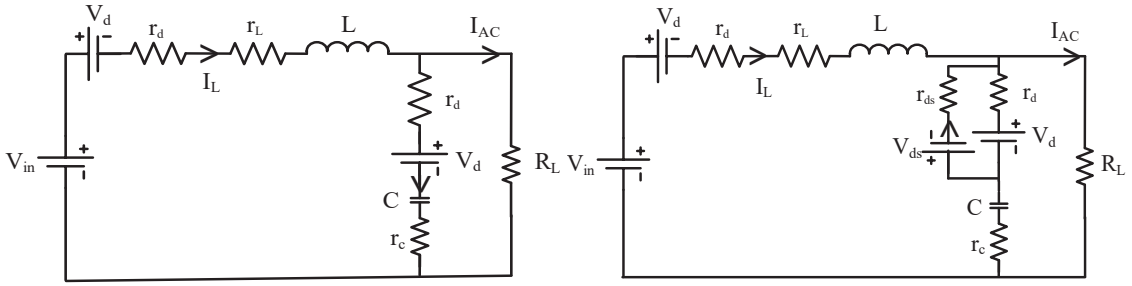
converter.

Non shoot through state

For SBI from Fig-3.17a, the power loss equation is

$$\begin{aligned} P_{nst} &= (1-d)\, V_d I_L + (1-d)^2 {I_L}^2 r_d + (1-d)^2 {I_L}^2 r_L + (1-d)\,(I_L - I_{AC})\, r_d \\ &+ (1-d)^2 (I_L - I_{AC})^2 r_d + (1-d)^2 (I_L - I_{AC})^2 r_c \end{aligned} \tag{3.40}$$

In PSBI, the duration for which the antiparallel switch is turned ON depends on the operating condition. From simulation it is found that around 30% of non shoot through period antiparallel switch conducts for $d = 0.25$. For remaining time, diode D_2 is in



(a) SBI (b) PSBI

Figure 3.17: Equivalent circuit in non shoot through state

operation. So, according to this analysis power loss equation is given as

$$\begin{aligned} P_{nst} &= (1-d)\,V_f I_L + (1-d)^2 {I_L}^2 r_d + (1-d)^2 {I_L}^2 r_L + 0.7\,(1-d)\,(I_L - I_{AC})\,V_d \\ &+ (0.7)^2(1-d)^2(I_L - I_{AC})^2 r_d + 0.7\,(1-d)\,(I_L - I_{AC})\,V_{ds} \\ &+ (0.3)^2(1-d)^2(I_L - I_{AC})^2 r_{ds} + (1-d)^2(I_L - I_{AC})^2 r_c \end{aligned} \tag{3.41}$$

The switching loss for switch S is given by

$$P_S = (V_c - V_{in})\,I_L \left(\frac{t_{d(on)} + t_r}{2} + \frac{t_{d(off)} + t_f}{2} \right) f_s \tag{3.42}$$

whereas for switch S_a, switching loss is given as

$$P_{Sa} = 0.3 V_c\,(I_L - I_{AC}) \left(\frac{t_{d(on)} + t_r}{2} + \frac{t_{d(off)} + t_f}{2} \right) f_s \tag{3.43}$$

The generalized efficiency for the SBI/PSBI is given as

$$\eta = \frac{P_{out}}{P_{out} + P_{st} + P_{nst} + P_S + P_{Sa} + P_c} = \frac{1}{1+\xi} \tag{3.44}$$

where ξ is given as

$$\xi = \frac{P_{st} + P_{nst} + P_S + P_{Sa}}{P_{out}} = A\frac{1}{R_L} + B\frac{1}{R_L} + C\frac{1}{V_{in}} + E\frac{1}{R_L} + F\frac{1}{V_{in}} + H\frac{1}{R_L} + J + \frac{P_c}{P_{out}} \tag{3.45}$$

where A, B, C, E, F, H and J are variable in nature which are presented in Table-3.1. For analysis, the value of converter variable is chosen from the data sheet. These are r_L=0.2 Ω, r_c=1.57 Ω, V_f=1.8 V, r_d=0.1 Ω, r_{ds}=0.75 Ω, V_{ds}=1.2 V, f_s=10 kHz, t_{don}=25 ns, t_r=21 ns, t_{doff}=380 ns and t_f=310 ns . Based on these values, A, B, C, E, F, H and J are plotted in Fig-3.18. Losses term A and B are same for both SBI and PSBI. For SBI, C and E has higher contribution in losses than PSBI. On the other hand, for F, H and J this situation get reversed. Therefore, overall it is inferred that PSBI has almost same

Table 3.1: Loss factors

Loss factor	**SBI**	**PSBI**
A	$\frac{d^2+(1-d)^2}{(1-2d)^2}r_L$	$\frac{d^2+(1-d)^2}{(1-2d)^2}r_L$
B	$\frac{d^2+4d^2(1-d)^2}{(1-2d)^2}r_c$	$\frac{d^2+4d^2(1-d)^2}{(1-2d)^2}r_c$
C	$(1+2d)\,V_d$	$(1+1.4d)\,V_d$
E	$\frac{\left(1+4d^2\right)(1-d)^2}{(1-2d)^2}r_d$	$\frac{\left(1+1.96d^2\right)(1-d)^2}{(1-2d)^2}r_d$
F	$\frac{d}{1-d}V_{ds},$	$\frac{d(1.6-0.6d)}{1-d}V_{ds}$
H	$\frac{d^2}{(1-2d)^2}r_{ds}$	$\frac{d^2+0.36d^2(1-d)^2}{(1-2d)^2}r_{ds}$
J	$\frac{d}{(1-d)(1-2d)}\left(\frac{t_{d(on)}+t_r}{2}+\frac{t_{d(off)}+t_f}{2}\right)f_s$	$0.3\frac{2d}{1-2d}f_s$

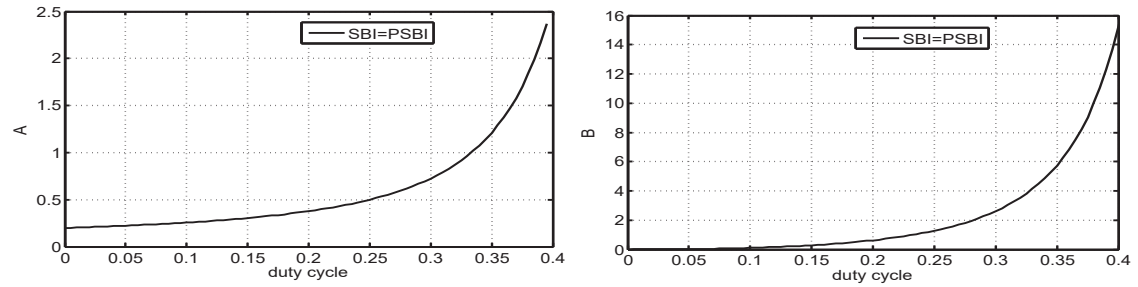
efficiency as SBI. For e.g. at $d = 0.25$, after substituting the values of different factors in Equ-(3.45) then replacing ξ in Equ-(3.44), the efficiency of SBI is 82% while PSBI has 81.7%.

Table 3.2: Comparison of components used in conventional SBI and proposed SBI

Comparison parameter	**Conventional SBI**	**Proposed SBI**
No. of passive element	2	2
No. of active switch	1	2
No. of diode	2	2
Higher duty cycle operation	Yes	Yes
Lower duty cycle operation	No	Yes

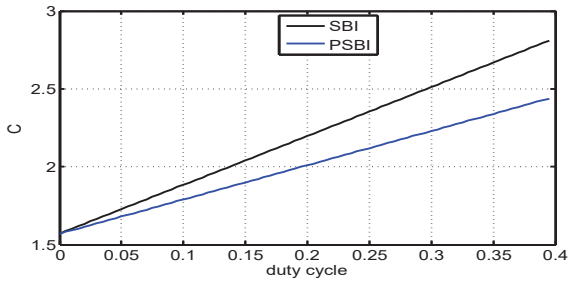
3.5.3 Comparison of passive components and voltage stress analysis

A comprehensive analysis for SBI and PSBI is presented in Table-3.2. Same number of passive elements are used in both SBI and PSBI. In SBI, only one switch(IGBT) is present while PSBI has two switches(one IGBT and one MOSFET). On the other hand, diode used in PSBI is one smaller than SBI if body diode of MOSFET serves as diode D_2,

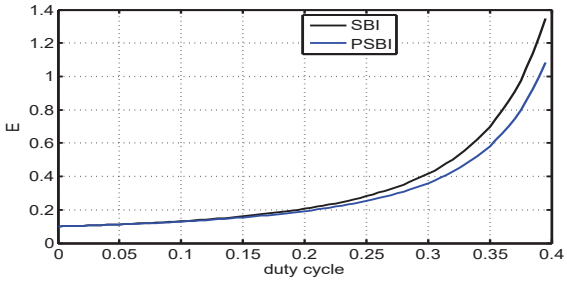


(a)

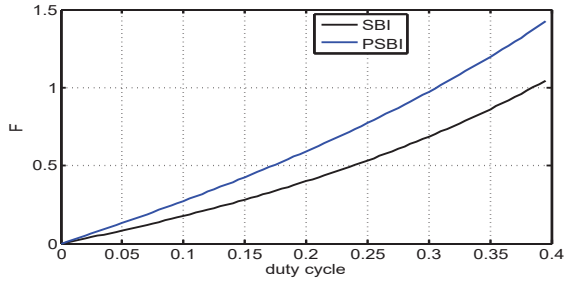
(b)



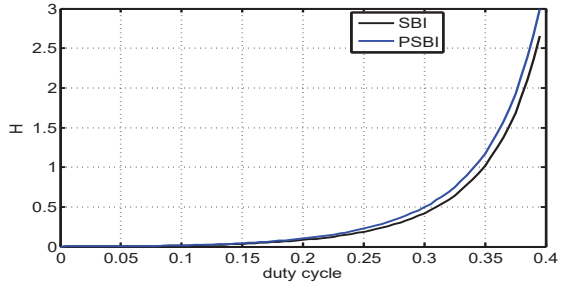
(c)



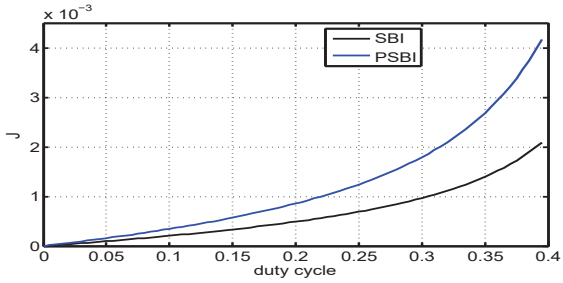
(d)



(e)



(f)



(g)

Figure 3.18: Loss factor variation with duty cycle

otherwise PSBI will also have 2 diodes. Moreover, PSBI perfectly works in both lower and higher duty cycle.

Due to aberrant operation of SBI in lower duty cycle, the voltage stress in SBI is different than the PSBI. The voltage stress across the capacitor(C) in lower duty cycle(V_{nzc}) is higher than the normal stress(V_c). So, the maximum voltage stress across the switches are subjected is higher in case of SBI. In PSBI, as the converter operates satisfactorily the voltage across the capacitor always remain V_c which reduces the overall stress across the elements. Voltage stress across different elements is presented in Table-3.3.

Table 3.3: Voltage stress analysis between SBI and proposed SBI

Max Voltage stress across	**Conventional SBI**	**Proposed SBI**
Inverter switch	V_{nzc}	V_P
Switch S_1	$V_{nzc} - V_{in}$	$V_c - V_{in}$
Switch S_2	NA	V_c
Diode D_1	$V_{in} - V_{nzc}$	$V_{in} - V_c$
Diode D_2	V_{nzc}	V_c
Capacitor C	V_{nzc}	V_c

3.6 Simulation and experimental results

For verification of operating characteristics of proposed converter, simulation is done on Matlab/Simulink platform and its validation is done experimentally. The parameters for the simulation and experimental validation are taken as per the Table-3.4.

Experimental set up is shown in Fig-3.19. The components used in the experiment are enlisted in Table-3.5. To check the severity of the problem at lower duty cycle the extensive analysis for three different duty cycle having NZ-DCM operation is considered. Moreover, for validation of the proper functioning at elevated duty cycle, experimental analysis is done. The spikes observed in the experimental results are due to antiparallel switch connected across diode, stray inductance and capacitances of circuit. The experiments and simulation are conducted corresponding to three modes-CCM, NZ-DCM and FCCM. In particular the origin of NZ-DCM and its mitigation using FCCM was the main

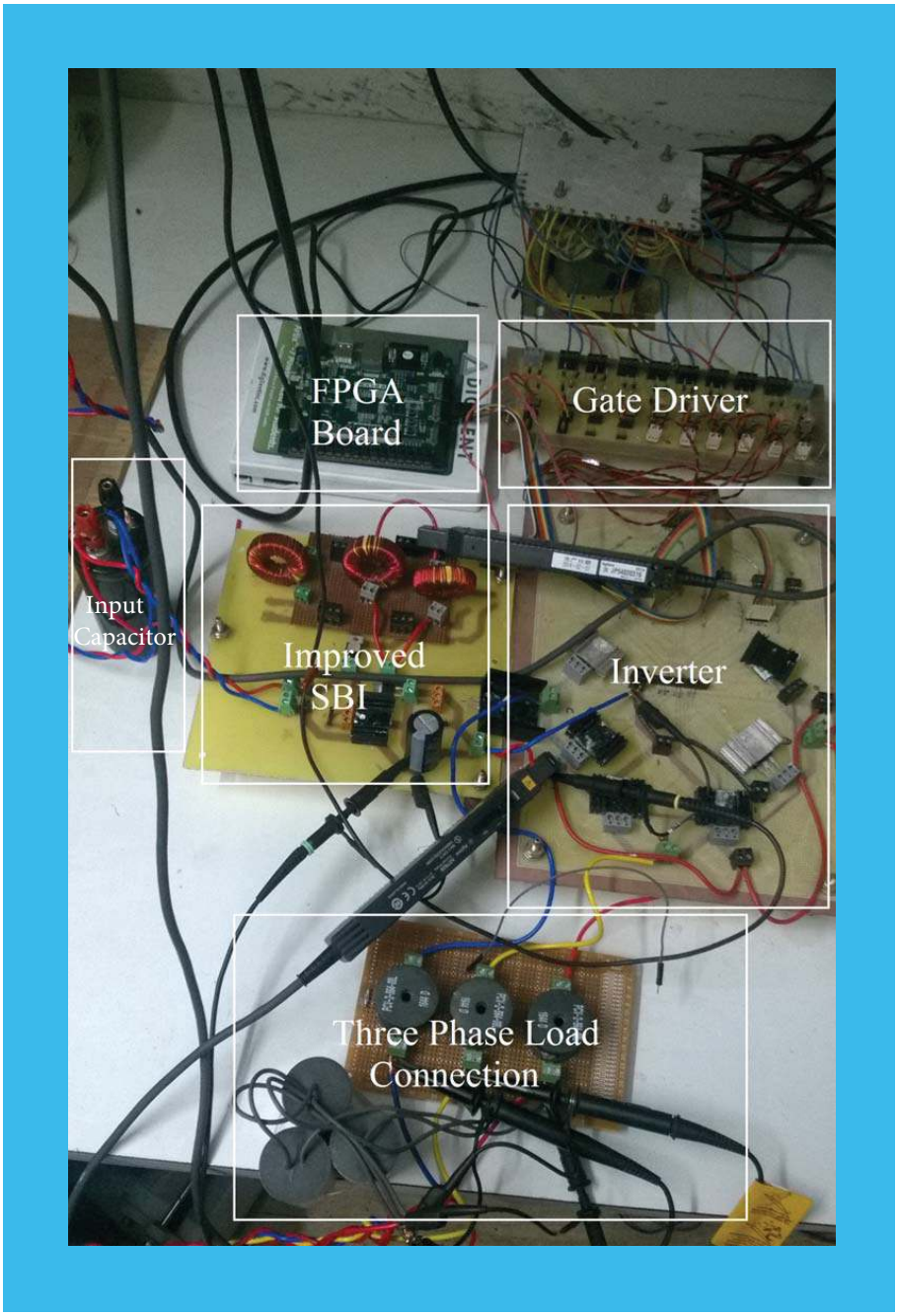


Figure 3.19: Experimental setup for SBI

Table 3.4: Design parameters and specification

Parameter	**Rating**
Power rating	370 W
Input Voltage	70 volt
Inductance	1.12 mH
Capacitance	$100\mu F$
Filter Inductance	0.56 mH
Filter Capacitance	$10\mu F$
AC load Resistance	5Ω
Switching frequency	10 kHz

objective. The experimental results for DC link voltage in case of NZ-DCM shows the ringing behaviour which is present due to self resonance of inductor.

Table 3.5: Converter component

S.N.	**Component**	**Number and Manufacturer**
1.	MOSFET	SIHG32N50D Vishay Siliconix
2.	IGBT	IRG4BC40FPbF IOR Corp.
3.	Diode (D_a)	ISL9R1560G2 Fairchild
4.	Gate Drive IC	HCPL3120 Avago Technology

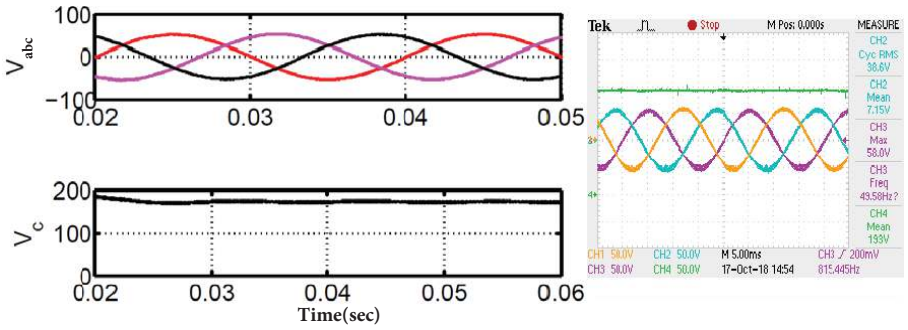


Figure 3.20: For CCM d=0.4, m=0.6: a) AC voltage b) DC voltage, $[Ch1 : 50V/div, Ch2 : 50V/div, Ch3 : 50V/div, Ch4 : 50V/div]$

3.6.1 Continuous mode analysis

For analyzing the performance of SBI in CCM, SBI is operated at a duty cycle of 0.4 and modulation index of 0.6. At this operating point, the duty cycle is high i.e. it draws a large amount of the current from the source end during shoot through period, while it discharges for short duration as active period is small. At R_{ac}=16 Ω, the average inductor current I_L=7.17 A, $\Delta I_L/2$=3.21 A and i_{ac} =3.28 A. From Equ-(3.20), i_{ac} = 3.28 A < $(I_L - \frac{\Delta I_L}{2})$ = 3.96 A, which is true. This ensures CCM operation of SBI. Fig-3.20 and Fig-3.21 also indicates that waveforms do not show any distortion in either of the waveforms.

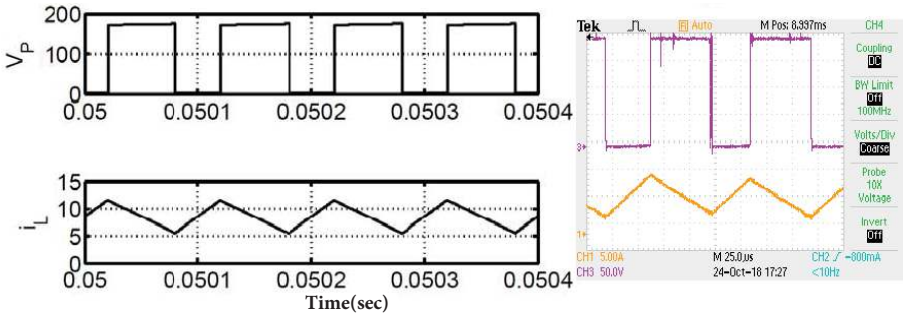


Figure 3.21: For CCM d=0.4, m=0.6: a) DC link voltage b) Inductor current, $[Ch2 : 50V/div, Ch3 : 5A/div]$

3.6.2 Redemption of NZ-DCM with FCCM

To verify the PSBI, two different duty cycle is chosen and analysed for NZ-DCM and FCCM in following sub-sections.

Duty cycle=0.25

The first case for the NZ-DCM analysis is considered at $d = 0.25$. For this, load resistance is reduced from R_{ac} =16 Ω to R_{ac} =5 Ω thereby current is increased to i_{ac} =7.1 A. Corresponding to this i_{ac}, I_L=7 A while $\Delta I_L/2 = 1.17$ A. From Equ-(3.23), i_{ac} = 7.1 A > $(I_L - \frac{\Delta I_L}{2})$=5.83 A which is true. So, NZ-DCM is observed as shown in Fig-3.22. The DC link voltage consist a small dip, while inductor current becomes discontinuous(saturated) for small interval. At d = 0.25, the duty cycle(d_1) for NZ-DCM is equal to 0.18. This causes increase in voltage across capacitor as per Equ-(3.27). The voltage across the

capacitor becomes 125 V which is higher than the expected value by 20 V as shown in Fig-3.23.

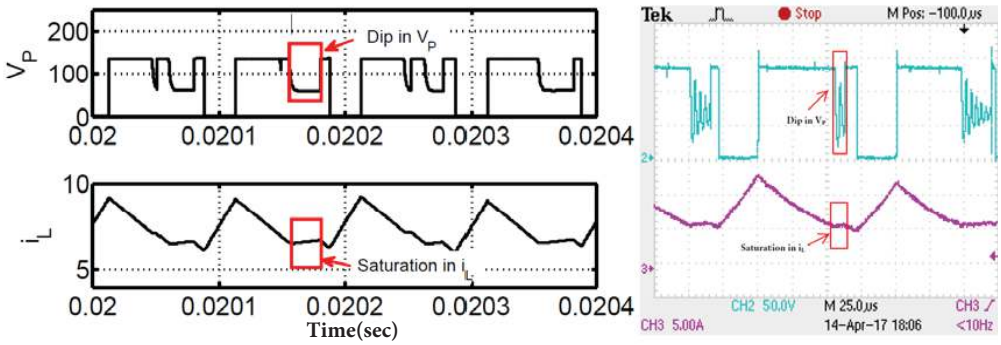


Figure 3.22: For NZ-DCM d=0.25, m=0.6: a) DC link voltage b) Inductor current, $[Ch2 : 50V/div, Ch3 : 5A/div]$

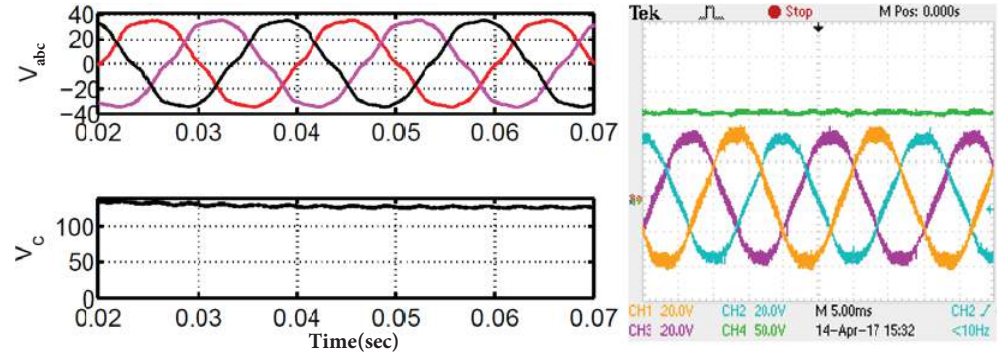


Figure 3.23: For NZ-DCM d=0.25, m=0.6: a) AC voltage b) DC voltage, $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

With the antiparallel switch across the diode D_2, the FCCM removes dip in DC link voltage and inductor current becomes continuous. The AC load voltage is sinusoidal during this mode. These are visible in both simulation and experimental results as shown in Fig-3.24 and Fig-3.25. The voltage across the capacitor is found to be 105 V and AC voltage is 35.4 V which is same as theoretical value.

Duty cycle=0.22

At d = 0.22 duty cycle, R_{ac} is kept at 5 Ω, hence, i_{ac} is reduced to 6.8 A, I_L=7 A and $\Delta I_L/2$= 0.99 A. From Equ-(3.23), i_{ac} = 6.8 A>$(I_L - \frac{\Delta I_L}{2})$ = 5.36 A which is true. The converter is still in NZ-DCM. At this duty cycle, the dc link voltage has higher dip and

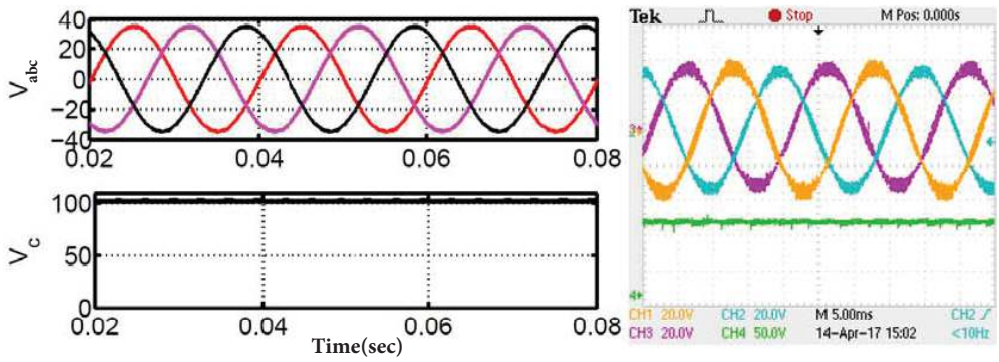


Figure 3.24: For FCCM d=0.25, m=0.6: a) AC voltage b) DC voltage, $[Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div]$

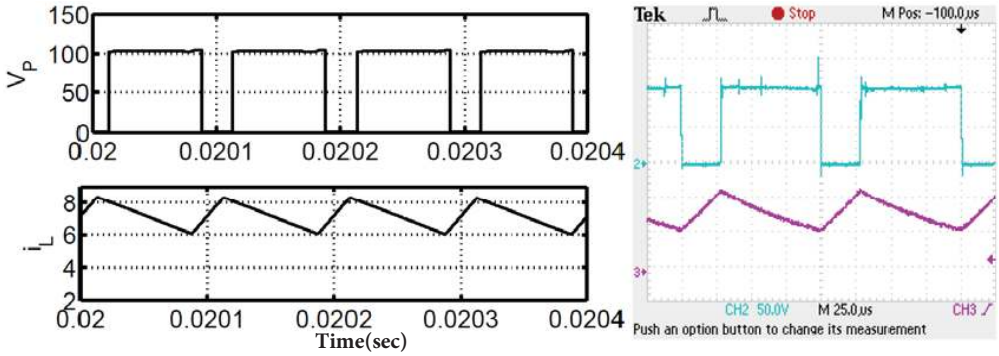


Figure 3.25: For FCCM d=0.25, m=0.6: a) DC link voltage b) Inductor current, $[Ch2 : 50V/div, Ch3 : 5A/div]$

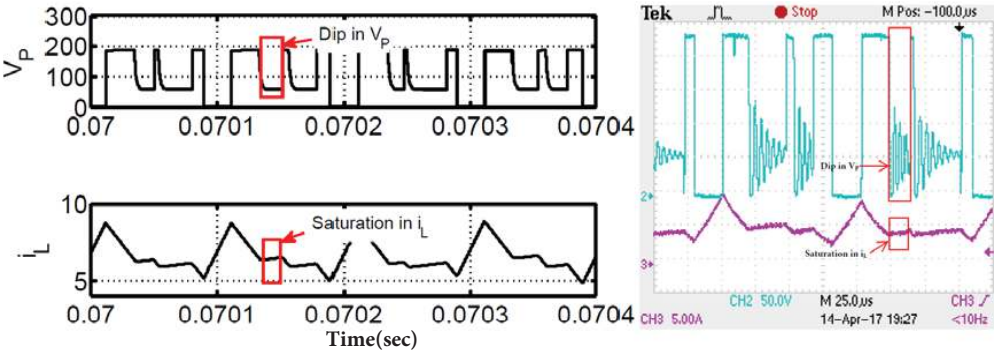


Figure 3.26: For NZ-DCM d=0.22, m=0.6: a) DC link voltage b) Inductor current, $[Ch2 : 50V/div, Ch3 : 5A/div]$

inductor current saturates for longer duration as shown in Fig-3.26. Therefore, NZ-DCM duty cycle increased to d_1=0.44. As per Equ-(3.27), the DC link voltage is 200 V which is 99 V higher than CCM. The AC voltage undergoes large distortion thereby THD is higher along with reduction in peak value by 3 V around as compared to expected value. This is due to un-clamping of capacitor C as shown in Fig-3.27.

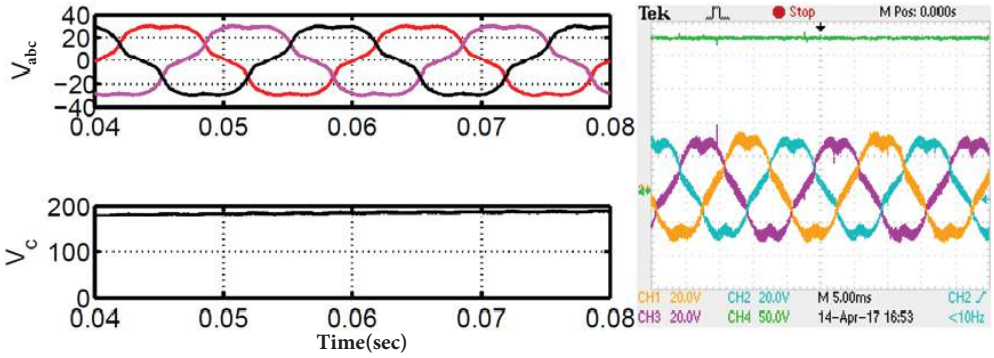


Figure 3.27: For NZ-DCM d=0.22, m=0.6: a) AC voltage b) DC voltage, [$Ch1 : 20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div$]

By turning on the switch Sa, the current flow path is provided, and no dip in dc link voltage is observed. Moreover, inductor current is triangular in nature as shown in Fig-3.28. The AC and DC voltages reach to its expected value 34 V and 101 V respectively. The nature of AC voltage is sinusoidal as shown in Fig-3.29.

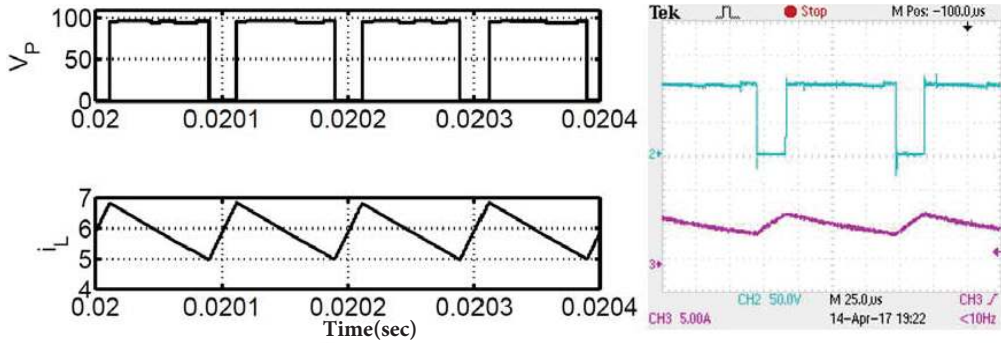


Figure 3.28: For FCCM d=0.22, m=0.6: a) DC link voltage b) Inductor current, [$Ch2 : 50V/div, Ch3 : 5A/div$]

A comprehensive analysis of variable duty cycle is presented in Table-3.6. Moreover, THD analysis for NZ-DCM and FCCM is presented in Fig-3.30. From analysis, it is obvious that as the duty cycle decreases, voltage across capacitor and THD increase

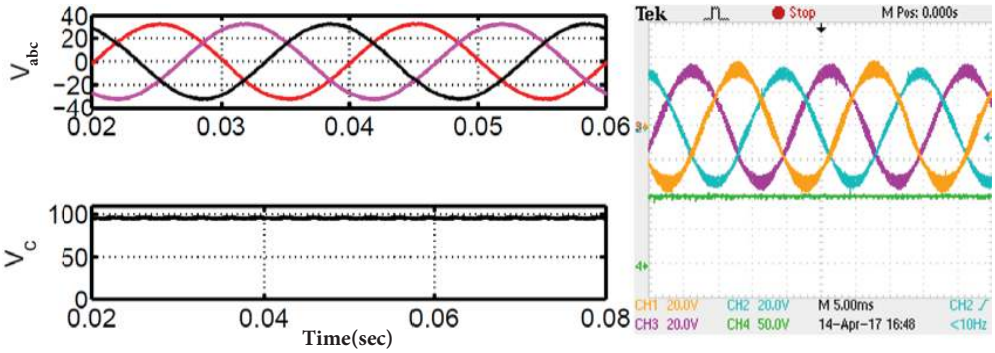


Figure 3.29: For FCCM d=0.22, m=0.6: a) AC voltage b) DC voltage, [$Ch1$: $20V/div, Ch2 : 20V/div, Ch3 : 20V/div, Ch4 : 50V/div$]

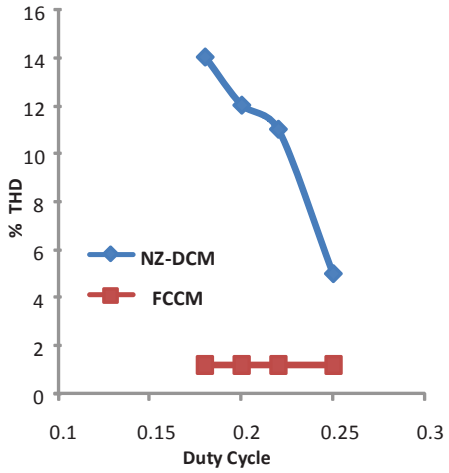


Figure 3.30: THD comparison for NZ-DCM and FCCM

Table 3.6: Comparison of SBI at different duty cycle in NZ-DCM and FCCM

Duty Cycle	**Expected Voltage**		**NZ-DCM Voltage**		**FCCM Voltage**	
	AC	**DC**	**AC**	**DC**	**AC**	**DC**
d=0.25	35.43	105	34	125	35	104
d=0.22	34	101	30	200	33.5	99
d=0.20	31.5	93	26	270	31	91

under NZ-DCM. Once NZ-DCM is replaced by FCCM, the capacitor voltage was equal to expected value and also THD is constant corresponding to different low duty cycles. Therefore, the proposed modified converter has potential to achieve high performance under duty cycle and load variation.

3.7 Conclusion

This chapter presented the behaviour of SBI in lower and higher duty cycle. In higher duty cycle, converter behaviour is satisfactory while in lower duty cycle its operation is aberrant. This aspect is proved by observing THD in AC voltage, the profile of AC voltage and the voltage across the capacitor. The AC output voltage has higher THD during NZ-DCM say 12% at $d = 0.22$. Moreover, the capacitor voltage is higher and AC voltage is lower than the expected. These changes are more effective in even lower duty cycle. During FCCM, the stress across the capacitor is reduced, AC voltage is restored to its original value and THD is lowered to 1.2% at $d = 0.22$. The effectiveness of the converter is proved by experimental and simulation studies.

Proposed SBI is able to operate in wide duty variation, however, the gain is not sufficient. In the subsequent chapter, a high gain coupled inductor based Z-source inverter will be proposed. The proposed converter exhibits high gain at lower duty cycle, therefore, the stress across the switches will be minimized. The proposed converter will be validated experimentally.