Chapter 2

An Ultra High Gain DC-DC Converter

2.1 Introduction

Boost converter is suitable for increasing the voltage gain. Theoretically, infinite gain is possible by conventional boost converter with large duty cycle variation. However, as the duty cycle is stretched, the efficiency of the converter decreases drastically. Normally, for duty cycle greater than 0.5, the non linearity present in the converter plays dominant role in deciding the gain of the converter. Therefore, around 2.5-3 times gain is achievable by the conventional boost converter.

Many efforts have been made to improve the gain of the converter in last few decades. Broadly, these topologies are categorised into two parts: isolated and non isolated. Cascading of two boost converter was proposed to further increase the gain of the converter. The gain of the converter can be extended depending on the number of stages present, however, cascading of converters reduces the efficiency drastically and increases the cost and volume which is not suitable from practical point of view. In order to reduce the size and complexity, quadratic boost converter employing diodes was proposed but the gain was limited. To enhance the gain, in last few decades, various non isolated topologies such as interleaved, voltage lift, switched capacitor and switched inductor, voltage multiplier cells and active switch network are proposed [109].

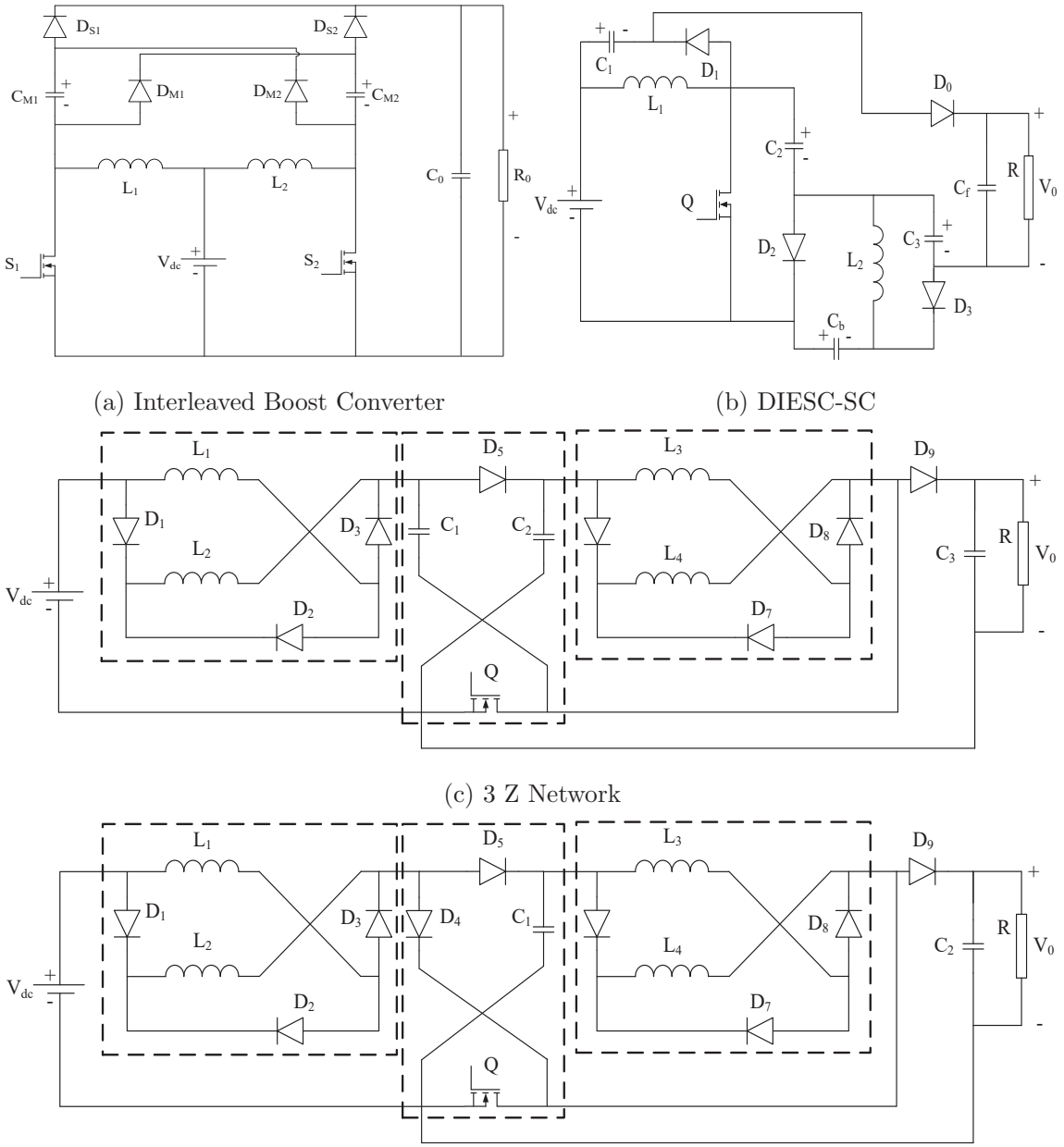
Though these converters increase the gain, the duty cycle is varied in a wide range(i.e. $0 < D < 1$). This increases the conduction loss of the converter, hence, efficiency of the

converter is compromised. In order to address this limitation, Peng et al proposed Z source converter. The Z source converter is a symmetrical arrangement of two inductors and two capacitors [56]. However, discontinuous input current and uneven degradation of capacitor with time are common problems. To overcome these issues, a family of quasi Z source converter was introduced in 2009 [59]. The gain provided by these converters is similar to Z source inverter and equal to $\frac{1}{1-2D}$. Recent development in the Z network is interconnection of 3 Z networks to achieve higher gain i.e. $\left(\frac{1+D}{1-D}\right)^2$ [110]. Although the gain of the converter is squared type but the duty cycle is varied over the entire range(i.e. $0 < D < 1$). Due to the presence of non linearity in the converter, the converter gain is restricted and for more than 50% duty cycle inductor become saturated therefore converter may become unstable. To address this challenge, Ngyuen et al proposed switched capacitor based dual switch high boost DC DC converter where the duty cycle is restricted in the range of $0 < D < 0.5$, but the gain was limited [111]. Zhang et al proposed a high gain converter which is capable to provide gain factor of $\frac{1+D}{1-3D}$ [112]. However, the number of components is higher in recently proposed network. Therefore, the motivation behind the proposed DC-DC converter in this chapter is to reduce the number of passive of elements and to produce higher voltage gain. The DC-DC converters which are close to the proposed converter are presented in Fig-2.1 and will be compared in the comparison section of this chapter.

In this chapter, a dual switched based high gain DC DC converter is proposed to enhance the gain. This converter has feature of low conduction loss, low voltage stress across diode and switches, high step up conversion ratio as compared to Ngyuen et al proposal. Furthermore, as compared to Zhang et al, the proposed converter utilizes reduced number of elements and provides higher gain. Moreover, due to lower duty cycle operation, the possibility of inductor saturation is eliminated, therefore the converter remains stable.

2.2 Proposed topology

Dual active switch based DC-DC converter is reported recently which has limited gain and lower number of passive components. However, 3 Z network [110] and a high gain impedance converter [112] have higher gain as compared to dual active switch based DC-



(a) Interleaved Boost Converter

(b) DIESC-SC

(c) 3 Z Network

(d) High Gain Impedance Network

Figure 2.1: Contemporary converters

DC converter. So, the motivation behind the proposed converter is to develop a DC-DC converter which has the property of high gain and lower passive components count.

The proposed topology imbibes the feature of switched inductor/switched capacitor arrangement as shown in Fig-2.2. The switches required in the proposed converter are two which is inspired from dual active switch DC-DC converter. The proposed converter has higher number of passive count than dual active switch based DC-DC converter and lower number of total component count than 3 Z network and a high gain impedance network. So, there is a trade off to realize a higher voltage gain with a smaller duty cycle by the proposed converter as compared to existing converter.

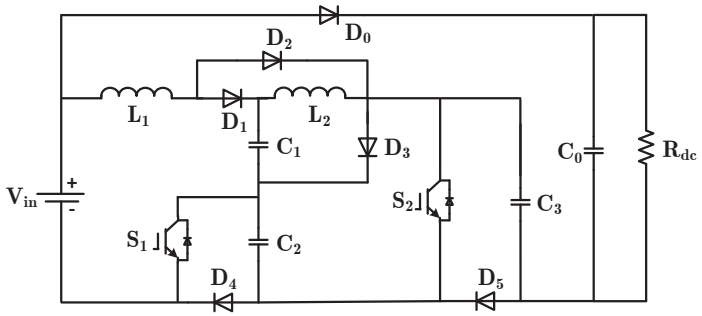


Figure 2.2: Proposed DC-DC converter

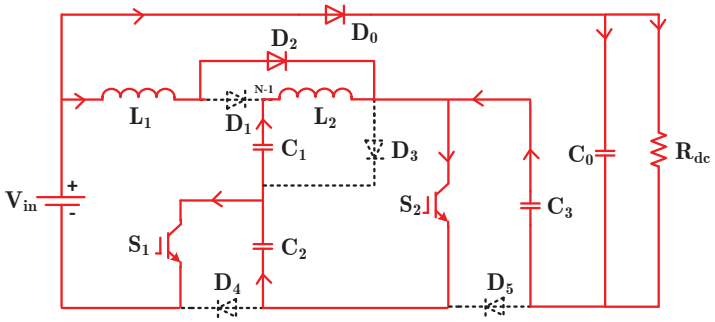


Figure 2.3: Operating mode 1

The proposed converter is able to operate in both continuous current mode(CCM) and discontinuous current mode(DCM). Different cases are possible for DCM in the proposed converter depending on the nature of currents through L_1 and L_2 . However, in this thesis, only CCM is taken into consideration for analysis, which is widely employed in the industrial applications. For simplicity, it is assumed that all components are ideal, the free-wheeling diode and internal diode of the switch are ignored, the forward voltage

drop of the diode is ignored, the capacitances of the capacitors C_1, C_2, C_3 and C_0 are large enough to assume the voltages V_{C1}, V_{C2}, V_{C3} and V_0 to be constant.

Two possible mode exists for the proposed boost converter. These modes are named as mode 1 and mode 2. The equivalent circuits for mode 1 and mode 2 are shown in Fig-2.3 and Fig-2.4, respectively. Therein, V_{in} is source voltage, V_{L1}, V_{L2} are the voltage across inductor L_1 and L_2, respectively. V_{D0}.....V_{D5} are the voltages across diodes D_0.....D_5, respectively. V_{S1} and V_{S2} are the voltages across switches S_1 and S_2 respectively, and V_0 is the output voltage.

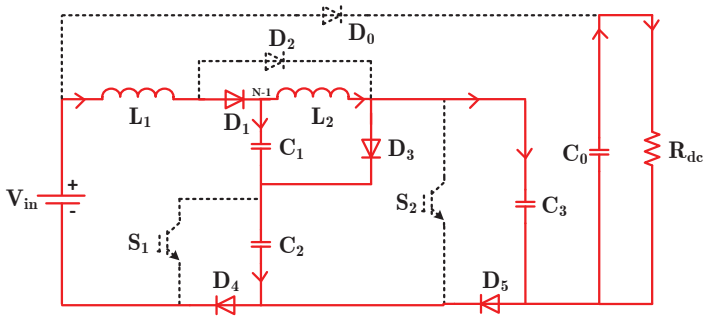


Figure 2.4: Operating mode 2

In order to describe the operation of proposed boost converter, the steady state waveforms are shown in Fig-2.5. The signal S_1 and S_2 represent the gate pulses for switches S_1 and S_2 as shown in Fig-2.5a, i_{L1} and i_{L2} are inductor currents profile (Fig-2.5b and c). The width of gate pulse is dT_S , where d is the duty cycle or charging period of the inductor and T_s is switching time period. The output voltage is represented by V_0 as shown in Fig-2.5d.

2.2.1 Mode 1, $t_0 < t < t_1$

The equivalent circuit pertaining to this mode is shown in Fig-2.3. As the switches G_1 and G_2 are turned ON, the diodes D_0 and D_2 experience positive voltage across them, therefore, become forward biased. Meanwhile, the diodes D_1, D_3, D_4 and D_5 bear negative voltage across them and hence are reverse biased. Thereafter, L_1 is charged by the source voltage V_{in} through D_2-S_1-C_2-S_2. Moreover, L_2 is charged by capacitor C_1 and C_2 through switch S_2. The inductor currents i_{L1} and i_{L2} start increasing linearly, and inductors store energy. The source V_{in} along with capacitor C_3 also discharges its energy into load through

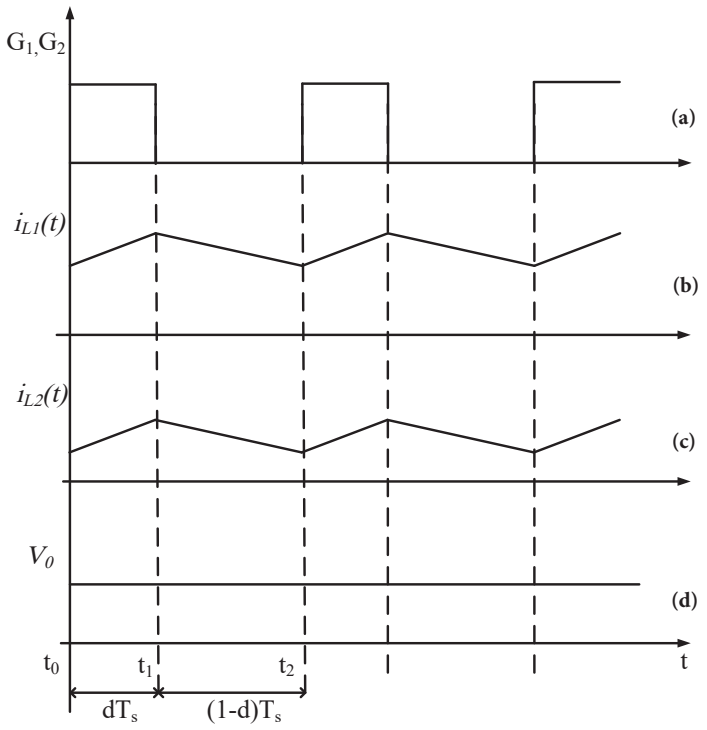


Figure 2.5: Operational waveform

diode D_0 and switches S_1, S_2. During this mode, voltage equations are

$$V_{in} - V_0 + V_{C3} + V_{C2} = 0 \tag{2.1}$$

$$V_{C1} + V_{L2} - V_{C2} = 0 \tag{2.2}$$

$$V_{in} - V_{L1} + V_{C2} = 0 \tag{2.3}$$

2.2.2 Mode 2, $t_1 < t < t_2$

The equivalent circuit corresponding to this mode is depicted in Fig-2.4. During this mode, the switches S_1 and S_2 are turned OFF. Therefore, diode D_4 and D_5 are forward biased. The diodes D_0 and D_2 experience negative voltage and diode D_1 has positive voltage across it as inductor L_1 and L_2 changes their polarity. Thereafter, inductor L_1 and L_2 discharges. The inductor L_1 charges the capacitor C_2 and C_3 through diode D_4 and D_5, respectively and L_2 charges the capacitor C_1 through D_3. In addition, the capacitor

C_0 maintains the constant voltage across the load by discharging into load. During this mode, the governing voltage equations are

$$V_{in} - V_{L1} + V_{C1} - V_{C2} = 0 \tag{2.4}$$

$$V_{L2} = -V_{C1} \tag{2.5}$$

$$V_{C2} = V_{C3} \tag{2.6}$$

Since average voltage across inductor L_2 is zero, hence

$$\int_0^{dT_S} V_{L2}dt + \int_{dT_s}^{T_s} V_{L2}dt = 0 \tag{2.7}$$

Substituting Equ-(2.2) and Equ-(2.5),

$$d\left(-V_{C1} + V_{C2}\right) + (1-d)\left(-V_{C1}\right) = 0 \tag{2.8}$$

After simplification, Equ-(2.8) can be written as

$$V_{C1} = dV_{C2} \tag{2.9}$$

Similar to L_2, the average voltage across L_1 is zero, hence

$$\int_0^{dT_S} V_{L1}dt + \int_{dT_s}^{T_s} V_{L1}dt = 0 \tag{2.10}$$

Substituting Equ-(2.3) and Equ-(2.4), Equ-(2.10) gives

$$d\left(V_{in} + V_{C2}\right) + (1-d)\left(V_{in} + V_{C1} - V_{C2}\right) = 0 \tag{2.11}$$

After rearrangement, and putting V_{C1} from Equ-(2.9), voltage across capacitor V_{C2} is given as

$$V_{C2} = \frac{1}{1 - 3d - d^2} V_{in} \tag{2.12}$$

After substituting V_{C1} and V_{C2} in Equ-(2.1), the output voltage V_0 is obtained as

$$V_0 = \frac{3 - 3d - d^2}{1 - 3d - d^2} V_{in} \tag{2.13}$$

Therefore, the gain G_{DC} of the proposed converter is given as

$$G_{DC} = \frac{V_0}{V_{in}} = \frac{3 - 3d - d^2}{1 - 3d - d^2} \tag{2.14}$$

2.3 Design guidelines

Assuming lossless components and by energy conservation, the input power should be equal to output power. Therefore, the input current is written as

$$I_{in} = \frac{P_0}{V_{in}} = \frac{{V_0}^2}{V_{in}R} \tag{2.15}$$

I_{L1} calculation:

The average inductor current I_{L1} is given by

$$I_{L1} = I_{in} - I_0 \tag{2.16}$$

Hence,

$$I_{L1} = \frac{{V_0}^2}{V_{in}R} - \frac{V_0}{R} \tag{2.17}$$

I_{L2} calculation: During mode 1, the KCL at N-1 is written as

$$i_{L1} + i_{C1} = i_{L2} \tag{2.18}$$

During mode 2, the KCL at N-1 is written as

$$i_{C1} = i_{L2} \tag{2.19}$$

Applying charge balance theory in capacitor C_1,

$$(1-d)\,(I_{L2} - I_{L1}) + dI_{L2} = 0 \tag{2.20}$$

This results in

$$I_{L2} = (1-d)\,I_{L1} \tag{2.21}$$

2.3.1 Inductor design

From Equ-(2.3), the peak to peak to ripple current(ΔI_{L1}) is calculated by putting $V_{L1} = L_1 \frac{\Delta I_{L1}}{dT_s}$. Therefore, the inductor L_1 in terms of peak to peak ripple current is given as

$$L_1 = \left(\frac{V_{in} + V_{C2}}{\Delta I_{L1}}\right) dT_s \tag{2.22}$$

From Equ-(2.2), the peak to peak to ripple current(ΔI_{L2}) is calculated by putting $V_{L2} = L_1 \frac{\Delta I_{L2}}{dT_s}$. Therefore, the inductor L_2 in terms of peak to peak ripple current is given as

$$L_2 = \left(\frac{V_{C2} - V_{C1}}{\Delta I_{L2}}\right) dT_s \tag{2.23}$$

2.3.2 Capacitor design

The design of the capacitor is based on the capacitor voltage ripple. This voltage ripple is dependent on the current flowing into the capacitor. Therefore, the capacitor calculation is dependent on the current flowing into the capacitor.

Capacitor C_1 calculation:

During mode 1, the current flowing through the capacitor is equal to I_{L2}. Therefore,

$$C_1 \frac{\Delta V_{C1}}{dT_s} = I_{L2} \tag{2.24}$$

Hence, the capacitor C_1 in terms of peak to peak ripple voltage is written as

$$C_1 = \left(\frac{I_{L2}}{\Delta V_{C1}} \right) dT_s \tag{2.25}$$

Capacitor C_2 calculation:

During mode 1, the current flowing through the capacitor is equal to $I_{L1} + I_{L2} + I_0$. Therefore,

$$C_2 \frac{\Delta V_{C2}}{dT_s} = I_{L1} + I_{L2} + I_0 \tag{2.26}$$

Hence, the capacitor C_2 in terms of peak to peak ripple voltage is written as

$$C_2 = \left(\frac{I_{L1} + I_{L2} + I_0}{\Delta V_{C2}} \right) dT_s \tag{2.27}$$

Capacitor C_3 calculation:

During mode 1, the current flowing through the capacitor is equal to I_0. Therefore,

$$C_3 \frac{\Delta V_{C3}}{dT_s} = I_0 \tag{2.28}$$

Hence, the capacitor C_3 in terms of peak to peak ripple voltage is written as

$$C_3 = \left(\frac{I_0}{\Delta V_{C3}} \right) dT_s \tag{2.29}$$

Capacitor C_0 calculation:

During mode 2, the current flowing through the capacitor is equal to I_0. Therefore,

$$C_0 \frac{\Delta V_{C0}}{(1-d)\, T_s} = I_0 \tag{2.30}$$

Hence, the capacitor C_0 in terms of peak to peak ripple voltage is written as

$$C_0 = \left(\frac{I_0}{\Delta V_{C0}} \right) (1-d)\, T_s \tag{2.31}$$

Table 2.1: Voltage stress across switches and diodes

	Mode 1	**Mode 2**
V_{S1}	0	$\frac{1}{1-3d-d^2}V_{in}$
V_{S2}	0	$\frac{1}{1-3d-d^2}V_{in}$
V_{d1}	$\frac{1-d}{1-3d-d^2}V_{in}$	0
V_{d2}	0	$\frac{d}{1-3d-d^2}V_{in}$
V_{d3}	$\frac{1}{1-3d-d^2}V_{in}$	0
V_{d4}	$\frac{1}{1-3d-d^2}V_{in}$	0
V_{d5}	$\frac{1}{1-3d-d^2}V_{in}$	0
V_{d0}	0	$\frac{2}{1-d-d^2}V_{in}$

2.3.3 Voltage stress across semiconductor devices

During conduction of diodes and switches, the voltage across them will be zero. Therefore, the diodes and switches are stressed during the reverse bias condition of diode and turn off state of switches. In mode 1, both the switches are turned On, therefore voltage stress across them is equal to zero. However, in mode 2, a voltage appears which is equal to V_{C2} or V_{C3}, as shown in Table-2.1. Similarly in mode 1, D_2 and D_0 are reverse biased, therefore voltage across them is zero. In mode 2, V_{C1} appears across diode D_2 and $V_{in}-V_0$ appears across D_0. In mode 2 diodes D_1, D_3, D_4 and D_5 are forward biased, hence the voltage across them is zero. In mode 1, voltage $V_{C1}-V_{C2}$, V_{C3}, V_{C4} and V_{C3} will appear across didoes D_1, D_3, D_4 and D_5 respectively as shown in Table-2.1.

2.4 Comparison with non isolated converters

The comparison of the proposed converter with few other non isolated converter which are presented in Table-2.2. In comparison to interleaved boost converter(IBC)(Fig-2.1a), the voltage stress across the device in the proposed converter is lower while gain is higher. As compared to double inductor storage cell based switched capacitor(DIESC-SC)(Fig-2.1b), the proposed converter utilizes higher number of switches and similar passive elements, however, the voltage stress across components is lower in the proposed converter is lower. In comparison to 3 Z network(Fig-2.1c), the proposed converter uses same number of

Table 2.2: Comparison of proposed converter with existing converter

	Interleaved	**DIESC-SC**	**3 Z Network**	**High Gain**	**Proposed**
Gain	$\frac{2}{1-d}$	$\frac{2+d}{(1-d)}$	$\frac{(1+d)^2}{(1-d)^2}$	$\frac{1+d}{1-3d}$	$\frac{3-3d-d^2}{1-3d-d^2}$
Inductor	2	2	4	4	2
Diodes	4	4	9	8	6
Capacitors	3	5	2	3	4
Switches	2	1	1	1	2
D_0 Voltage	$\frac{V_0}{2}$	$\frac{V_0}{2+d}$	$\frac{(1+d)^2}{(1-d)^2}V_{in}$	$\frac{1+d}{1-3d}V_{in}$	$V_0 - V_{in}$
Input ripple	Low	High	High	High	Low
Efficiency	95.2%	95%	90%	91%	94%

passive elements , nevertheless, the semiconductor devices are lower. On the other hand, one lower semiconductor device and passive element each is used in proposed DC-DC converter than a high gain impedance(Fig-2.1d).

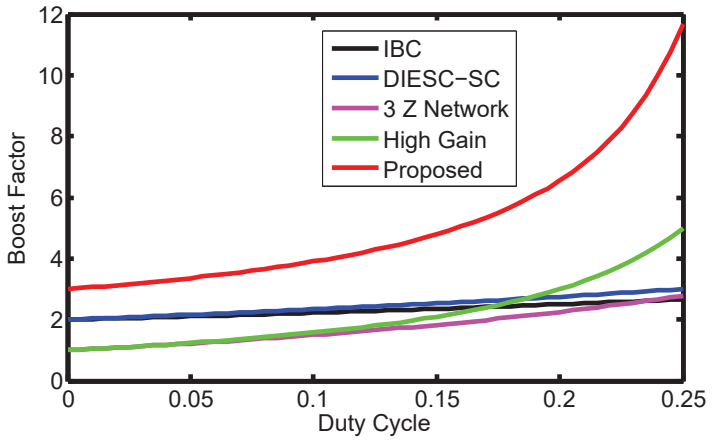


Figure 2.6: Boost factor comparison

Moreover, similar to interleaved converter the input current ripple in the proposed converter is low. The duty cycle is restricted in the range of $0 < d < 1/3$ which is lower than other existing converters. The comparison of boost factor for various topologies is shown in Fig-2.6. The gain achieved by the proposed converter is quite high in the lower duty cycle range as compared to other converter. Due to lower duty cycle operation, the proposed converter has lower conduction losses than other converters. For a 200 W power rating, the efficiency of various converters is calculated using simulation, which is listed in

Table-2.2. It is found that proposed DC-DC converter(94%) has better efficiency than 3-Z network(90%) and high gain impedance network(91%). On the other hand, IBC(95.2%) and DIESC-SC(95%) has better efficiency due to lower number of passive component counts as compared to the proposed DC-DC converter.

Table 2.3: Specification and design parameters of converter

Parameter	**Rating**
Input Voltage	43 V
Output Voltage	200 V
Inductance L_1	2.24 mH
Inductance L_2	1.12 mH
Capacitor C_1	5 μF
Capacitor C_2	10 μF
Capacitor C_3	15 μF
Capacitor C_0	100 μF
Frequency	10 kHz
Load Resistance	200 Ω

2.5 Experiment results

For experimental verification, a 200 W prototype is designed and tested. The converter is operated at 20 kHz switching frequency. The inductor L_1 is designed for 10% ripple current, however, inductor L_2 is designed for 9% ripple current. Based on ripple currents, the inductance L_1 and L_2 are designed 2.24 mH and 1.12 mH, respectively. The values for capacitances are chosen corresponding to 1% of ripple voltage. The calculated values for capacitances C_1, C_2, C_3 and C_0 are 10 μF, 15 μF, 15 μF, and 100 μF respectively. The load resistance is equal to 200 Ω. The converter specification and design parameters are listed in Table-2.3.

The proposed converter is tested in continuous current mode. Fig-2.7 shows the profile of input and output voltage. The converter is operated at 0.16 duty cycle. At 43 V input, the output voltage is equal to 200 V which is slightly lesser (10 V) as compared to

theoretical value. The drop in output voltage is due to forward voltage drop of diodes, switches voltage drop and passive elements voltage drop.

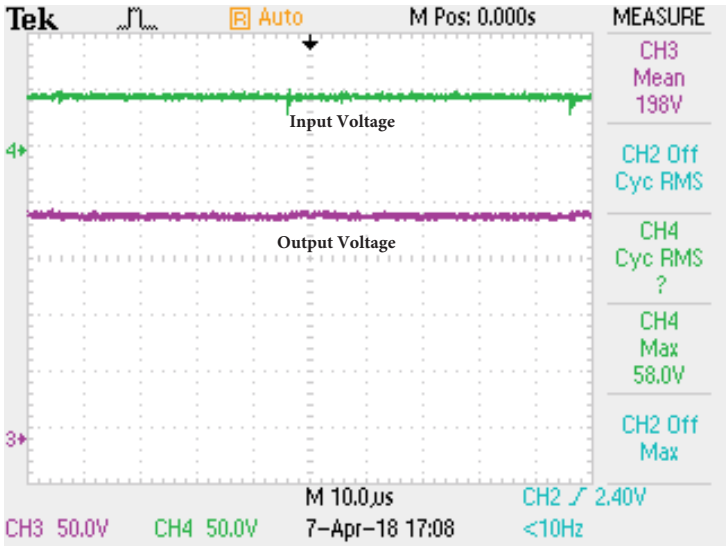


Figure 2.7: Input and output voltages $[Ch3 : 50V/div, Ch4 : 50V/div]$

The profile of inductor current through L_1 and L_2 is shown in Fig-2.8. The zoomed inductor currents are shown in Fig-2.9. As soon as the switches S_1 and S_2 are turned ON, the inductor current increases, while the switches S_1 and S_2 are turned OFF, the inductor current decreases. The input voltage source is always connected to inductor, therefore, the current at input is continuous in nature.

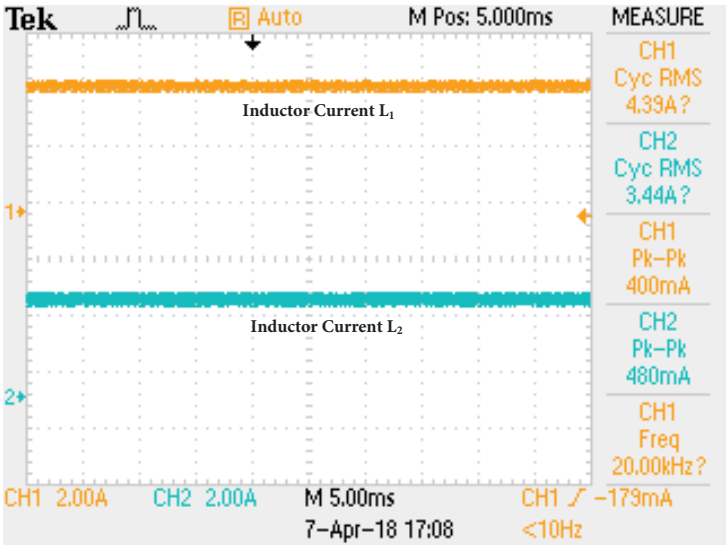


Figure 2.8: Inductors current in L_1 and L_2 $[Ch1 : 1A/div, Ch2 : 1A/div]$

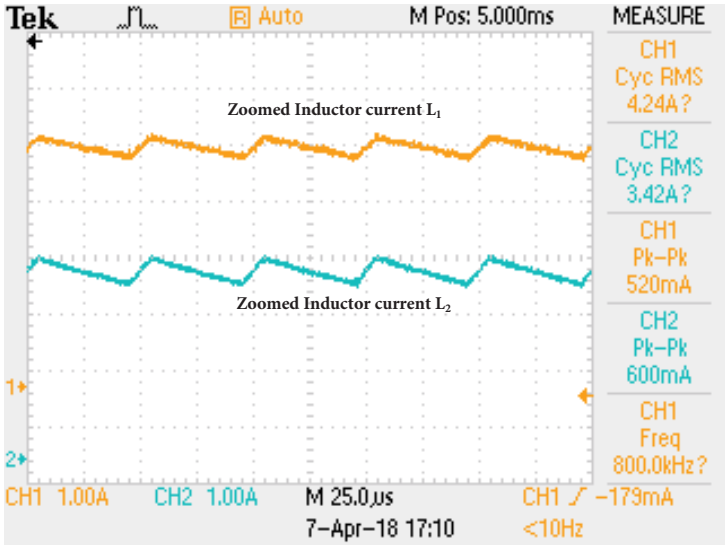


Figure 2.9: Zoomed inductors current in L_1 and L_2 $[Ch1 : 1A/div, Ch2 : 1A/div]$

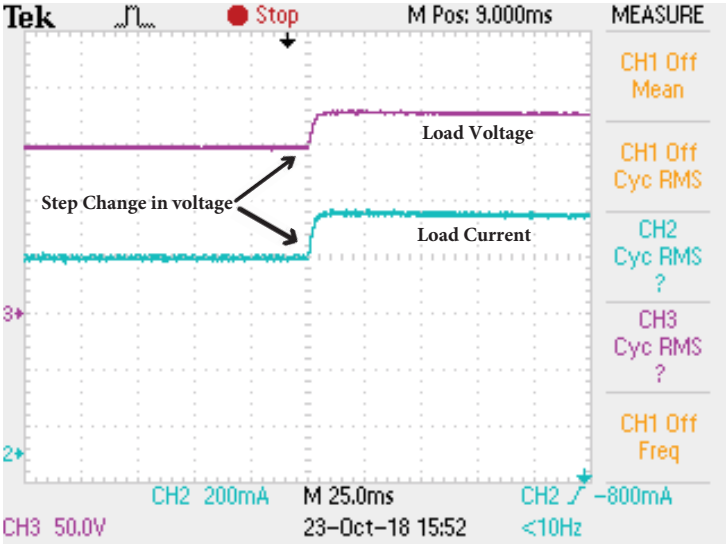


Figure 2.10: Step change in load voltage

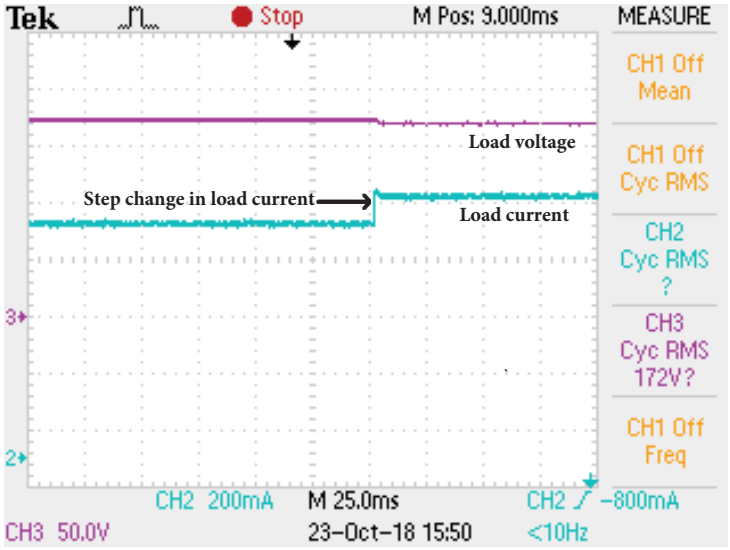


Figure 2.11: Step change in load current

For evaluating dynamic performance of the proposed converter, two distinct cases are considered. In first case, a step change in load voltage initiated. The load voltage is changed from 150 V to 175 V, eventually, the load current changes accordingly which is shown in Fig-2.10. In the second case, the load voltage and input voltage is kept constant while the load is switched to 8% higher current rating. The load current is changed from 0.8 A to 0.86 A as shown in Fig-2.11. Due to step change in load current, there is small drop in output voltage which is due higher voltage drop across passive elements at higher current.

For performance evaluation of the converter in terms of efficiency, the converter is tested at seven different power levels by varying the input voltage. Due to power loss in passive elements, diodes and switches, the maximum efficiency of the converter is measured as 93.33%. At other power levels, the efficiency measured is above 90% which is suitable for PV applications.

2.6 Conclusion

A high gain DC-DC converter which utilizes the concept of switched inductor/switched capacitor is reported in this paper. The main feature of the converter are as follows: A simple structure which achieves high voltage gain at smaller duty cycle. This reduces the conduction loss of the power switches, and also lowers the voltage stress across MOSFET

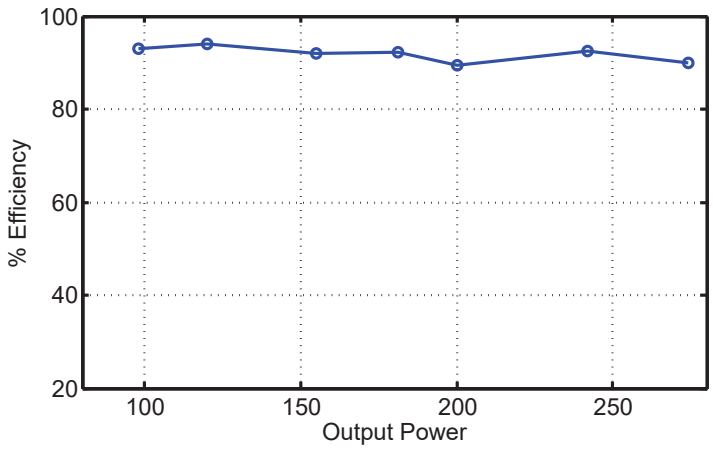


Figure 2.12: Experimental efficiency

and diodes. The converter has lesser number of components count and better efficiency as compared to its contemporary converters. The performance of the converter is validated in CCM and design analysis for different components is presented. The converter is tested at 200 W power rating, and maximum 93.33% efficiency is achieved.

Since HEV has both AC and DC loads, therefore, after covering the DC-DC converter in this chapter, the next chapter will discuss DC-AC Z-source inverters for energising AC loads.

Chapter 3

Modified Switched Boost Inverter For wide Duty Cycle Operation

3.1 Introduction

The Z-source converter [56] since its inception is quiet popular in power electronic research community. A few of its salient features include single stage conversion, wide range of load regulation, no dead time requirement and immunity to EMI. The prime motive of the various derived topologies is the huge gain, reduced count of circuit elements and minimum stress [107]. Z-source converter has following operating states- active, shoot-through and zero. The profile of the inductor current during these states broadly define whether the converter operates in CCM or DCM. Unlike established CCM and DCM, a peculiar constant inductor current phenomenon occurs which is responsible for non-zero discontinuous mode (NZ-DCM) in the certain Z-source converter.

The converters containing NZ-DCM in their operation have a common feature, i.e., during active or zero states, a diode in series with a capacitor is connected parallel across the inverter. Due to a specific arrangement of circuit elements, NZ-DCM appears, keeping the inductor current almost constant up to the next zero state. The NZ-DCM creates the potential threat to stiff DC link voltage resulting in higher THD at AC load terminal. This effect further degrades the performance of the load. To demonstrate NZ-DCM, switched boost inverter(SBI) is selected which has aforementioned feature to have NZ-DCM. However, this theory can be extended to other Z-source converters.

The SBI is operated for high AC load current along with low duty cycle condition.