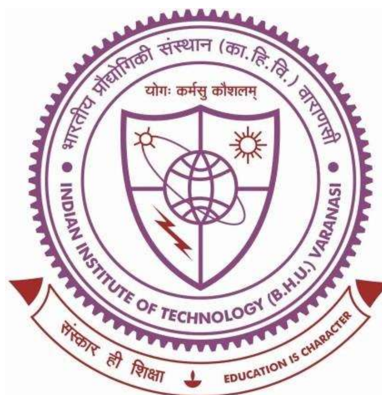
Performance Investigation of Some Heterojunction TFETs on SELBOX Substrates: Application to Dielectric Modulated Label-Free Biosensors



Thesis submitted in partial fulfillment for the Award of Degree

Doctor of Philosophy

By

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Summary Conclusion and Future Scope

7.1 Introduction

The major objective of this thesis is to enhance the performance of TFET using SELBOX substrate and different engineering techniques (i.e., Heterojunction engineering and Gate oxide stack engineering) through TCAD analysis. SELBOX substrate provides thermal insulation and lowers the leakage current over FD-SOI TFET. Various engineering techniques such as horizontal and vertical gate oxide engineering, heterojunction engineering, gate material engineering and use of III-IV material over SELBOX substrate have been studied to enhance the electrostatic performance and trapped charges reliability of TFET. Effect of back gate on engineered STFET (SELBOX-TFET) is also analyzed in detail. Finally an optimized STFET structure is proposed. The optimized STFET structure is then used for dielectric modulated label free bio-senseing application. Further, IV-IV material (Ge/Si heterojunction) is replaced with III-V material (GaSb/GaAs heterojunction) to increase the sensitivity of the bio-sensor. An important overview of the work contained in this thesis is summarized here.

7.2 Chapterwise Contributions and Conclusion

Chapter 2 proposes an electrostatic comparison between conventional fully depleted SOI TFET and proposed *Heterojunction TFET on SELBOX Substrate*. This chapter discusses the advantages of the proposed TFET structure over the conventional fully depleted SOI TFET structure. The major observations can be given as follows:

- This work investigates the DC and Analog/RF performance of a newly suggested GSHJ-STFET-based TFET structure with stacked HfO_2/SiO_2 gate and Ge (source)/Si (channel) heterojunction.
- The rapid rate of BTB tunneling of carriers from the source to the channel region is due to the presence of germanium (a low bandgap material) in the source region.
- It has been shown that the SELBOX structure demonstrates the advantages over SOI and bulk structures. So, it can be considered a good option while selecting between SOI and bulk structures. This is mainly due to the gap present in the buried oxide in the SELBOX structure.
- The SELBOX substrate has been used in the proposed TFET to reduce the lattice heat and improve the I_{ON}/I_{OFF} ratio.
- Vertical gate stacked SiO_2/HfO_2 is highly responsible for the reduction of the gate leakage current due to the higher physical thickness of the gate oxide layer. The proposed TFET structure with SELBOX improves both DC and RF characteristics.
- The ATLAS™ TCAD tool which is commercially available has been utilized to simulate the devices throughout a temperature range of 250 to 400 K. The influence of temperature on the suggested GSHJ-STFET structure's performance is shown to be minimal over the GSHJ-FD-SOITFET structure. This makes GSHJ-STFET ideal for low-power applications

Chapter 3 investigates the influence of both the donor and acceptor type interface trap charges (ITCs) on the reliability of LS-STFET and VS-STFET in terms of their DC, analog/RF, and linearity parameters. This is a comparative analysis work based on their DC/RF and linearity parameters. The major observations in chapter 3 are given following.

- The presence of ITCs causes more severe effects on the performance degradation of VS-STFET than the LS-STFET structure. Thus, the proposed LS-STFET is more reliable than the VS-STFET device structure.
- Therefore, the LS-STFET device structure can be considered a promising MOS device for low-power and high-frequency applications.
- The ATLAS™ TCAD tool which is commercially available has been utilized for the simulation of both proposed TFETs.

Chapter 4 reports the device-level simulation analysis of a back-gated Ge/Si heterojunction TFET on SELBOX substrate (BG-HJ-STFET). There are some major points listed below about chapter 4:

- The proposed structure implements a stacked gate oxide where the conventional SiO_2 is replaced by a SiO_2/HfO_2 in a stacked manner to increase its On-current.
- A back gate (BG) is also considered in the proposed TFET to enhance the device-level performance.
- Investigation of DC, RF, and linearity parameters such as drain current, transconductance, electric field, parasitic capacitance, cut-off frequency (f_T), gain-bandwidth product (GBP), intrinsic delay (τ), higher-order of g_m (gm_2, gm_3), VIP2, VIP3, IIP3, IMD3, and 1-dB compression point are carried out for the proposed TFET and the results are compared with other conventional structures.
- Finally, we have discussed back gate effects on the performance of the proposed TFET.
- Performance evaluation shows that BG-HJ-STFET is a suitable candidate for distortionless and high-frequency applications.

Chapter 5 reports the device-level performance of a back gated ferroelectric heterojunction TFET on SELBOX substrate (BG-Fe-HJ-STFET). The proposed structure implements a stacked gate oxide where the conventional SiO_2 is replaced by a

SiO_2/ferroelectric oxide in a stacked manner to increase its on-current. The following major points of this chapter are listed below.

- Investigation of DC, RF, and linearity parameters such as drain current, transconductance, electric field, parasitic capacitance, cut-off frequency (f_T), gain-bandwidth product (GBP), intrinsic delay (τ), higher-order of g_m (gm_2, gm_3), VIP2, VIP3, IIP3, IMD3, and 1-dB compression point are carried out for the proposed TFET and the results are compared with other conventional structures.
- The internal voltage amplification with the ferroelectric (FE) effect was beneficial to the subthreshold range, while the BTBT boost was slightly enhanced by the saturation current. The performance of a steep subthreshold slope device with an integrated FE could be improved in future applications by optimizing the device structure and processing conditions.
- The sensitivity of the BG-Fe-HJ-STFET-based biomolecule sensor has been performed on different dielectric constant values (k = 3, 5, 7, 10, and 12) of biomolecules.
- Performance evaluation shows that BG-Fe-HJ-STFET is a more suitable candidate for distortionless and high-frequency applications as compared to BG-HJ-STFET.

Chapter 6 investigates the performance of SiO_2/ferroelectric oxide stacked back-gated Ge/Si heterojunction STFETs (BG-Fe-HJ-STFET) based dielectric modulated label-free biosensor. Cavities in the ferroelectric gate-oxide of the studied TFET are created. These cavities contain the biomolecules to be sensed through the principle of gate-dielectric modulation. The main results of chapter 6 can be written as follows:

- The threshold voltage sensitivity (S_{VT}) and I_{ON}/I_{OFF} sensitivity parameters of the proposed BG-Fe-HJ-STFET structure have been thoroughly investigated considering different biomolecules.
- The proposed BG-Fe-HJ-STFET structure is shown to have the higher current sensitivity (~ 4.2×10^{11}) and threshold voltage sensitivity (0.38V) values over some recently reported TFET based biosensors.

Chapter 7 studies the sensitivity analysis of SiO_2/HfO_2 oxide stacked GaSb/GaAs type-II heterojunction STFETs based dielectric modulated label-free biosensor. Cavities in the HfO_2 of the studied TFET are created. These cavities contain the biomolecules to be sensed through the principle of gate-dielectric modulation. The main results of chapter 7 can be written as follows:

- The threshold voltage sensitivity (S_{VT}) and I_{ON}/I_{OFF} sensitivity parameters of the proposed DM-HJ-STFET structure have been thoroughly investigated considering different biomolecules.
- The proposed DM-HJ-STFET structure is shown to have the higher current sensitivity (~ 6.67×10^{11}) and threshold voltage sensitivity (0.37V) values over some recently reported TFET based biosensors.

7.3 Future Scope of Work

The works presented in this thesis have a wider scope for researchers working in the domain of TFETs.

- Although we have designed Ge/Si heterojunction TFET on SELBOX substrate (HJ-STFET) but there are lots of technologies that can be further used for the performance improvement of the proposed TFETs.

- In the proposed TFETs, we have used Ge (germanium) as a low bandgap material in the whole thesis but in the future readers can implement this TFETs structure for the different compound semiconductors such as III-V compound semiconductors etc.
- The proposed Ge/Si heterojunction TFET on the SELBOX substrate, having a channel length below 10 nm can be investigated to study the Quantum Mechanical Effects on its device and circuit level performances.
- Gate structure and source material engineering of our proposed device based on Ge/Si heterojunction TFET on SELBOX substrate also guidelines for other device structures such as vertical TFETs, Fin-TFETs, Tri-gate, and Ring TFETs. The device and circuit level analysis presented in this thesis for Ge/Si heterojunction TFET on SELBOX substrate may be a good foundation to analyze the device and circuit level performance for these devices.
- Gate structure and source material engineering of our proposed device based on Ge/Si hétérojonction TFET on SELBOX substrate also guideline for other device structures such as vertical TFETs, Fin-TFETs, Tri-gate, and Ring TFETs. The device and circuit level analysis presented in this thesis for Ge/Si hétérojonction TFET on SELBOX substrate may be a good foundation to analyze the device and circuit level performance for these devices.
- In the future, our proposed TFET structure can be implemented in the design of circuits such as inverters, logic circuits, SRAM, DRAM etc.