Preface

Scaling of a MOS transistor, deals with the reduction in the dimensions of the device to increase the transistor density per unit area of the chip in integrated circuit (IC) technology. However, in practice, the performance of the MOS transistors is degraded severely with the reduction in gate length in the nanoscale regime. The major problem associated with the scaling is the degradation of subthreshold characteristics in terms of threshold voltage, subthreshold current (SC) and subthreshold swing (SS), and drain induced barrier lowering (DIBL) which are collectively known as short-channel-effects (SCEs). Therefore, the suppression of the SCEs up to certain acceptable level is the utmost important to sustain further scaling of the MOSFETs for the development of future generation ICs. In this direction, the conventional bulk MOSFETs have been replaced by many non-conventional MOS structures such as the single and multi-gate silicon-on-insulator (SOI) MOSFETs, Junctionless transistors, Tunnel FETs etc. In addition to the basic structural changes, different techniques such as the channel engineering (i.e. use of strained-Si channel, different channel materials other than Si, different channel doping profiles other than the conventional uniform doping in the channel etc.), gate engineering (i.e. use of single and multiple gate structures with different gate electrode materials other than poly-Si, high-*k* dielectrics in place of SiO_2, combination of different materials with different work functions in cascade to form gate electrode etc.) and source/drain engineering (i.e. use of different materials such as Ge and SiGe for source and drain, raised source/drain electrodes etc.) have been explored by the researchers to improve the SCEs in the MOS transistors. Channel engineered dual-material double-gate MOSFETs have been explored as the remedies to solve small geometry related issues. Subthreshold characteristics of the graded channel and strained-Si channel DG MOSFETs with dual-material-gate (DMG) engineering are reported to have better performance than the conventional DG MOSFETs. Lateral graded-channel (GC) doping engineering (obtained by maintaining a high doping near the source end and a low doping at the drain end) has been explored for achieving improved drive current, reduced short-channel effects (SCEs) and reduced hot-carrier effects (HCEs). The low doped region near the drain end reduces the electric field

thereby reducing the impact ionization and hence the HCEs at the drain side of the device. However, the strained-Si channel MOSFETs enhances the speed of operation of the transistor but at the cost of increased DIBL and HCEs. The DMG electrode structure in MOS devices may be used to reduce both the SCEs and HCEs. In such structures, the entire gate electrode over the gate-oxide consists of the two non-overlapping regions of two different materials: the larger work function material is placed near the source side (i.e. called the control gate) while the lower work function material is placed near the drain side (i.e. called the screen gate). The sum of the control and screen gate lengths becomes equal to the total gate length of the device. The difference in the work functions of the gate-electrode materials used for the control and screen gates introduces a step-function like shape in the channel potential profile which can be explored for reducing the electric field at the drain side to reduce the HCEs and DIBL characteristics of the device. The objective of the present thesis is to develop some theoretical analyses for investigating the effects of graded-channel (GC) engineering, strain-channel engineering and Gaussian doping channel engineering on the subthreshold characteristics of the DMDG MOSFETs. The thesis consists of SIX chapters which are briefly outlined in the following:

Chapter-1 introduces the principle of MOSFET scaling and different CMOS technology boosters like structural engineering, gate engineering, and channel engineering to reduce SCEs in the MOS transistors. A detailed literature survey has been carried out to define the scopes of the present thesis.

Chapter-2 deals with the analytical modeling of surface potential and threshold voltage of the graded-channel dual-material double-gate (GCDMDG) MOSFETs obtained by intermixing the concepts of graded channel doping engineering and dual material gate engineering in the MOSFETs. The surface potential model has been obtained by solving the 2D Poisson's equation using parabolic approximation method. The surface potential has been explored for modeling the threshold voltage of the GCDMDG MOSFETs. The effects of different device parameters on channel potential and threshold voltage characteristics have been investigated and compared with the 2D ATLAS™ TCAD simulation data to show the validity of the proposed models.

Chapter-3 presents the modeling and ATLAS^{TM} based simulation of the subthreshold-current (SC) and subthreshold-swing (SS) of the GCDMDG MOSFETs proposed in Chapter-2. The potential model of Chapter-2 has been directly used to model SC and SS characteristics of the device by exploring the concept of an effective conduction path for the subthreshold current in the DG MOS structures. The effects of different device parameters on the SC and SS have been discussed.

Chapter-4 deals with the 2D modeling of the potential and threshold voltage of an ion-implanted strained-Si (s-Si) DMDG MOSFET with a vertical Gaussian-like doping profile. The effects of different device parameters (such as device channel length, gate length ratios, germanium mole fraction) and doping parameters (such as projected range, straggle parameter) on the threshold voltage of the proposed structure have been investigated. It is observed that in addition to the peak doping, the straggle and projected range parameters of the Gaussain-like doping profile may provide additional flexibility for optimizing the subthreshold characteristics of the device. The model results have been validated through a good matching between the theoretical results and ATLAS™ simulation data.

Chapter-5 presents the analytical modeling of the SC and SS characteristics of the ion-implanted strained-Si (s-Si) double-material double-gate (DMDG) MOSFETs considered in Chapter-4. The potential model derived in Chapter-4 has been directly used for modeling the SC and SS in the similar manner as carried out for GCDMDG MOSFETs in Chapter-3. The dependence of SC and SS on various device parameters such as gate length ratio, Ge mole fraction, peak doping concentration, projected range, straggle parameter etc. has been studied in details. The model results have also been compared with the ATLAS™ for the validity of the proposed models.

Chapter-6 includes the summary and conclusions of the thesis. The major findings of the present study are summarized in this chapter. Finally, a brief discussion on the future scope of research in the related areas of the present thesis is also presented in this chapter.