# Chapter 6

## *Conclusion and Future Scope*

### 6.1 Introduction

The objective of this thesis is to develop some analytical models for the subthreshold characteristics of channel engineered dual-material double-gate MOSFETs presented in Chapters 2-5 in this thesis. The effects of three different channel engineering techniques namely the lateral graded channel (GC) doping engineering, strained-Si channel engineering and vertical Gaussian channel doping profile engineering on the subthreshold performance of the DMDG MOS structures have been investigated in the present thesis. In this chapter, we will summarize and conclude the major observations presented in the various chapters of this thesis. Finally, we will also outline some scopes for the future research related to area considered in this thesis.

### 6.2 Summary and Conclusion of Various Chapters

**Chapter-1** discusses a brief introduction to IC technology, CMOS scaling and non-classical CMOS device structures. Various MOSFET scaling techniques and their effects on the performance of the CMOS devices have been briefly discussed. Various CMOS technology boosters including various channel engineering and gate-material engineering techniques have also been introduced. A detailed literature survey on the strained-Si (s-Si)

channel MOSFETs and graded channel (GC) MOSFETs has been carried out. Finally, based on the major findings of the literature survey summarized in the thesis, the scopes of the present thesis have been outlined at the end of this chapter.

**Chapter-2** includes the analytical modeling and ATLAS$^{TM}$ TCAD based simulation of surface potential and threshold voltage of graded-channel dual-material double-gate (GCDMDG) MOS structures obtained by combining concepts of graded-channel (GC) and dual-material-gate (DMG) engineering in the DG MOSFETs. In the GCDM engineering, the lateral channel region has been divided into two non-overlapped regions under the control gate and screen gate with respective doping concentrations of $N_{a1}$ (at the source side) and $N_{a2}$ (at the drain side) where $N_{a1} > N_{a2}$. The parabolic approximation method has been explored for obtaining the surface potential function of the device by solving the 2D Poisson's equation with suitable boundary conditions. The effects of different device parameters on the potential and threshold voltage of the proposed GCDMDG MOSFETs have been modeled and discussed in this chapter. The merits of the GCDMDG MOS structures over the graded-channel double-gate (GCDG) and dual-material double-gate (DMDG) MOS structures have also been discussed. The major observations can be summarized as follows:

- The source-to-channel barrier height (and hence the threshold voltage) can be enhanced by increasing the $L_1 : L_2$ ratio.
- The position of the minimum surface potential is shifted towards the drain with the increase in the $L_1 : L_2$ ratio which may be explored for optimizing the threshold voltage roll-off of the proposed GCDMDG MOS structures.

- Both the threshold voltage and its roll-off can be improved by increasing the channel doping ( $N_{a1}$ ) of the source side due to the increase in the source-to-channel barrier height.
- The performance degradation of the device due to increased threshold voltage roll-off, DIBL and HCEs with the decrease in the channel length can be effectively reduced/controlled by selecting the appropriate values of control-to-screen gate length ratio ($L_1$:$L_2$), doping concentrations ( $N_{a1}$ and $N_{a2}$ ) of the two regions of the graded-channel and the work functions of the control and screen gates of DMG structures.
- GCDMDG MOSFETs possess better immunity to the SCEs over the GCDG MOSFETs and DMDG MOSFETs.
- All the model results are well-matched with the commercially available ATLAS$^{TM}$ based TCAD simulation data which show the validity of our proposed analytical models developed in this chapter.
- To the best of our knowledge, the modeling of surface potential and threshold voltage of the GCDMDG MOSFETs is reported for the first time in this thesis.

**Chapter-3** presents the modeling and ATLAS$^{TM}$ based simulation of the subthreshold current (SC) and subthreshold swing (SS) of the GCDMDG MOSFETs proposed in Chapter-2. The potential function obtained in Chapter-2 has been used to formulate the SC while the effective subthreshold conduction path concept has been used for modeling the SS of the device. The variations of SC and SS against different device parameters have been discussed in details. The SC and SS characteristics of the

proposed GCDMDG MOS transistor have been compared with the conventional DMDG and GCDG MOS structures. The effects of different device parameters like channel length, control-to-screen gate length ratio, channel thickness, doping concentration etc. have been investigated on the subthreshold characteristics of the device. The major observations of this chapter can be outlined as follows:

- The effective conduction path parameter ( $d_{eff}$ ), is a hypothetical distance measured from the channel center of the device which represents the total effective subthreshold current flowing path between the source and drain in the DG MOS structure. An analytical model for $d_{eff}$ has been developed for the proposed GCDMDG MOSFETs to model the SS of the device.
- The deterioration in the SC and SS with decreased channel length can be minimized by choosing appropriate values of $N_{a1}$ and $N_{a2}$, and $L_1 : L_2$ ratio of the proposed GCDMDG MOS structure.
- The increased values of $L_1/L_2$ ratio, helps in reducing the SC and SS characteristics of the device effectively.
- The SC increases with the channel thickness.
- Theoretical results of the proposed model show a good matching with the ATLAS$^{TM}$ based TCAD simulation data.

**Chapter-4** reports the 2D analytical modeling of the surface potential and threshold voltage of ion-implanted strained-Si (s-Si) double-material (DM) double-gate (DG) MOSFETs by incorporating the features of both the s-Si channel and DMDG structure in a single MOSFET with a vertical Gaussian-like channel doping profile. The surface

potential has been modeled by solving the 2D Poisson's equation following the similar method as described in Chapter-2. The surface potential function has been used to finally model the threshold voltage of the proposed device. The effects of different device parameters (e.g. channel length, gate length ratios, germanium mole fraction, channel thickness, gate-oxide thickness etc.) and doping parameters (i.e. projected range, straggle and peak doping concentration) on the potential and threshold voltage of the proposed structure have been investigated. Some important observations of this chapter are briefly discussed in the following:

- The actual non-integrable Gaussian doping profile of an ion-implanted channel has been replaced by a Gaussian-like double-integrable analytic function for the simplicity of the model.
- To the best of our knowledge, the effects of strain in an ion-implanted Si-channel on the potential and threshold voltage of the DMDG MOSFETs have been investigated for the first time in this thesis.
- The minimum of the surface potential always occurs in the control gate region due to higher work function of the gate electrode material of the DMG structure.
- The threshold voltage of the device can be improved by simply controlling the projected range and straggle parameter of the Gaussian-like doping profile while maintaining other device parameters constant. Thus, the projected range and straggle parameters provide us additional flexibilities for optimizing the subthreshold characteristics of the s-Si DMDG MOSFETs.
- Threshold voltage is increased with the peak doping concentration $N_p$ of the Gaussian doping due to increased barrier height at the source/channel junction.

- For a fixed channel length, the threshold voltage of the device is increased with control-to-screen gate length ratio $L_1 : L_2$ (while maintaining constant gate length $L = L_1 + L_2$).
- The model results are in good agreement with the simulation data obtained by using ATLAS™ TCAD tool.

**Chapter-5** presents the analytical modeling of the subthreshold current (SC) and subthreshold swing (SS) characteristics of the ion-implanted s-Si DMDG MOSFETs proposed in Chapter-4. The surface potential model of Chapter-4 has been directly used to model the SC and effective subthreshold conduction path concept discussed in Chapter-3 has been used to model the SS of the proposed device. The dependence of SC and SS characteristics on various device parameters such as gate length ratio, Ge mole fraction, peak doping concentration, projected range, straggle parameter etc. has been studied. The major observations of this chapter are discussed below:

- The resultant subthreshold current conduction path parameter ( $d_{eff}$ ) of the proposed device has been modeled following the similar method as discussed in Chapter-3.
- The subthreshold current gets increased with the increased strain in the Si channel due to reduced built-in potential at the source/channel junction.
- Increase in $L_1$:$L_2$ ratio reduces the subthreshold current due to increase in the source to channel barrier height.
- Keeping the position of peak doping concentration in the middle of the channel i.e. ($R_p=0$) gives minimum value of SC.

- Subthreshold swing (SS) is degraded with the increased gate oxide thickness due to the reduction in the gate control over the channel. However, the deterioration in the SS can be improved by increasing the doping concentration in the channel.
- The SS can be controlled by controlling $L_1$:$L_2$ ratio. The SS gets reduced with the increase in $L_1$:$L_2$ ratio.
- The modeling results are well matched with the simulation data obtained by the ATLAS™ TCAD simulator which confirms the validity of our proposed models of the SC and SS reported in this chapter for the proposed s-Si DMDG MOSFETs with a vertical Gaussian-like doping profile.

## 6.3 Future Scopes of Work

In this thesis, we have presented the 2D analytical modeling of the subthreshold characteristics of some channel engineered dual-material double-gate MOSFETs. In this section, we will outline some future scopes of research related to the area of research carried out in this thesis which are given as following:

- In the present work, we have considered channel thickness more than 10 nm to avoid the effects of quantum mechanical effects (QMEs) for the simplicity of our models. However, the effects of QMEs may be included in the modeling of subthreshold characteristics of the GCDMDG and s-Si DMDG MOSFETs for improving their accuracy over any gate-lengths and channel-thicknesses.
- An extensive study of GCDMDG and s-Si DMDG MOSFETs for analog and RF applications can be carried out.

- Equivalent circuit models of the GCDMDG and s-Si DMDG MOSFETs for both the low and high frequencies could be very useful for the design and simulation of the GCDMDG and s-Si DMDG MOSFET based analog and digital circuits.
- The modeling presented in this thesis for DG MOSFET may be extended for the FinFETs, Tri-gate and Gate-All-Around (GAA) MOSFETs. The concepts can also be applied for other channel engineered non-classical MOSFET structures like the Junctionless Field Effect Transistors (JFETs), Tunnel Field Effect Transistors (TFETs), Ring MOSFETs etc.
- A continuous drain current model valid in all regimes of the device operation for short-channel GCDMDG and s-Si DMDG MOSFET can be worked out.
- A capacitance model of short-channel GCDMDG and s-Si DMDG MOSFET could be proposed.