Chapter 5

Analytical Modeling of Subthreshold Current and Subthreshold Swing of Ion-Implanted Strained-Si Dual-Material Double-Gate MOSFETs

5.1 Introduction

Besides the threshold voltage, the subthreshold current (SC) and subthreshold swing (SS) play important roles in determining the static power loss and switching performance characteristics of any MOS transistor. Thus, after modeling the surface potential and threshold voltage of the ion-implanted strained-Si DMDG MOSFETs with a vertical Gaussian-like channel doping profile in Chapter-4, we will now consider the analytical modeling of the SC and SS of the device in the present chapter. The SC has been derived by using the surface potential model taken directly from Chapter-4. The concept of effective conduction path parameter [Chen *et al.* (2002), Dey *et al.* (2008), Dubey *et al.* (2011)] has been used to model the SS of the ion-implanted s-Si DMDG MOSFETs in the similar manner as considered in Chapter-3. The effects of different device and doping profile parameters on SC and SS have been studied in details. We have compared the theoretical results with the ATLAS^{TM} TCAD simulation data to validate the proposed SC and SS models presented in this chapter. The layout of the present chapter can be given as follows:

In Sec. 5.2, the channel potential model derived in Sec. 4.2 has been used for modeling the SC of the ion-implanted s-Si DMDG MOSFETs. Using the concept of effective subthreshold conduction path parameter considered in Chapter-3 for GCDMDG

MOSFETs, we have also modeled the SS of the proposed device in this section. Some important model results have been discussed in Sec. 5.3. The model results have also been compared with the related ATLAS based TCAD simulation data for validating the proposed models. Finally, Sec. 5.4 includes conclusion of the present chapter.

5.2 Model Derivation

Figure 5.1 shows the cross-sectional view of s-Si DMDG MOSFET where the channel length, s-Si film thickness and thickness of front as well as back SiO_2 layers are represented by the notations L, t_{s-Si} , t_{ox} respectively. However, Chapter-4 presented the channel potential and threshold voltage models of same MOS structure, still the structure is redrawn here for easy understanding. The x-axis and y-axis of the 2-D structure are taken along the center of the channel and the source-channel interface, respectively, as shown in the figure. The channel is considered to be divided into two parts of respective lengths L_1 and L_2 having metal gate work function ϕ_{m1} and ϕ_{m2} respectively, where total channel length $L = L_1 + L_2$ and $\phi_{m1} > \phi_{m2}$. ϕ_{m1} and ϕ_{m2} are the work functions of the gate material near the source and the drain region respectively, as already discussed in Chapter-4. The Gaussian-like doping profile is taken in the vertical direction of the channel. Subscripts f and b are used for the front and back surface related parameters, respectively. Channel length and gate oxide thickness of the device are taken as 40 nm and 2 nm respectively. To study the subthreshold behavior, the device is operated under subthreshold regime i.e. below threshold. The 2D numerical simulation has been carried out in the similar manner as in Chapter-4 by using

ATLAS™, a 2D device simulator. *I–V* characteristics are predicted by drift-diffusion (DD) model. To take account of recombination effects, we have used Shockley-Read-Hall (SRH) model. This simulates the leakage currents that exist due to thermal generation. The transverse field, doping dependent and temperature dependent parts of the mobility are modeled by CVT model as used in Chapter-4.

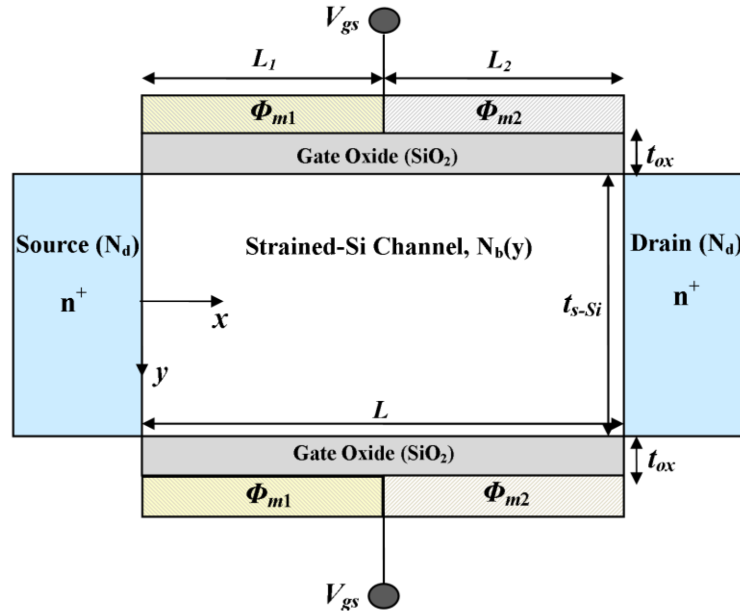

Fig. 5.1: Cross-sectional view of strained-Si double-material double-gate (DMDG) MOSFET

The Gaussian-like doping profile, assumed to be same as in chapter-4, is reproduced here as

$$N_b(y) \cong N_p\, c\left[(a+2b\alpha Y)^2 - 2b\right]\exp\left(-a\alpha Y - bY^2\right) \tag{5.1}$$

where N_p is the peak doping concentration at $y = R_p$, (R_p is the projected range); $Y = \frac{y - R_p}{y_b}$, $y_b = \sqrt{2}\,\sigma_p$ (σ_p is the straggle parameter of the Gaussian Function); a, b and c are the fitting parameters with values $a = 1.786$, $b = 0.646$ and $c = 0.56$; $\alpha = +1$ for $y \geq 0$ and -1 for $y \leq 0$ [Dubey *et al.* (2010a)].

It is mandatory to mention here that in the present chapter is the continued work of Chapter-4, so the same nomenclature used in Chapter-4, will be used in the present chapter, for all the device parameters. Further we will use some of the results directly from Chapter-4 in the present chapter. Effect of strain on bandgap and flatband voltage is already explained in Chapter-4.

5.2.1 Modeling of Subthreshold Current

As diffusion is the dominant process for current flow in subthreshold regime, the SC can be expressed as [Kumar *et al.* (2013c), Dubey *et al.* (2010b)]

$$I_s = \int_{-\frac{t_{s-Si}}{2}}^{\frac{t_{s-Si}}{2}} J_n(y)\,dy \tag{5.2}$$

where the SC is calculated in $A/\mu m$ i.e. current per unit channel width in the present paper. $J_n(y)$ is the current density and can be expressed as [Kumar *et al.* (2013c)]

$$J_n(y) = \frac{qD_n n_{\min}(y)}{L_e}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{5.3}$$

where D_n is diffusion constant, V_T is the thermal voltage, L_e is effective channel length, V_{ds} is the drain-to-source voltage, and

$$n_{\min}(y) = \frac{n_i^2}{N_p}\exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) \tag{5.4}$$

being the carrier concentration at the virtual cathode (already explained in Chapter-4), where n_i represents the intrinsic concentration and $\phi_{1,\min}(y)$ is the channel potential of region 1 at the virtual cathode, given by

$$\phi_{1,\min}(y) = \phi_1(y)\big|_{x=x_{1,\min}} \tag{5.5}$$

The effective channel length L_e can be expressed as [Dubey *et al.* (2011), Dubey *et al.* (2010b)]

$$L_e = L - L_s - L_d + 2L_D \tag{5.6}$$

where L_D is extrinsic Debye channel length, given below [Dubey *et al.* (2011), Dubey *et al.* (2010b)]

$$L_D = \left(\frac{\varepsilon_{Si}V_T}{qN_p}\right)^{1/2} \tag{5.7}$$

L_s and L_d are source channel and drain channel depletion widths, given as [Dubey *et al.* (2011), Dubey *et al.* (2010b)]

$$L_s \approx \left(\frac{2\varepsilon_{Si}\left(V_{bi,s-Si}(y_{\min}) - \phi_{1,\min}(y_{\min})\right)N_d}{N_p\left(N_p + N_d\right)}\right)^{1/2} \tag{5.8}$$

$$L_d \approx \left(\frac{2\varepsilon_{Si}\left(V_{bi,s-Si}(y_{\min}) + V_{ds} - \phi_{1,\min}(y_{\min})\right)N_d}{N_p\left(N_p + N_d\right)}\right)^{1/2} \tag{5.9}$$

where, $\phi_{1,\min}(y_{\min}) = \phi_{1,\min}(y)\big|_{y=y_{\min}}$ (5.10)

where $y_{\min}$ can be obtained by putting

$$\frac{\partial \phi_{1,\min}(y)}{\partial y} = 0 \tag{5.11}$$

Further, $V_{bi,s-Si}(y_{\min})$ is the built-in voltage of strained silicon at $y = y_{\min}$ and obtained by the method explained in Chapter-4

$$V_{bi,s-Si}(y_{\min}) = V_{bi,s-Si}(y)\big|_{y=y_{\min}} \tag{5.12}$$

$$V_{bi,s-Si}(y)\big|_{y=y_{\min}} = V_{bi,Si}(y)\big|_{y=y_{\min}} + \Delta V_{bi} \tag{5.13}$$

where $V_{bi,Si}$ is the built-in voltage for unstrained silicon and can be expressed as given in Chapter-4

$$V_{bi,Si}(y)\big|_{y=y_{\min}} = V_T \ln\left(\frac{N_{b,\min} N_d}{n_i^2}\right) \tag{5.14}$$

where, $N_{b,\min} = N_b(y)\big|_{y=y_{\min}}$ (5.15)

Using Ref. [28]

$$N_b(y)\big|_{y=y_{\min}} = N_p\, c\left[(a + 2b\alpha Y_{\min})^2 - 2b\right]\exp\left(-a\alpha Y_{\min} - bY_{\min}^2\right) \tag{5.16}$$

where $Y_{\min} = \dfrac{y_{\min} - R_p}{y_b}$ (5.17)

The total current I_s, of the device can be assumed as the addition of the current I_{sf} (for $-\frac{t_{s-Si}}{2} \le y \le y_{\min}$) due to front region and the current I_{sb} (for $y_{\min} \le y \le \frac{t_{s-Si}}{2}$) due to back region of the channel [Dubey *et al.* (2010b)].

$$I_s = I_{sf} + I_{sb} \tag{5.18}$$

Now I_{sf} and I_{sb} can be expressed as [Dubey *et al.* (2010b)]

$$I_{sf} = C \int_{-\frac{t_{s-Si}}{2}}^{y_{\min}} \exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) dy \tag{5.19}$$

$$I_{sb} = C \int_{y_{\min}}^{\frac{t_{s-Si}}{2}} \exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) dy \tag{5.20}$$

where $C = \frac{qD_n n_i^2}{N_p L_e}\left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right)$ (5.21)

After solving, Eq. (5.19) and Eq. (5.20), we obtained

$$I_{sf} = \frac{CV_T}{E_f}\left(\exp\left(\frac{\phi_{1,\min}(y_{\min})}{V_T}\right) - \exp\left(\frac{\phi_{1,\min}\left(-\frac{t_{s-Si}}{2}\right)}{V_T}\right)\right) \tag{5.22}$$

$$I_{sb} = \frac{CV_T}{E_b}\left(\exp\left(\frac{\phi_{1,\min}\left(\frac{t_{s-Si}}{2}\right)}{V_T}\right) - \exp\left(\frac{\phi_{1,\min}(y_{\min})}{V_T}\right)\right) \tag{5.23}$$

where,

$$E_f = \frac{\phi_{1,\min}(y_{\min}) - \phi_{1,\min}\left(-\frac{t_{s-Si}}{2}\right)}{y_{\min} + \frac{t_{s-Si}}{2}} \tag{5.24}$$

and $E_b = \frac{\phi_{1,\min}(y_{\min}) - \phi_{1,\min}\left(\frac{t_{s-Si}}{2}\right)}{y_{\min} - \frac{t_{s-Si}}{2}}$ (5.25)

E_f and E_b are the electric fields associated with the front and back surface of the device.

5.2.2 Modeling of Effective Conduction Path Parameter

Let us assume $d_{eff,A}$ and $d_{eff,B}$ represent the effective conduction path parameters of the front and back regions of the channel, then $d_{eff,A}$ can be expressed as [Dubey *et al.* (2011)]

$$d_{eff,A} = \frac{\int_{-\frac{t_{s-Si}}{2}}^{y_{\min}} y \exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) dy}{\int_{-\frac{t_{s-Si}}{2}}^{y_{\min}} \exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) dy} \tag{5.26}$$

After solving, we obtained

$$d_{eff,A} = \frac{n_1 + n_2}{n_3 - n_4} \tag{5.27}$$

where, $$n_1 = \left(y_{\min} - \frac{V_T}{E_f}\right) \exp\left(\frac{\phi_{1,\min}(y_{\min})}{V_T}\right) \tag{5.28}$$

$$n_2 = \left(\frac{t_{s-Si}}{2} + \frac{V_T}{E_f}\right) \exp\left(\frac{\phi_{1,\min}\left(-\frac{t_{s-Si}}{2}\right)}{V_T}\right) \tag{5.29}$$

$$n_3 = \exp\left(\frac{\phi_{1,\min}(y_{\min})}{V_T}\right) \tag{5.30}$$

$$n_4 = \exp\left(\frac{\phi_{1,\min}\left(-\frac{t_{s-Si}}{2}\right)}{V_T}\right) \tag{5.31}$$

Further $d_{eff,B}$ can be expressed as

$$d_{eff,B} = \frac{\int_{y_{\min}}^{\frac{t_{s-Si}}{2}} y \exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) dy}{\int_{y_{\min}}^{\frac{t_{s-Si}}{2}} \exp\left(\frac{\phi_{1,\min}(y)}{V_T}\right) dy} \quad (5.32)$$

Again solving, $d_{eff,B}$ can be written as

$$d_{eff,B} = \frac{n_6 - n_1}{n_5 - n_3} \quad (5.33)$$

where, $$n_6 = \left(\frac{t_{s-Si}}{2} - \frac{V_T}{E_f}\right) \exp\left(\frac{\phi_{1,\min}\left(\frac{t_{s-Si}}{2}\right)}{V_T}\right) \quad (5.34)$$

$$n_5 = \exp\left(\frac{\phi_{1,\min}\left(\frac{t_{s-Si}}{2}\right)}{V_T}\right) \quad (5.35)$$

The effective conduction path parameter for the whole device, can be written as [Dubey *et al.* (2011)]

$$d_{eff} = \frac{I_{sf}\left|d_{eff,A}\right| + I_{sb}\left|d_{eff,B}\right|}{I_s} \quad (5.36)$$

5.2.3 Modeling of Subthreshold Swing

The subthreshold swing (SS) can be written as [Dubey *et al.* (2011)]

$$S = \left(\frac{\partial \log I_s}{\partial V_{gs}}\right)^{-1} \quad (5.37)$$

Again for the ease of calculation, SS can be expressed in terms of minimum channel potential as [Dubey *et al.* (2011)]

$$S = V_T \left(\ln 10\right)\left(\frac{\partial \phi_{1,\min}\left(y\right)}{\partial V_{gs}}\right)^{-1} \tag{5.38}$$

Using the methodology of Ref. [Dubey *et al.* (2011)], y is replaced by d_{eff} to make swing independent of y.

5.3 Results and discussion

In the present section the modeling results are discussed and compared with the numerical simulation data to verify the validity of the proposed model. Fig. 5.2 shows the variation of SC with V_{gs} for different values of gate length L, maintaining all other parameters constant. Here it is clear that SC gets increased as channel length is decreased. It happens due to severe increase in SCEs. Again as the model is developed for subthreshold region, there occurs a mismatching between the modeling results and the simulation data above subthreshold region. Increasing slope of SC for increasing channel length demonstrates better switching characteristics.

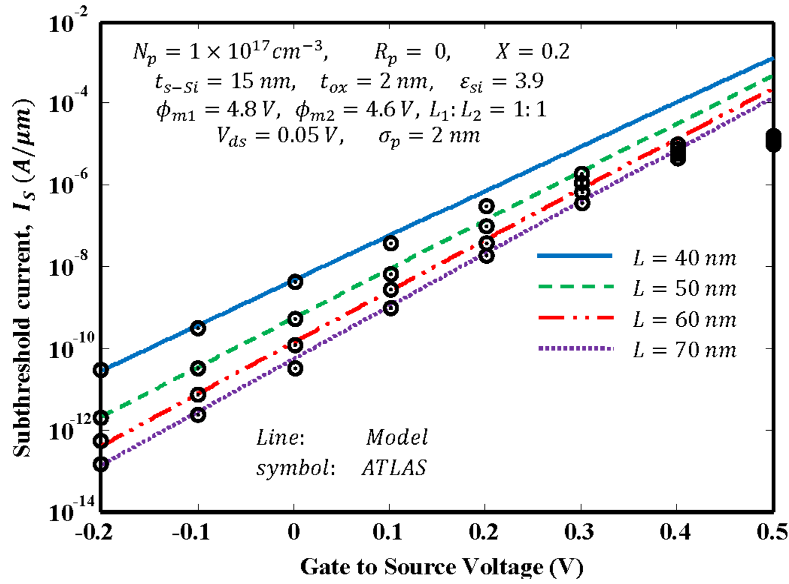

Fig. 5.2: Variation of SC with V_{gs} for different values of channel length

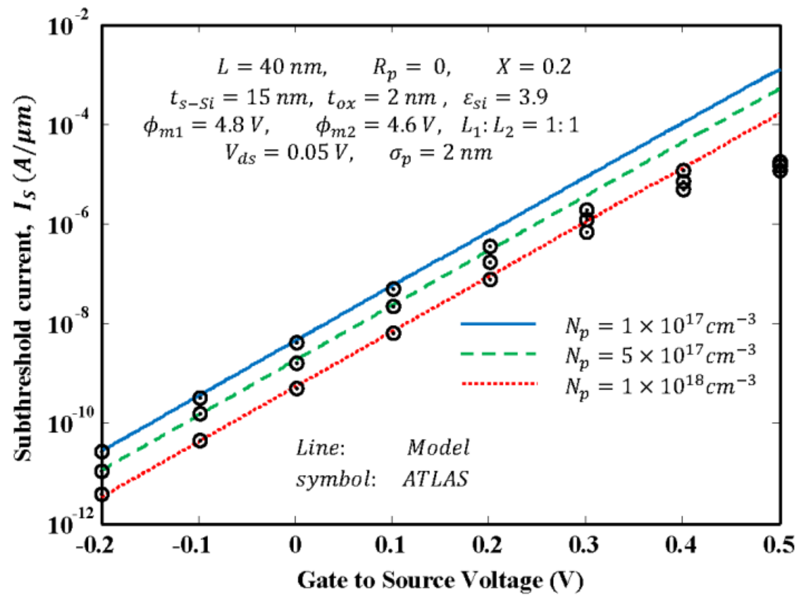

Fig. 5.3: Variation of SC with V_{gs} for different values of peak doping concentration

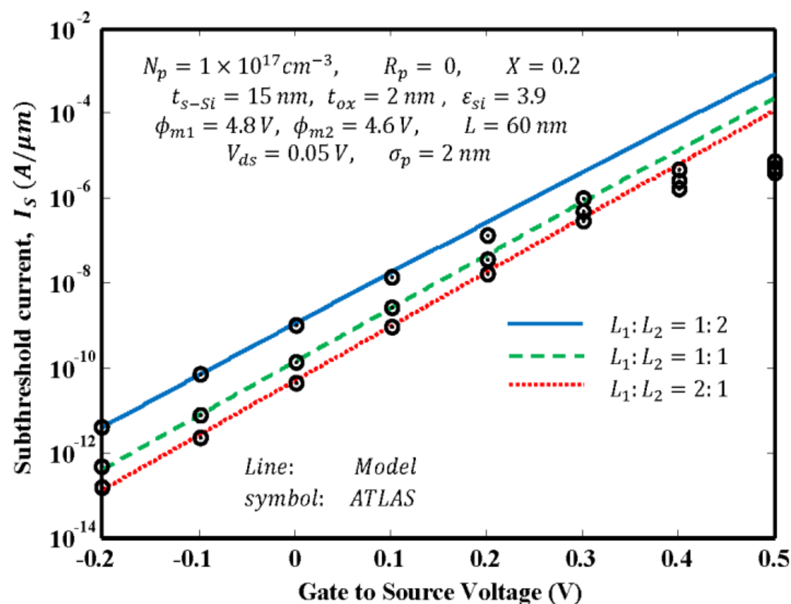

Fig. 5.4: Variation of SC with V_{gs} for different values of L_1:L_2

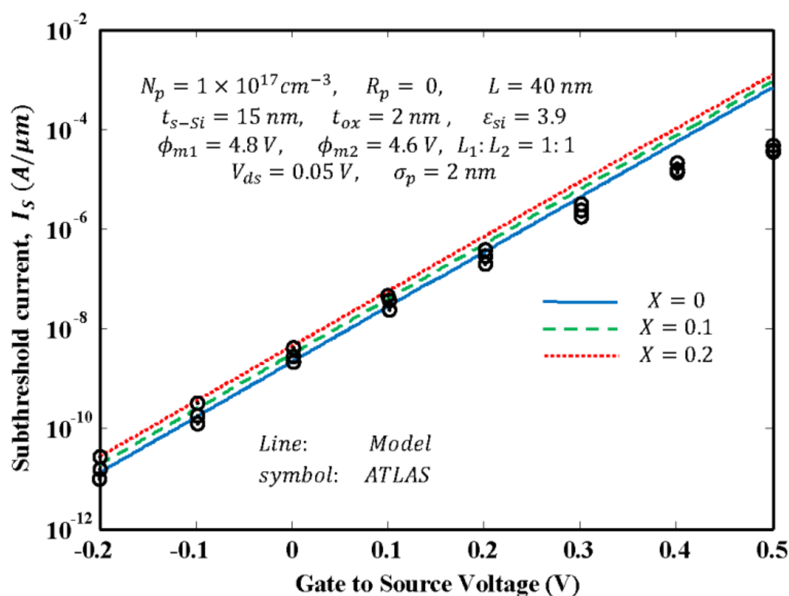

Fig. 5.5: Variation of SC with V_{gs} for different values of Ge mole fraction

Fig. 5.3 depicts SC variation with V_{gs} for different values of peak channel doping concentration. It can be concluded from the figure that as the channel doping is reduced, SC gets increased. The lower doping in the channel reduces the channel barrier and hence the flow of electrons from source to drain is increased which finally gives rise to the SC of the device. Fig. 5.4 demonstrates the effect of control-to-screen gate length ratio (L_1:L_2) on the graphs of SC vs V_{gs} while all other parameters are kept unchanged. An increasing value of L_1:L_2 reduces the SC due to a rise in the source to channel barrier height [Kumar *et al.* (2013c)]. Fig. 5.5 explains the impact of increasing value of strain (Ge mole fraction) on SC of the device. It shows that with increasing value of strain, the SC also gets increased due to reduced built-in potential [Kumar *et al.* (2013c)].

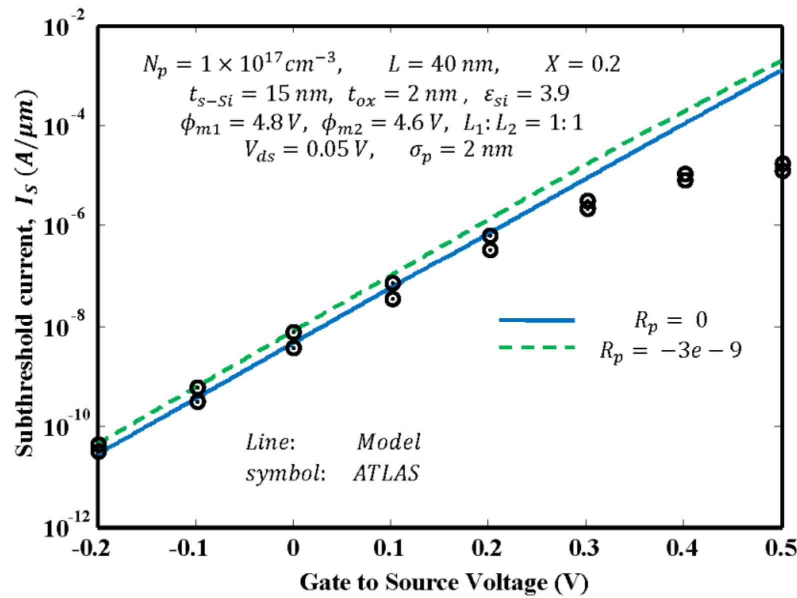

Fig. 5.6: Variation of SC with V_{gs} for different values of projected range

Fig. 5.6 shows the variation of SC as a function of V_{gs} for different values of projected range (R_p). Projected range indicates the position of peak channel doping concentration. It can be observed from the figure that keeping the position of peak doping concentration in the middle of the channel i.e. (R_p=0) gives minimum value of SC (maximum value of source to channel barrier height and threshold voltage described in Chapter-4), as the displacement in the position of peak doping concentration towards front (back) surface from the middle of the channel reduces the source channel barrier height at back (front) surface. This reduction in barrier height raises the SC. Thus, it can be observed that just by changing the projected range, the subthreshold characteristics of the device can be controlled without changing the geometry of the device.

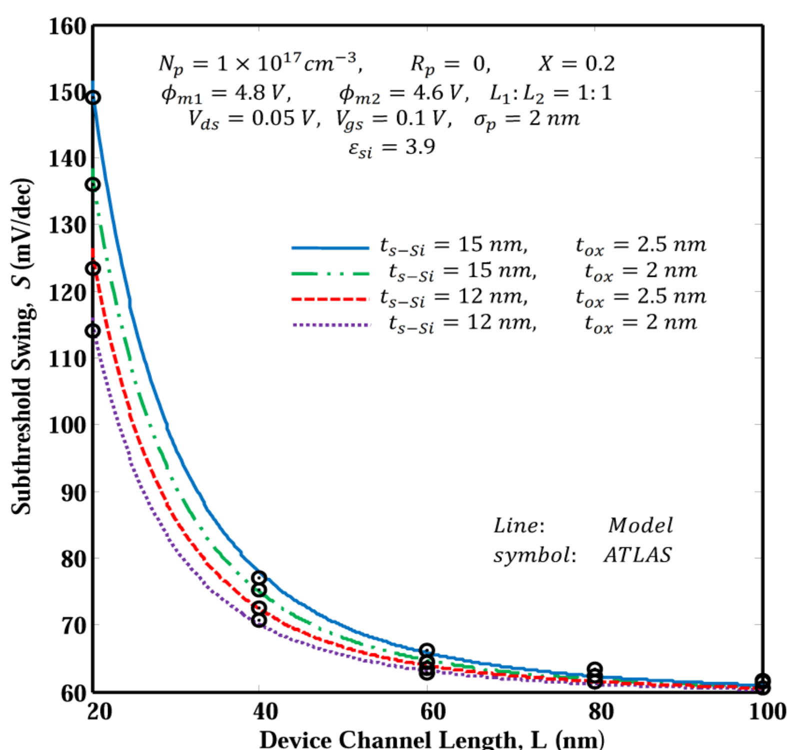

Fig. 5.7: Variation of SS along the device channel length for different values of s-Si channel thickness and gate oxide thickness

The variations of SS versus channel length for different values of s-Si film thickness ($t_{s\text{-}Si}$) and gate oxide thickness (t_{ox}) are explained in Fig. 5.7. Figure says as silicon film thickness is increased SS also increases very rapidly for shorter channel lengths especially for $L \leq 50\,\text{nm}$ and hence switching characteristics of the device are adversely affected. It may also be noted from the figure as gate oxide thickness is increased, the value of SS is also increased due to the reduction in the electric field lines through the oxide layer and hence control of the gate over the channel also gets reduced.

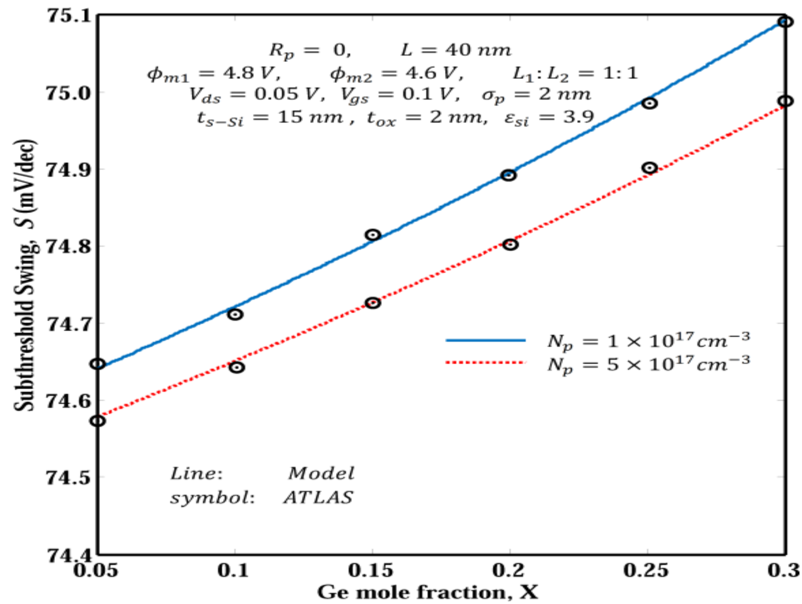

Fig. 5.8: Variation of SS with Ge mole fraction for different values of peak doping concentration

Fig. 5.8 shows variation of SS with Ge mole fraction for different values of peak channel doping concentration. It is clear from the figure that the SS is decreased with increased peak channel doping possibly due to the slight increase in the subthreshold

slope of current versus V_{gs} graphs as shown in Fig. 5.3. Hence it can be concluded from the figure that switching characteristics of the device can be improved by increasing the doping concentration. Again increasing value of Ge mole fraction also deteriorates the switching performance of the device by increasing the SS.

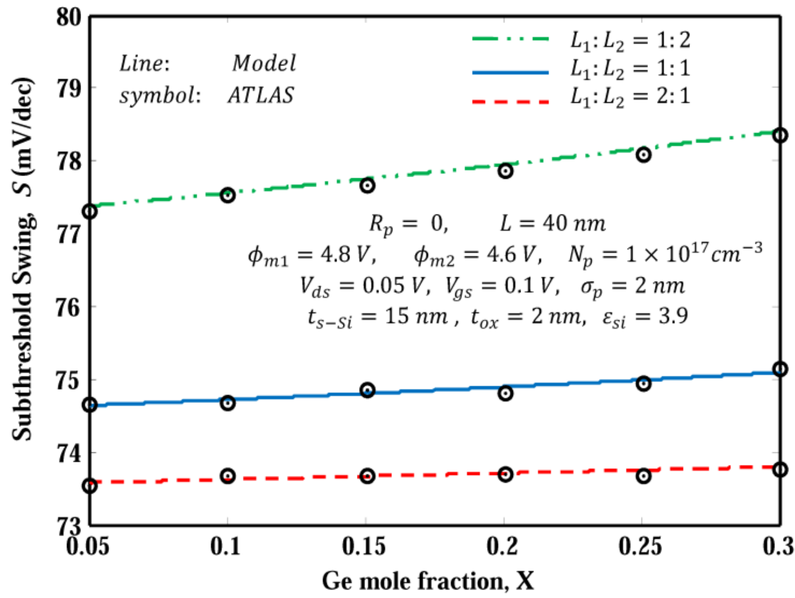

Fig. 5.9: Variation of SS with Ge mole fraction for different values of L_1:L_2

Fig. 5.9 shows variation of SS with Ge mole fraction for different values of control-to-screen gate length ratio (L_1:L_2). It is found that SS gets reduced with increasing value of L_1:L_2.

5.4 Conclusion

In the present chapter, two dimensional analytical models for SC and SS are developed for ion-implanted s-Si gate DMDG MOSFETs. The subthreshold behavior of the device

is examined thoroughly by investigating the effect of different device parameters i.e. channel length, s-Si channel thickness, gate oxide thickness, control-to-screen gate length ratio, etc. on the device performance. Furthermore, the use of Gaussian-like doping profile introduces the advantage of precise control over the subthreshold characteristics of the device without any change in the geometry of the device. The device offers the combined benefits of s-Si channel, double-material gate (DMG) and Gaussian-like doping profile. The model results are found well agreed with the simulation data obtained by ATLAS™, a 2-D device simulator from SILVACO.