Chapter 4

Analytical Modeling of Potential Distribution and Threshold Voltage of Ion-Implanted Strained-Si Dual-Material Double-Gate MOSFETs

4.1 Introduction

We have discussed in Chapter-1 that the channel characteristics of a MOS device can be modified by channel doping profile engineering and strain engineering. In last two chapters, we have studied the subthreshold characteristics of the newly proposed GCDMDG MOS structure where the graded channel (GC) engineering [Chen *et al.* (2002), Kaur *et al.* (2008), Kaur *et al.* (2007a), Kaur *et al.* (2007b), Kranti *et al.* (2004)] and dual-material-gate (DMG) [Chiang and Chen (2007), Long *et al.* (1999), Kumar and Chaudhry (2004), Reddy and Kumar (2005), Chaudhry and Kumar (2004), Chiang and Chiang (2007)] have been explored simultaneously for improving the immunity to short-channel-effects (SCEs) and hot-carrier-effects (HCEs) of the device. The literature review presented in Chapter-1 shows that strained-Si (s-Si) channel engineering can enhance the drive current and speed of the device due to enhanced channel carrier mobility [Welser *et al.* (1994), Ieong *et al.* (2004), Kuchipudi and Mahmoodi (2007), Venkataraman *et al.* (2007), Kumar *et al.* (2007), Jin *et al.* (2011)] at the cost of increased drain-induced barrier lowering (DIBL) and HCEs [Kumar *et al.* (2013b)]. We have also discussed that the double-material-gate (DMG) based MOS structures have the capability to suppress the SCEs and HCEs [Long *et al.* (1999),

Tiwari *et al.* (2010), Mahato *et al.* (2008), Sharan and Rana (2011)]. The literature review in Chapter-1 also shows that the vertical-Gaussian doping channel profile engineering in the DG MOSFETs can provide better flexibilities for controlling the SCEs than the conventional uniformly doped DG MOSFETs due to two additional parameters namely the straggle and projected range (in addition to the peak doing concentration) of the doping profile [Tiwari and Jit (2010b), Rawat *et al.* (2014)]. Clearly, the Gaussian doped channel profile engineering [Zhang *et al.* (2008), Tiwari and Jit (2010b), Tiwari and Jit (2010c), Rawat *et al.* (2014)] and the s-Si channel engineering [Welser *et al.* (1994), Ieong *et al.* (2004), Kuchipudi and Mahmoodi (2007), Venkataraman *et al.* (2007), Kumar *et al.* (2007), Jin *et al.* (2011)] can be explored simultaneously in the DMDG MOSFETs to achieve the combined benefits of the Gaussian doped channel engineering, s-Si channel engineering and DMG engineering in the single MOS device. Thus the objective of the present chapter is to develop the analytical models for the surface potential and threshold voltage of the s-Si DMDG MOSFETs with a vertical Gaussian channel doping profile commonly obtained by the ion-implantation technique [Sze (1981), Zhang *et al.* (2008)]. For the simplicity of the model, the actual non-integrable vertical Gaussian function over any finite interval has been replaced by an analytic double-integrable vertical Gaussian-like function [Dasgupta and Lahiri (1986)] as discussed in Chapter-1. The layout of the present chapter has been outlined as follows:

In Section 4.2, we have first repeated some discussions of Chapter-1 related to the effect of strain on the bandgap and flat-band voltage for the better understanding of the models developed in this chapter. Then the surface potential has been modeled by solving the 2D Poisson's equation in the channel region using the parabolic approximation method already

discussed in Chapter-2. The surface potential has been used to model the threshold voltage of the proposed Gaussian doped s-Si DMDG MOSFETs. The theoretical results along with their comparison with the respective ATLAS based TCAD simulation data have been presented and discussed in Sec. 4.3. Finally, Sec. 4.4 describes the conclusion of the present chapter.

4.2 Model Derivation

The schematic structure of the s-Si DMDG MOSFET under study is shown in Fig. 4.1 where the notations L, t_{s-Si} and t_{ox} represent the channel length, s-Si channel thickness and the thickness of the SiO_2 gate-oxide at both the front and back gates of the device, respectively. The strain in the channel of the proposed structure is assumed to be introduced by the layer transfer technique reported by Rim *et al.* [Rim *et al.* (2001)] as already discussed in Chapter-1. The x-axis and y-axis of the 2D structure are taken along the center of the channel and the source-channel interface, respectively, as shown in the figure. The lengths L_1 and L_2 represent the lengths of the control gate and screen gate electrode metals with work functions ϕ_{m1} and ϕ_{m2} respectively so that the total channel length $L = L_1 + L_2$ and $\phi_{m1} > \phi_{m2}$. The channel doping profile is assumed to be a Gaussian-like function [Dasgupta and Lahiri (1988), Dubey *et al.* (2010a)] in the vertical direction *y* of the channel which can be described as

$$N_b(y) \cong N_p\, c\left(\left(a + 2b\alpha Y\right)^2 - 2b\right)\exp\left(-a\alpha Y - bY^2\right) \tag{4.1}$$

where N_p is the peak doping concentration at $y = R_p$, (R_p is the projected range); $Y = \dfrac{y - R_p}{y_b}$, $y_b = \sqrt{2}\,\sigma_p$ (σ_p is the straggle parameter of the Gaussian Function); a, b and c are the fitting parameters with values $a = 1.786$, $b = 0.646$ and $c = 0.56$; $\alpha = +1$ for $y \geq 0$ and -1 for $y \leq 0$ [Dubey *et al.* (2010a)].

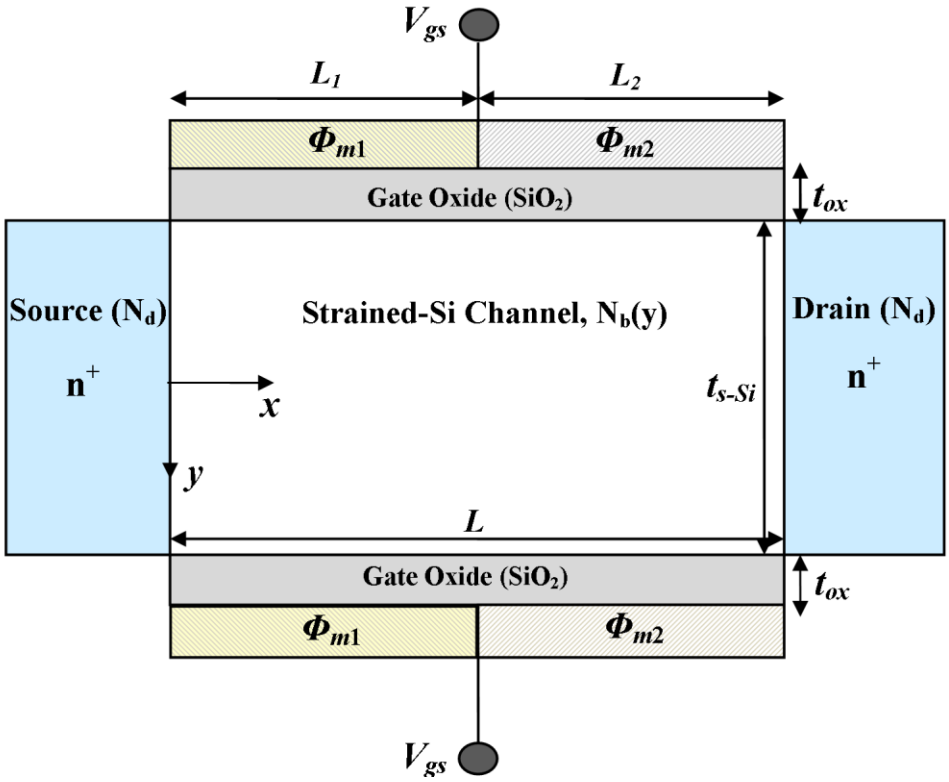

Fig. 4.1: Schematic structure of Strained Silicon Double-Material Double-Gate (DMDG) MOSFET

4.2.1 Effect of Strain on the Bandgap and Flat-band Voltage

The effect of strain on the energy band structure of s-Si channel can be modelled as a function of the germanium mole fraction X as follows (already discussed in Chapter-1) [Venkataraman *et al.* (2007)]:

$$\Delta E_c = 0.57X \tag{4.2}$$

$$\Delta E_g = 0.4X \tag{4.3}$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{3/2} = 0.075X \tag{4.4}$$

where ΔE_c is the change in conduction band energy, ΔE_g is the decrease in the bandgap energy, V_T is the thermal voltage; $N_{V,Si}$ is the effective density of states in the valence band of unstrained p-Si corresponding to the effective mass of hole $m^*_{h,Si}$ and $N_{V,s-Si}$ is the changed density of states in the valence band corresponding to the changed effective mass of hole $m^*_{h,s-Si}$ in the strained p-Si channel.

Here, $k = 1$ and $k = 2$ are used to denote the region 1 and 2, and "*b*" and "*f*" denote the back channel and front channel, respectively, in the subscripts of the conventional parameters, the effect of strain on the front-channel and back-channel flat-band voltages can be modeled as [Venkataraman *et al.* (2007)]:

$$\left(V_{fbfk}\right)_{s-Si} = \left(V_{fbfk}\right)_{Si} + \Delta V_{fb} \tag{4.5}$$

where

$$\left(V_{fbfk}\right)_{Si} = \phi_{mk} - \phi_{Si,f} \tag{4.6}$$

$$\Delta V_{fb} = -\frac{\Delta E_c}{q} + \frac{\Delta E_g}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \tag{4.7}$$

$$\phi_{Si,f} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \phi_{ff,Si} \tag{4.8}$$

$$\phi_{ff,Si} = V_T \ln\left(\frac{\mathrm{N_b}(y)}{n_i}\right)\Bigg|_{y=-\frac{t_{s-Si}}{2}} = V_T \ln\left(\frac{N_{bf}}{n_i}\right) \tag{4.9}$$

$$N_{bf} = N_b(y)\Big|_{y=-\frac{t_{s-Si}}{2}} \tag{4.10}$$

and

$$\left(V_{fbbk}\right)_{s-Si} = \left(V_{fbbk}\right)_{Si} + \Delta V_{fb} \tag{4.11}$$

where

$$\left(V_{fbbk}\right)_{Si} = \phi_{mk} - \phi_{Si,b} \tag{4.12}$$

$$\phi_{Si,b} = \frac{\chi_{Si}}{q} + \frac{E_g}{2q} + \phi_{fb,Si} \tag{4.13}$$

$$\phi_{fb,Si} = V_T \ln\left(\frac{\mathrm{N_b}(y)}{n_i}\right)\Bigg|_{y=\frac{t_{s-Si}}{2}} = V_T \ln\left(\frac{N_{bb}}{n_i}\right) \tag{4.14}$$

$$N_{bb} = N_b(y)\Big|_{y=\frac{t_{s-Si}}{2}} \tag{4.15}$$

where, $\left(V_{fbfk}\right)_{s-Si}$ [$\left(V_{fbbk}\right)_{s-Si}$] and $\left(V_{fbfk}\right)_{Si}$ [$\left(V_{fbbk}\right)_{Si}$] are the front [back] flat-band voltages of the strained and normal silicon corresponding to the region "*k*" respectively; $\phi_{Si,f}$ [$\phi_{Si,b}$], $\phi_{ff,Si}$ [$\phi_{fb,Si}$] and N_{bf} [N_{bb}] are the work function, Fermi potential and doping concentration of the front [back]; and χ_{si}, E_g, and n_i are the electron affinity, band-gap energy and intrinsic carrier concentration of the unstrained p-Si channel, respectively.

Finally, the effect of strain on the built-in voltage at the source (drain)/p-Si channel can be expressed as [Venkataraman *et al.* (2007)]:

$$V_{bi,s-Si} = V_{bi,Si} + \Delta V_{bi} \tag{4.16}$$

$$V_{bi,Si} = V_T \ln\left(\frac{N_b(y)N_d}{n_i^2}\right) \tag{4.17}$$

$$\Delta V_{bi} = -\frac{\Delta E_g}{q} + V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \tag{4.18}$$

where $V_{bi,s-Si}$ and $V_{bi,Si}$ are the built-in voltages of the source (drain)/channel junction for the strained and unstrained silicon respectively.

4.2.2 Modeling of Surface Potential

Let the 2D potential distribution function corresponding to the region "*k*" be denoted by $\phi_k(x,y)$. Now the 2D Poisson's equation can be written as

$$\frac{\partial^2\phi_k(x,y)}{\partial x^2} + \frac{\partial^2\phi_k(x,y)}{\partial y^2} = \frac{qN_b(y)}{\varepsilon_{Si}} \qquad \text{for } \frac{-t_{s-Si}}{2} \le y \le \frac{t_{s-Si}}{2} \tag{4.19}$$

where, subscript $k = 1$is for region 1 (i.e. below the control gate region) and $k = 2$ is for region 2 (i.e. below the screen gate region) of the channel.

From the continuity of the electric flux at the front and back channel and gate-oxide interfaces, we obtain the following boundary conditions [Kumar *et al.* (2013b), Dubey *et al.* (2010a)]:

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_{gs}-V_{fbfk}-\phi_k\left(x,-\frac{t_{s-Si}}{2}\right)\right]=-\varepsilon_{Si}\left.\frac{\partial\phi_k(x,y)}{\partial y}\right|_{y=-\frac{t_{s-Si}}{2}} \tag{4.20}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_{gs}-V_{fbbk}-\phi_k\left(x,\frac{t_{s-Si}}{2}\right)\right]=\varepsilon_{Si}\left.\frac{\partial\phi_k(x,y)}{\partial y}\right|_{y=\frac{t_{s-Si}}{2}} \tag{4.21}$$

where, ε_{Si} and ε_{ox} are the permittivities of silicon and gate-oxide layers respectively; and V_{gs} is the gate-to-source voltage.

Using the parabolic approximation method [Young (1989)], the potential distribution in the k^{th} region of the silicon channel film can be written as [Tiwari *et al.* (2010)]:

$$\phi_k(x,y)=C_{ko}(x)+C_{k1}(x)y+C_{k2}(x)y^2 \tag{4.22}$$

Putting $y=0$ in Eq. (4.22), we get

$$C_{ko}(x)=\phi_k(x,y)\big|_{y=0}=\phi_{ok}(x) \tag{4.23}$$

where $\phi_{ok}(x)$ is the central channel potential along the channel.

Using the boundary conditions described by Eqs. (4.20) and (4.21) in Eq. (4.22), we obtain

$$C_{k1}=\left(\frac{V_{fbfk}-V_{fbbk}}{2}\right)\left(\frac{2C_{ox}}{t_{s-Si}C_{ox}+2\varepsilon_{Si}}\right) \tag{4.24}$$

$$C_{k2}=\left(V_{gs}-\frac{\left(V_{fbfk}+V_{fbbk}\right)}{2}-\phi_{ok}(x)\right)\left(\frac{4C_{ox}}{t_{s-Si}^2C_{ox}+4\varepsilon_{Si}t_{s-Si}}\right) \tag{4.25}$$

where, $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$ is the gate-oxide capacitance per unit area.

Using Eq. (4.22) and (4.23) in Eq. (4.19) for $y=0$, the central channel potential $\phi_{ok}(x)$ can be expressed as:

$$\frac{\partial^2 \phi_{ok}(x)}{\partial x^2} - \frac{1}{\lambda^2}\phi_{ok}(x) = -\frac{1}{\lambda^2}\Gamma_k \tag{4.26}$$

where

$$\frac{1}{\lambda^2} = \frac{8C_{ox}}{4\varepsilon_{Si}t_{s-Si} + t_{s-Si}^2 C_{ox}} \tag{4.27}$$

$$\Gamma_k = V_{gs} - w_k \tag{4.28}$$

$$w_k = \frac{\left(V_{fbfk} + V_{fbbk}\right)}{2} + \frac{qN_{b0}t_{s-Si}}{2C_{ox}} + \frac{qN_{b0}t_{s-Si}^2}{8\varepsilon_{Si}} \tag{4.29}$$

$$N_{b0} = N_b(y)\big|_{y=0} \tag{4.30}$$

The general solution for the Eq. (4.26) can be expressed as [Tiwari *et al.* (2010)]:

$$\phi_{ok}(x) = A_k \exp\left(\frac{x}{\lambda}\right) + B_k \exp\left(-\frac{x}{\lambda}\right) + \Gamma_k \tag{4.31}$$

where, A_k and B_k are the constants to be determined with the help of the following boundary conditions [Kumar *et al.* (2013b), Tiwari *et al.* (2010), Dubey *et al.* (2010a)]:

$$\phi_{o1}(L_1) = \phi_{o2}(L_1) \tag{4.32}$$

$$\left.\frac{\partial \phi_{o1}(x,y)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial \phi_{o2}(x,y)}{\partial x}\right|_{x=L_1} \tag{4.33}$$

$$\text{At } x = 0: \quad \phi_{o1} = \phi_{o1}(0) = V_{bi,s-Si}(y)\big|_{y=0} = V_{bi,s-Si0} \tag{4.34}$$

$$V_{bi,s-Si0} = V_{bi,s-Si}(y)\big|_{y=0} = V_{bi,Si}(y)\big|_{y=0} + \Delta V_{bi} \tag{4.35}$$

$$V_{bi,Si}(y)\big|_{y=0} = V_{bi,Si0} = V_T \ln\left(\frac{N_{b0}N_d}{n_i^2}\right) \tag{4.36}$$

$$\text{at } x = L_1 + L_2: \qquad \phi_{o2} = \phi_{o2}(0) = V_{bi,s-Si0} + V_{ds} \tag{4.37}$$

Using Eqs. (4.32)-(4.37) in Eq. (4.31), we write

$$A_2 = \alpha_2 V_{gs} + \beta_2 \tag{4.38}$$

where

$$\alpha_2 = \frac{\exp\left(-\frac{(2L_1 + L_2)}{\lambda}\right) - \exp\left(-\frac{L_1}{\lambda}\right)}{\exp\left(\frac{L_2}{\lambda}\right) - \exp\left(-\frac{(2L_1 + L_2)}{\lambda}\right)} \tag{4.39}$$

$$\beta_2 = \frac{D_1 + D_2}{D_3} \tag{4.40}$$

where

$$D_1 = V_{ds} \exp\left(-\frac{L_1}{\lambda}\right) - V_{bi,s-Si0}\left(\exp\left(-\frac{(2L_1 + L_2)}{\lambda}\right) - \exp\left(-\frac{L_1}{\lambda}\right)\right) - w_1 \exp\left(-\frac{(2L_1 + L_2)}{\lambda}\right) + w_2 \exp\left(-\frac{L_1}{\lambda}\right) \tag{4.41}$$

$$D_2 = (w_1 - w_2)\exp\left(-\frac{(L_1 + L_2)}{\lambda}\right) - \left(\frac{w_1 - w_2}{2}\right)\left(\exp\left(-\frac{(L_1 + L_2)}{\lambda}\right) - \exp\left(-\frac{(3L_1 + L_2)}{\lambda}\right)\right) \tag{4.42}$$

$$D_3 = \exp\left(\frac{L_2}{\lambda}\right) - \exp\left(-\frac{(2L_1 + L_2)}{\lambda}\right) \tag{4.43}$$

$$B_2 = \gamma_2 V_{gs} + K_2 \tag{4.44}$$

where

$$\gamma_2 = -\alpha_2 \exp\left(\frac{2(L_1 + L_2)}{\lambda}\right) - \exp\left(\frac{L_1 + L_2}{\lambda}\right) \tag{4.45}$$

$$K_2 = (V_{bi,s-Si0} + V_{ds} + w_2)\exp\left(\frac{L_1 + L_2}{\lambda}\right) - \beta_2 \exp\left(\frac{2(L_1 + L_2)}{\lambda}\right) \tag{4.46}$$

$$A_1 = \alpha_1 V_{gs} + \beta_1 \tag{4.47}$$

where

$$\alpha_1 = \alpha_2 \tag{4.48}$$

$$\beta_1 = \beta_2 + \frac{w_1 - w_2}{2}\exp\left(-\frac{L_1}{\lambda}\right) \tag{4.49}$$

$$B_1 = \gamma_1 V_{gs} + K_1 \tag{4.50}$$

where

$$\gamma_1 = -\alpha_2 - 1 \tag{4.51}$$

$$K_1 = V_{bi,s-Si0} + w_1 - \beta_2 - \frac{(w_1 - w_2)}{2}\exp\left(-\frac{L_1}{\lambda}\right) \tag{4.52}$$

Now, the respective back and front surface potentials can be obtained as:

$$\phi_{sbk}(x) = \phi_k(x,y)\Big|_{y=\frac{t_{s-Si}}{2}} \tag{4.53}$$

and

$$\phi_{sfk}(x) = \phi_k(x,y)\Big|_{y=-\frac{t_{s-Si}}{2}} \tag{4.54}$$

4.2.3 Modeling of Threshold Voltage

In conventional MOSFETs, threshold voltage (V_{th}) is taken as the value of the gate voltage V_{gs} at which the minimum surface potential is equal to the twice of the bulk Fermi potential [Dubey *et al.* (2010a)]. Note that, in the proposed structure, the minimum of the surface potential will occur in the control gate region due to higher work function of the gate

electrode metal. Thus, the position $x_{1,\min}$ of the minimum surface potential, called the virtual cathode [Tiwari *et al.* (2010)], can be estimated by solving either

$$\left(\frac{\partial \phi_{sf1}(x)}{\partial x}\right)\Bigg|_{x=x_{1,\min}} = 0 \tag{4.55}$$

or

$$\left(\frac{\partial \phi_{sb1}(x)}{\partial x}\right)\Bigg|_{x=x_{1,\min}} = 0 \tag{4.56}$$

where $\phi_{sf1}(x)$ and $\phi_{sb1}(x)$ are the front and back surface potentials which will be minimum at that position of x where the central channel potential $\phi_{ok}(x)$ is minimum [Dubey *et al.* (2010a)].

Thus, the position of the virtual cathode $x_{1,\min}$ is obtained by solving

$$\left(\frac{\partial \phi_{o1}(x)}{\partial x}\right)\Bigg|_{x=x_{1,\min}} = 0 \tag{4.57}$$

which gives

$$x_{1,\min} = \left(\frac{\lambda}{2}\right)\ln\left(\frac{B_1}{A_1}\right) \tag{4.58}$$

The minimum value of the front surface potential is defined as

$$\phi_{sf,\min} = \phi_{sf1}(x)\Big|_{x=x_{1,\min}} \tag{4.59}$$

Similarly, the minimum value of the back surface potential is defined as

$$\phi_{sb,\min} = \phi_{sb1}(x)\Big|_{x=x_{1,\min}} \tag{4.60}$$

Since the proposed structure consists of the two channels, the device possesses two threshold voltages corresponding to the turning on of the front and back channels. The threshold voltage of the front surface V_{thf} can be defined by incorporating the effect of strain of the channel as

$$\phi_{sf,\min} = 2\phi_{ff,Si} + \Delta V_{bi} \tag{4.61}$$

Similarly, the threshold voltage of back channel V_{thb} can be defined as

$$\phi_{sb,\min} = 2\phi_{fb,Si} + \Delta V_{bi} \tag{4.62}$$

It may be mentioned that the device is said to be ON if any of the two channels is turned on. Thus, the effective threshold voltage of the device is given by the minimum of the V_{thf} and V_{thb} which is given by

$$V_{th} = Min\ \left(V_{thf}, V_{thb}\right) \tag{4.63}$$

4.3 Results and Discussion

In this section, we will compare the model results with the TCAD simulation data obtained by simulating the proposed structure using ATLAS^{TM}, a 2D device simulator. The drift-diffusion model for carrier transport, CVT (Lombardi Model) mobility model and SRH recombination model have been used in the ATLAS for simulating the structure.

First of all, we have plotted the surface potential as a function of the channel position in Fig. 4.2 for different values of the control gate to screen gate length ratio $L_1 : L_2$ but of the fixed gate length $L = L_1 + L_2$. The peak doping position of the Gaussian profile is assumed to be located at the middle of the channel in the vertical direction (i.e. $y = R_p = 0$) so that the front and back surface potentials become the same due to the symmetric nature of the device. It is observed from the figure that the DMG structure introduces a step in the potential profile which is responsible for screening the device from the variations in drain-to-source voltage and thereby reducing the DIBL. Further, the increase in the control-to-screen gate length ratio decreases the minimum surface potential (i.e. increases the maximum source to channel barrier height) and shifts the position of the minimum surface potential away from the source side towards the drain side.

Figure 4.3 shows the effect of strain (in terms of Ge mole fraction X) on the surface potential profile. The increased strain with the increased value of X leads to the decrease in the source to channel potential barrier. Thus, it is expected that more number of carriers may enter from the source into the channel in the subthreshold region due to the reduction in the source/channel barrier which, in turn, may increase the subthreshold current of the device with the increased strain in the channel. In other words, the enhanced mobility of carriers in the s-Si channel can be achieved at the cost of poor immunity to SCEs.

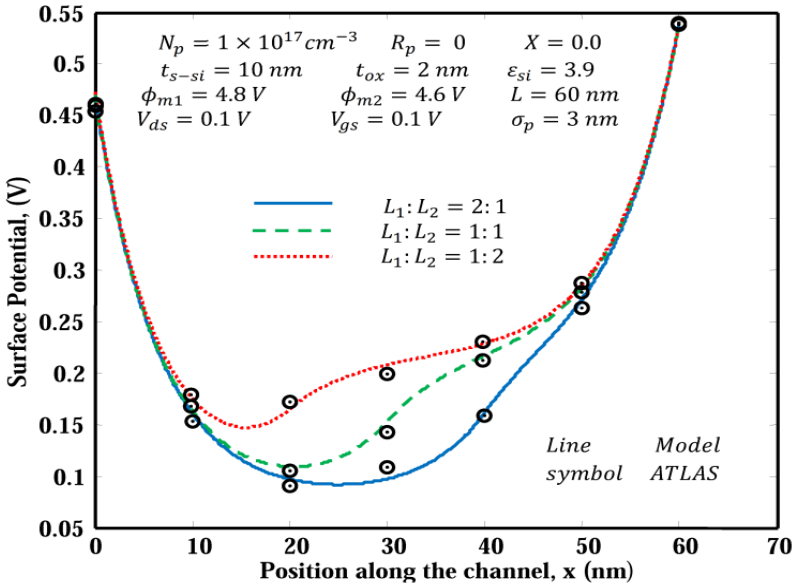

Fig. 4.2: Variation of surface potential along the position of the channel for different values of $L_1 : L_2$

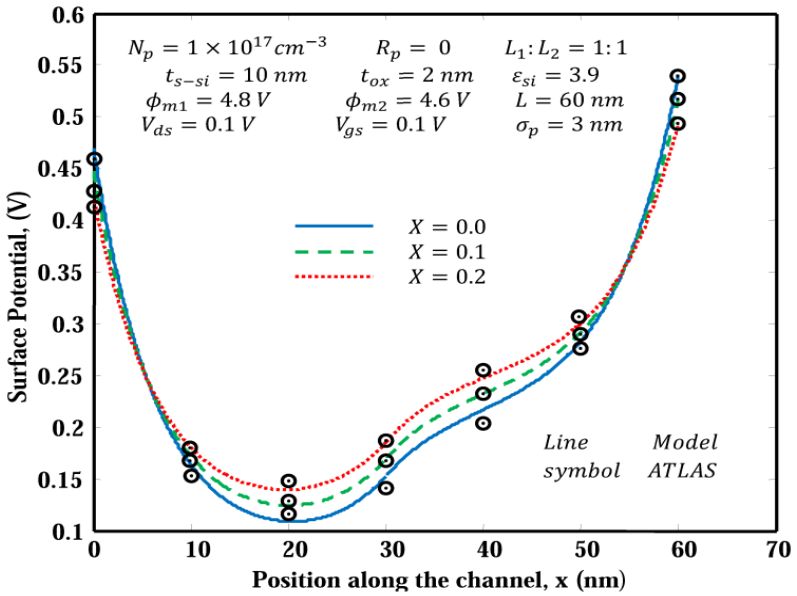

Fig. 4.3: Variation of surface potential along the position of the channel for different values of Ge mole fraction

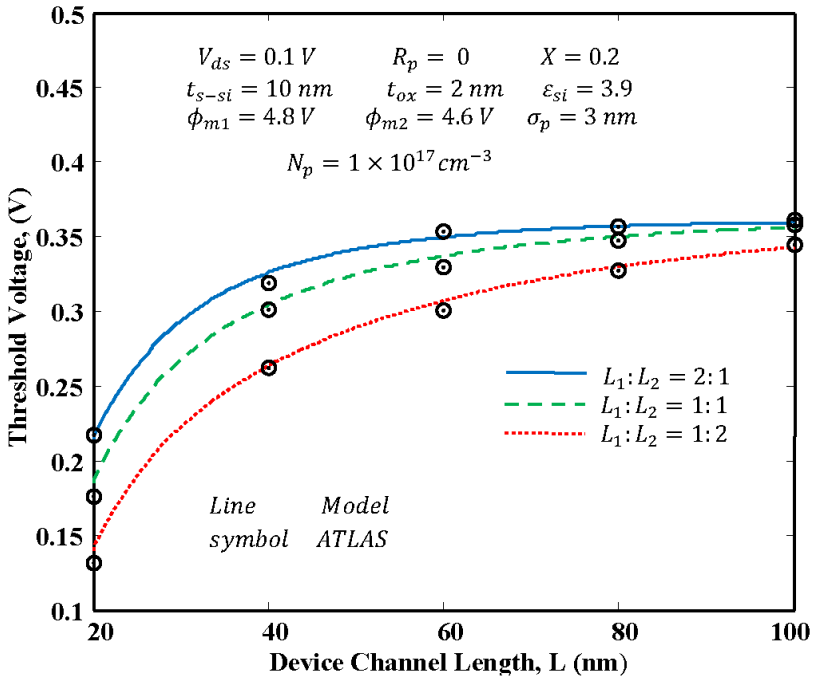

Fig. 4.4: Variation of threshold voltage with channel length for different values of $L_1 : L_2$

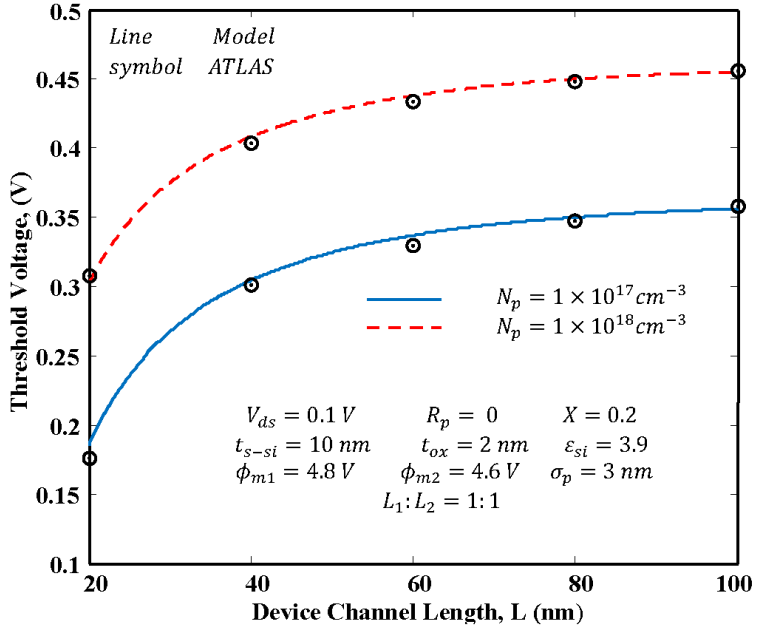

Fig. 4.5: Variation of threshold voltage with channel length for different values of peak doping concentration

Figure 4.4 shows the variation of the threshold voltage with the channel length for different values of control-to-screen gate length ratios. Note that for a fixed channel length, the increase of the control-to-screen gate length ratio (but constant gate length $L = L_1 + L_2$) increases the threshold voltage of the device due to the increase in the source/channel barrier height already discussed in Fig. 4.2. However, the threshold voltage is found to be decreased with the decrease in the channel length due to enhanced SCEs. It is also observed from Fig. 4.4 that the threshold voltage roll-off is decreased with the increase in control-to-screen gate length ratio. Figure 4.5 shows the variation of the threshold voltage with the channel length for different values of peak Gaussian doping concentrations. It is observed from the figure that the threshold voltage is increased with peak doping concentration N_p as observed in the uniformly doped channels due to increased barrier height of the channel [Kumar *et al.* (2013a)]. However, the threshold voltage is found to be decreased with the decrease in the channel lengths due to enhanced SCEs. It is also observed from Fig. 4.5 that the threshold voltage roll-off is decreased with the increase in the peak doping concentration. Effect of strain and projected range, on the threshold voltage of the device, are depicted in Fig. 4.6. The increased strain reduces the threshold voltage due to the decrease in the source/channel barrier height (i.e. increase in the minimum surface potential) as demonstrated earlier in Fig. 4.3. Note that the projected range (R_p) indicates the position of peak doping concentration of the Gaussian doping profile in the channel with $R_p = 0$ representing the peak doping concentration at the middle of the channel i.e. $y = 0$. It is also important to note that despite the symmetric physical structure of the device, the location of the peak doping at any other position except at middle of the channel

in the vertical direction (i.e. $R_p \neq 0$) makes the device asymmetric in nature due to asymmetric doping concentration with respect to $y = 0$ axis [Dubey *et al.* (2010a)]. As the position of peak doping concentration moves towards front (back) surface from $y = 0$ axis while keeping other parameters unchanged, the lowest doping concentration is obtained at the back (front) surface (i.e. the opposite to the front (back) surface). Since the threshold voltage is increased with the doping concentration, the lower threshold voltage of the back (front) surface than the front (back) surface will determine the effective threshold voltage of the device as per Eq. (4.63). Further, the threshold voltage of the device (i.e. of the back (front) surface) is decreased with the increase in the shifting of the peak doping position from the middle of the channel (i.e. $y = 0$) towards the front (back) surface. In other words, the threshold voltage is decreased with increased value of R_p (with respect to $R_p = 0$) as shown in Fig. 4.6.

Effect of straggle parameters on the threshold voltage of the device is explored in Fig. 4.7. It is observed that the threshold voltage increases with the straggle parameter σ_p due to the increase in the doping concentration at any arbitrary position of the channel except at $x = 0 = R_p$ as observed from Fig. 4.7.

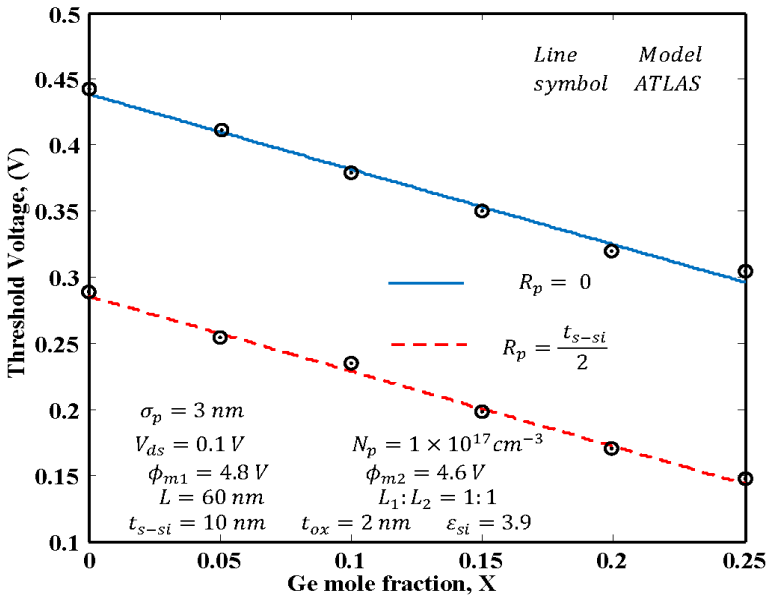

Fig. 4.6: Variation of threshold voltage with Ge mole fraction for different values of projected range

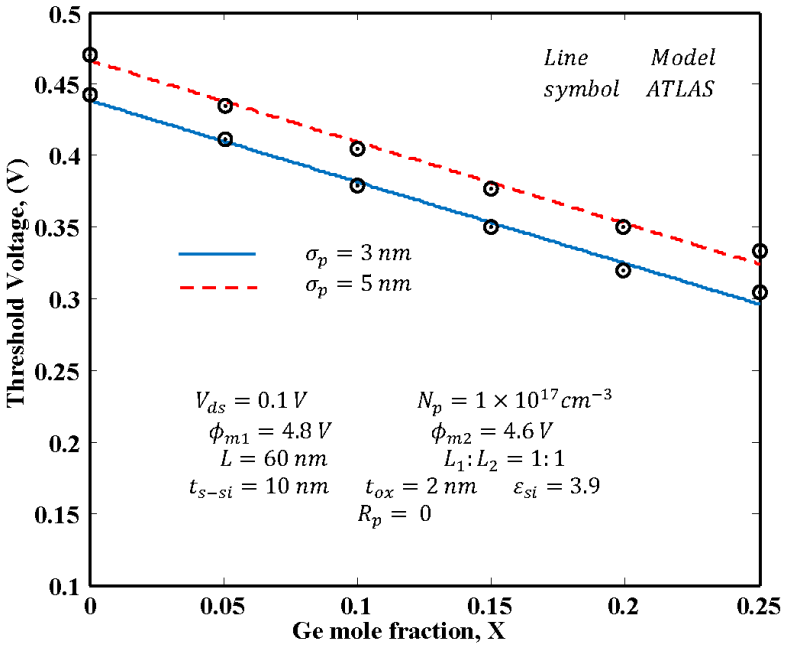

Fig. 4.7: Variation of threshold voltage with Ge mole fraction for different values of straggle parameter

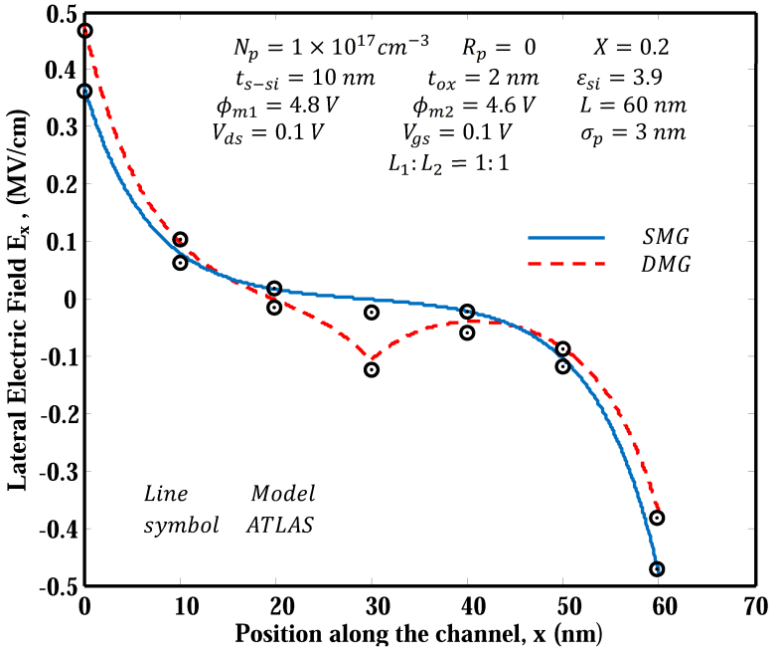

Fig. 4.8: Variation of lateral electric field along the position of the channel for SMG and DMG structures

Finally, the effectiveness of DMG structure to reduce the HCEs is demonstrated in Fig. 4.8. In this figure, the lateral electric field $E_{xk} = -\dfrac{d\phi_{sfk}(x)}{dx}$ (where '*k*' denotes the region in DMG structure, as explained earlier), at the front surface of the channel of the single-material gate (SMG) and double-material gate (DMG) structures have been compared. Note that the positive, zero and negative electric fields in $0 \le x < x_{1,\min}$ (i.e. the position of the potential minimum), at $x = x_{1,\min}$ and $x_{1,\min} < x \le L$ are the results of the negative, zero and positive slopes of the surface potential function (see Figs. 4.2 and 4.3), respectively. The smaller magnitude of the lateral electric field of the DMG structure at the drain end than that of the SMG structure shows that the DMG structure can improve the immunity to impact ionization and HCEs of the proposed device. However, the average electric field is

observed to be increased in the device which may increase the average speed of the carrier thereby reducing the transit time delay of the device.

4.4 Conclusion

Threshold voltage of ion-implanted s-Si DMDG MOSFETs has been modeled in this chapter. The effect of various device and doping parameters on the threshold voltage has been shown. It is found that the proposed DMG MOS structure with a Gaussian profile may provide additional flexibilities in terms of Gaussian profile parameters, control-to-screen gate length ratio and strain for optimizing the threshold voltage, DIBL and HCEs of the devices. Replacing the uniform doping by the Gaussian-like doping profile enables one to get the control over the subthreshold characteristics by simply changing doping parameters while maintaining other device parameters unchanged. The model results are found to be in good agreement with the TCAD simulation data obtained by the ATLAS™, a 2D device simulator from SILVACO.