Chapter 2

Analytical Modeling of Potential Distribution and Threshold Voltage of Graded-Channel Dual-Material Double-Gate MOSFETs

2.1 Introduction

We have already discussed in Chapter-1 that the graded channel (GC) MOSFETs have superior performance characteristics over the uniformly doped MOS transistors. It is also discussed that the GC MOSFETs (with a high doping near the source end and a low doping at the drain end [Kaur *et al.* (2008)]) have better drive current, lower short-channel-effects (SCEs) and lower hot-carriers-effects (HCEs) [Chen *et al.* (2002), Kaur *et al.* (2008), Kaur *et al.* (2007), Kranti *et al.* (2004)] than the conventional uniformly doped MOSFETs. On the other hand, the dual-material-gate (DMG) [Chiang and Chen (2007), Long *et al.* (1999), Kumar and Chaudhry (2004), Reddy and Kumar (2005), Chaudhry and Kumar (2004), Chiang and Chiang (2007)] and triple-material-gate (TMG) [Tiwari *et al.* (2010)] engineering in the MOSFETs can be explored for suppressing the SCEs and HCEs of the double-gate (DG) MOS structures. However, to the best of our knowledge, no significant research has been carried out in the literature to model the combined effects of GC engineering and DMG engineering on the subthreshold performance of the DG MOS structures. Thus, the objective of the present Chapter is to develop two-dimensional (2D) analytical models for the surface potential and threshold voltage characteristics of a newly proposed structure, named as graded-channel dual-material double-gate (GCDMDG)

MOSFETs, obtained by incorporating both the DGM engineering and GC engineering concepts in the DG MOS structures. The developed models will be validated by comparing them with the data obtained by using the commercially available ATLAS^{TM} based TCAD simulator. The layout of the present Chapter is given as follows:

Sec. 2.2 deals with the modeling of the surface potential and threshold voltage of the proposed device. The surface potential function in the channel has been obtained by solving the 2D Poisson's equation using parabolic approximation technique. The surface potential model has then been used to model the threshold voltage and drain-induced-barrier-lowering (DIBL) of the proposed GCDMDG MOSFET device under consideration. Some important results and discussions related to the surface potential, channel electric field, threshold voltage, and DIBL of the GCDMDG MOSFETs have been presented in Sec. 2.3. Finally, Sec. 2.4 includes the summary and conclusion of the present chapter.

2.2 Model Derivation

The schematic view of the proposed GCDMDG MOSFET under study is shown in Fig. 2.1 where the notations L, t_{si} and t_{ox} represent the channel length, silicon film thickness and oxide thickness (of both the front and back gates) respectively. The x-axis and y-axis of the 2D structure is taken along the front SiO_2/Si channel interface and the source-channel interface respectively as shown in the figure. The graded channel region consists of two non-overlapped regions 1 and 2 of respective lengths L_1 and L_2 and uniform doping concentrations of N_{a1} and N_{a2} where $L = L_1 + L_2$ and $N_{a1} > N_{a2}$. For achieving the DMG structure, two different gate electrode materials with work functions ϕ_{m1} and ϕ_{m2} (where

$\phi_{m1} > \phi_{m2}$) are used over the channel regions 1 and 2 respectively. We have assumed that the channel is fully depleted under zero-bias condition.

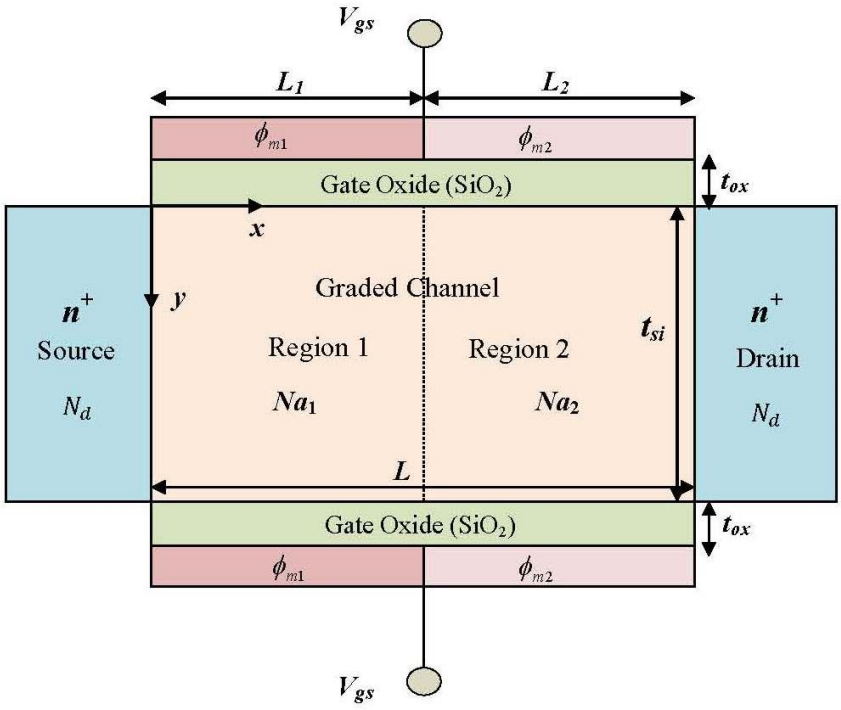

Fig. 2.1: Schematic Diagram of GCDMDG MOSFET

2.2.1 Modeling of Surface Potential

The 2D potential distribution, say $\psi_r(x,y)$, in the channel region can be obtained by solving the 2D Poisson's equation:

$$\frac{\partial^2 \psi_r(x,y)}{\partial x^2} + \frac{\partial^2 \psi_r(x,y)}{\partial y^2} = \frac{qN_{ar}}{\varepsilon_{si}} \tag{2.1}$$

where, $\psi_1(x,y)$ corresponding to the subscript $r=1$ denotes the potential function of region 1 and $\psi_2(x,y)$ for $r=2$ represents the potential distribution in the channel region 2.

We will now solve the 2D Poisson's equation in Eq. (2.1) for the potential function $\psi_r(x,y)$ in the r^{th} region for $r=1$ and 2 by assuming a symmetrical DG MOS structure (i.e. with identical front and back gate structure in the r^{th} region). Since the tangential electric fields should be continuous at the gate-oxide interfaces of both the front and back gates, we can use the following boundary conditions for the front and back gate-oxide/channel interfaces [Tiwari *et al.* (2010), Tiwari and Jit (2010(a)), Dubey *et al.* (2010a)]:

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_{gs}-V_{fbr}-\psi_r(x,0)\right]=-\varepsilon_{si}\left.\frac{\partial\psi_r(x,y)}{\partial y}\right|_{y=0} \tag{2.2}$$

$$\frac{\varepsilon_{ox}}{t_{ox}}\left[V_{gs}-V_{fbr}-\psi_r(x,t_{si})\right]=\varepsilon_{si}\left.\frac{\partial\psi_r(x,y)}{\partial y}\right|_{y=t_{si}} \tag{2.3}$$

where, ε_{si} and ε_{ox} are the permittivities of the silicon and SiO_2 gate-oxide layers respectively; q is the electronic charge; V_{gs} is the gate-to-source voltage; and V_{fbr} is the flat band voltage of the r^{th} channel region given by:

$$V_{fbr}=\phi_{mr}-\phi_{sir} \tag{2.4}$$

where, ϕ_{mr} is the work function of the gate-electrode metal in the r^{th} channel region and ϕ_{sir} is work function of the Si channel in the r^{th} channel region given by:

$$\phi_{sir}=\frac{\chi_{si}}{q}+\frac{E_{g-si}}{2q}+\phi_{F,sir} \tag{2.5}$$

where χ_{si} and E_{g-si} are the electron affinity and energy band-gap of the silicon respectively and $\phi_{F,sir}$ is the Fermi potential given as:

$$\phi_{F,sir} = V_T \ln\left(\frac{N_{ar}}{n_i}\right) \tag{2.6}$$

where, V_T is the thermal voltage and n_i is the intrinsic carrier concentration.

Using parabolic approximation method [Young (1989)], the potential distribution in the silicon film can be written as [Tiwari *et al.* (2010)]:

$$\psi_r(x,y) = C_{ro}(x) + C_{r1}(x)y + C_{r2}(x)y^2 \tag{2.7}$$

where, $C_{ro}(x)$, $C_{r1}(x)$ and $C_{r2}(x)$ are functions of x which can be expressed as follows.

Let the surface potential at the Si/SiO_2 interface below the front gate in the r^{th} channel region be denoted as $\psi_{rs}(x) = \psi_r(x,y)\big|_{y=0}$. Now putting $y=0$ in Eq.(2.7), we obtain

$$C_{ro}(x) = \psi_r(x,y)\big|_{y=0} = \psi_{rs}(x) \tag{2.8}$$

Using the boundary conditions of Eqs.(2.2) and (2.3) in Eq.(2.7), we can write

$$C_{r1} = -\frac{C_{ox}}{\varepsilon_{si}}\left(V_{gs} - V_{fbr} - \psi_{rs}(x)\right) \tag{2.9}$$

$$C_{r2} = \frac{C_{ox}}{t_{si}\varepsilon_{si}}\left(V_{gs} - V_{fbr} - \psi_{rs}(x)\right) \tag{2.10}$$

$$\text{where, } C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.11}$$

Using Eq.(2.7) in the Poisson's equation of Eq.(2.1) for $y=0$, the surface potential $\psi_{rs}(x) = \psi_r(x,y)\big|_{y=0}$ can be described as:

$$\frac{\partial^2 \psi_{rs}(x)}{\partial x^2} - \frac{1}{\lambda^2}\psi_{rs}(x) = -\frac{1}{\lambda^2}\sigma \tag{2.12}$$

where, $\frac{1}{\lambda^2} = \frac{2C_{ox}}{\varepsilon_{si} t_{si}}$ (2.13)

and $\sigma = V_{gs} - V_{fbr} - \frac{qN_{ar} t_{si}}{2C_{ox}} = V_{gs} + W_r$ (2.14)

where, $W_r = -V_{fbr} - \frac{qN_{ar} t_{si}}{2C_{ox}}$ (2.15)

The general form of the front surface potential function $\psi_{rs}(x)$ in the r^{th} channel region obtained from Eq.(2.12) can be expressed as [Tiwari *et al.* (2010)]:

$$\psi_{rs}(x) = A_r \exp\left(\frac{x}{\lambda}\right) + B_r \exp\left(\frac{-x}{\lambda}\right) + \sigma \tag{2.16}$$

where, $A_r\{r = 1, 2\}$ and $B_r\{r = 1, 2\}$ are the arbitrary constants to be determined by using the following boundary conditions [Tiwari *et al.* (2010)]:

$$\psi_{1s}(L_1) = \psi_{2s}(L_1) \tag{2.17}$$

$$\left.\frac{\partial \psi_{1s}(x, y)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial \psi_{2s}(x, y)}{\partial x}\right|_{x=L_1} \tag{2.18}$$

$$\psi_{1s}(0) = V_{bi1} \tag{2.19}$$

$$\psi_{2s}(L) = V_{bi2} + V_{ds} \tag{2.20}$$

where, V_{bi1}, and V_{bi2} are the built-in potentials at the source/channel and drain/channel junctions respectively and, V_{ds} is the drain-to-source voltage.

Using Eqs.(2.17)-(2.20) in Eq.(2.16) and rearranging the terms, we may write

$$B_1 = \gamma_1 V_{gs} + K_1 \tag{2.21}$$

where,

$$K_1 = \frac{W_1 D_2 + W_2 D_3 + D_1 + D_4}{D_5} \tag{2.22}$$

$$\gamma_1 = \frac{D_2 + D_3}{D_5} \tag{2.23}$$

$$D_1 = -2V_{bi1} + 2V_{bi2} \exp\left(-\frac{L}{\lambda}\right) \tag{2.24}$$

$$D_2 = 2 - \exp\left(\frac{-L_1}{\lambda}\right) - \exp\left(\frac{L_1 - 2L}{\lambda}\right) \tag{2.25}$$

$$D_3 = \exp\left(\frac{-L_1}{\lambda}\right) + \exp\left(\frac{L_1 - 2L}{\lambda}\right) - 2\exp\left(\frac{-L}{\lambda}\right) \tag{2.26}$$

$$D_4 = 2\exp\left(\frac{-L}{\lambda}\right) V_{ds} \tag{2.27}$$

$$D_5 = -2 + 2\exp\left(\frac{-2L}{\lambda}\right) \tag{2.28}$$

$$B_2 = \gamma_2 V_{gs} + K_2 \tag{2.29}$$

where,

$$\gamma_2 = \frac{D_9 + D_7 + D_8}{D_{10}} \tag{2.30}$$

$$K_2 = \frac{D_6 + W_1 D_7 + W_2 D_8}{D_{10}} \tag{2.31}$$

$$D_6 = K_1\left(\exp\left(\frac{-L_1}{\lambda}\right)-\exp\left(\frac{L_1}{\lambda}\right)\right)+V_{bi1}\exp\left(\frac{L_1}{\lambda}\right)-V_{bi2}\exp\left(\frac{L_1-L}{\lambda}\right)-V_{ds}\exp\left(\frac{L_1-L}{\lambda}\right) \quad (2.32)$$

$$D_7 = 1-\exp\left(\frac{L_1}{\lambda}\right) \quad (2.33)$$

$$D_8 = \left(\exp\left(\frac{L_1-L}{\lambda}\right)-1\right) \quad (2.34)$$

$$D_9 = \gamma_1\left(\exp\left(\frac{-L_1}{\lambda}\right)-\exp\left(\frac{L_1}{\lambda}\right)\right) \quad (2.35)$$

$$D_{10} = \exp\left(\frac{-L_1}{\lambda}\right)-\exp\left(\frac{-2L+L_1}{\lambda}\right) \quad (2.36)$$

$$A_2 = \alpha_2 V_{gs} + \beta_2 \quad (2.37)$$

where,

$$\alpha_2 = -\exp\left(\frac{-L}{\lambda}\right)-\gamma_2\exp\left(\frac{-2L}{\lambda}\right) \quad (2.38)$$

and

$$\beta_2 = \left(V_{bi2}+V_{ds}-W_2\right)\exp\left(\frac{-L}{\lambda}\right)-K_2\exp\left(\frac{-2L}{\lambda}\right) \quad (2.39)$$

$$A_1 = \alpha_1 V_{gs} + \beta_1 \quad (2.40)$$

where, $\alpha_1 = -1-\gamma_1$ (2.41)

and, $\beta_1 = \left(V_{bi1}-W_1\right)-K_1$ (2.42)

2.2.2 Modeling of Threshold Voltage

The threshold voltage (V_{th}) represents the gate-to-source voltage (V_{gs}) at which the minimum surface potential equals to twice the Fermi potential [Dubey *et al.* (2010a)]. Since the gate-electrode material over region 1 has higher work function than that of the gate-electrode material of region 2, the minimum surface potential will occur under the region 1. Further, for the moderately doped (with concentration $\geq 10^{16}$ cm^{-3}) channel considered in the present study, the leakage path is normally close to the surface and hence the threshold voltage can be determined from the surface potential by using the conventional definition as reported by others [Kaur *et al.* (2008), Kaur *et al.* (2007a), Dubey *et al.* (2010a)]. Thus, the threshold voltage can be obtained by solving the following equation [Kaur *et al.* (2008), Kaur *et al.* (2007a), Dubey *et al.* (2010a)]:

$$\psi_{1s,\min}\big|_{V_{gs}=V_{th}} = \psi_{1s}(x_{\min})\big|_{V_{gs}=V_{th}} = 2\phi_{F,si1} \tag{2.43}$$

where, $\psi_{1s,\min}$ and $\phi_{F,si1}$ are the minimum surface potential and Fermi potential in channel region 1; and the $x_{\min}$ represents the position of the minimum surface potential measured with respect to the source, which can be obtained by solving the following equation [Tiwari *et al.* (2010)]:

$$\left.\frac{d\psi_{1s}(x)}{dx}\right|_{x=x_{\min}} = 0 \tag{2.44}$$

Using the value of $x_{\min}$ in Eq.(2.43) and then solving the resultant equation, the threshold voltage can be described as:

$$V_{th} = V_{gs} = \frac{-D_{11} + \sqrt{(D_{11})^2 - 4D_{13}D_{12}}}{2D_{13}} \tag{2.45}$$

where,

$$D_{11} = 4(\alpha_1 K_1 + \beta_1 \gamma_1) - 2W_1 + 4\phi_{F,si1} \tag{2.46}$$

$$D_{12} = 4\beta_1 K_1 - W_1^2 - 4\phi_{F,si1}^2 + 4\phi_{F,si1} W_1 \tag{2.47}$$

$$D_{13} = 4\alpha_1 \gamma_1 - 1 \tag{2.48}$$

The DIBL has been calculated as the difference in the threshold voltages at two different drain-to-source voltages of 0.5 V and 0.05 V as follows

$$DIBL = V_{th}\big|_{V_{DS}=0.5} - V_{th}\big|_{V_{DS}=0.05} \tag{2.49}$$

2.3 Results and Discussion

In this section, model results of the proposed GCDMDG MOSFETs are compared with their corresponding results of the conventional dual-material double-gate (DMDG) MOSFETs [Kumar and Chaudhry (2004), Reddy and Kumar (2005)] and graded-channel double-gate (GCDG) MOSFETs [Kaur *et al.* (2007a), Kaur *et al.* (2007b), Kaur *et al.* (2008)], for investigating the merits of the GCDMDG MOSFETs over the DMDG and GCDG MOS structures. For the DMDG MOSFETs, the uniform doping of the channel has been assumed to be the arithmetic mean of N_{a1} and N_{a2} whereas the average value of ϕ_{m1} and ϕ_{m2} has been considered as the work function of the single-material-gate-electrode of the GCDG MOSFET structures. The drift-diffusion, CVT mobility (Lombardi Model), Fermi-Dirac carrier statistics and the standard SRH and Auger recombination models (*srh*

and *aug*) have been used for simulating all the device structures in the ATLAS^{TM} 2D device simulator.

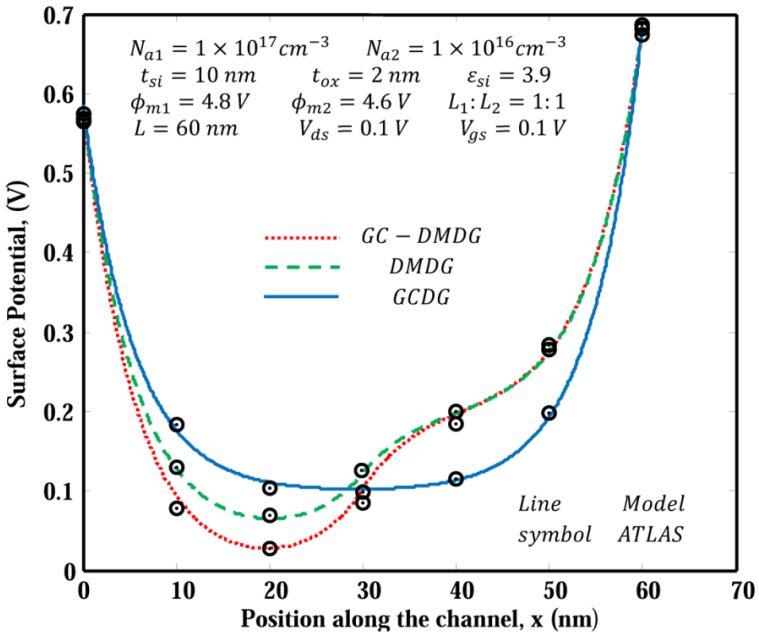

Fig. 2.2: Variation of surface potential along the channel for the three different structures with $L = 60nm$

First of all, the surface potentials of all the three MOS structures have been compared as a function of the position along the channel in Fig. 2.2 for the device parameters and bias voltages (i.e. $V_{gs} = V_{ds} = 0.1\,\mathrm{V}$) shown inside the figure. It is quite clear from the figure that the GCDMDG structure has the highest source-channel potential barrier (i.e. the largest threshold voltage) among all the three structures. This shows that GCDMDG MOSFET has the highest immunity to the SCEs among all the three MOS devices under study. Further, the position of the minimum surface potential of the DMDG and GCDMDG structures are observed to be much closer to the source than that of the GCDG structure. As a result, both the DMDG structures [Chiang and Chen (2007)] with and without a graded channel can

provide much better screening of the channel against the drain-to-source voltage fluctuations than the single gate GCDG MOS structure.

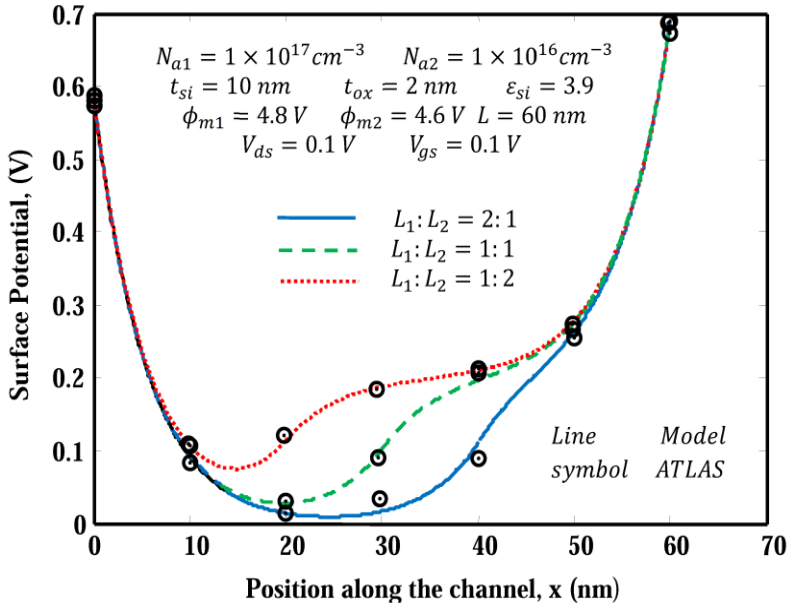

Fig. 2.3: Variation of surface potential along the channel for GCDMDG MOSFET for different values of $L_1 : L_2$ with $L = 60nm$

Figure 2.3 shows the variation of the surface potential as a function of x for the same parameters as used in Fig. 2.2 but with different control-to-screen gate length ratios ($L_1 : L_2$) for testing the pros and cons of different operating modes of GCDMDG MOSFETs. The source-to-channel barrier height (and hence the threshold voltage) is increased with the $L_1 : L_2$ value along with a shift in the position of the minimum channel potential towards the drain end. The shifting towards the drain with the increase in the $L_1 : L_2$ ratio may be explored for optimizing the threshold voltage roll-off [Bhushan *et al.* (2013)]. However, the decrease in the potential step at the junction of the two channel regions 1 and 2 enhances the influence of the drain-to-source voltage on the channel potential thereby indicating a

poor immunity to the DIBL with the increased $L_1 : L_2$ ratio of the device. One of the important features of the GCDMDG MOS structure observed from Fig. 2.3 is the tuning of the DIBL by changing the source-to-channel barrier in terms of the $L_1 : L_2$ ratio. A small decrease in the source-to-channel barrier obtained by decreasing the $L_1 : L_2$ ratio can increase the accumulation of the majority carriers of the substrate at the source end thereby reducing the DIBL of the device [Tsuchiya *et al.* (1998)]. Fig. 2.4 shows the variation of surface potential along the channel for GCDMDG MOSFET for different values of V_{gs} and V_{ds}. It is clear from the figure that with increasing value of V_{ds} potential minima is not affected much.

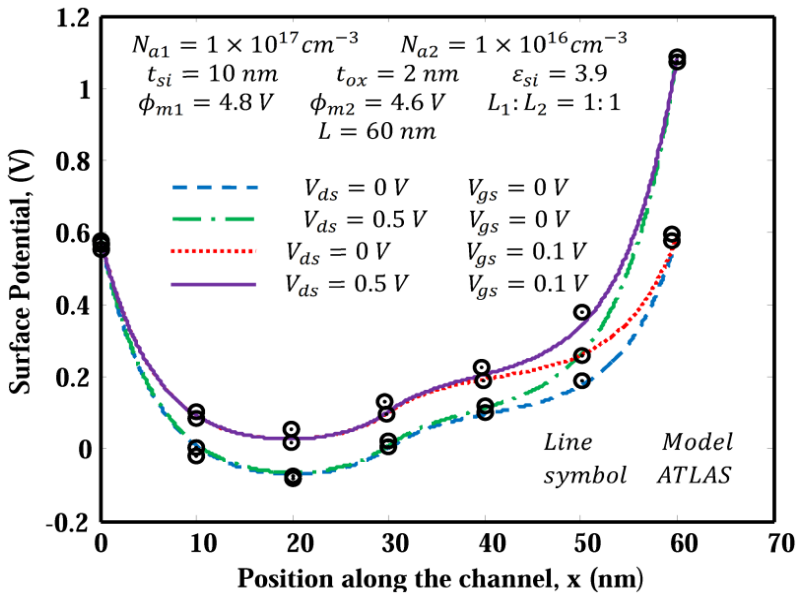

Fig. 2.4: Variation of surface potential along the channel for GCDMDG MOSFET for different values of V_{gs} and V_{ds} with $L = 60nm$

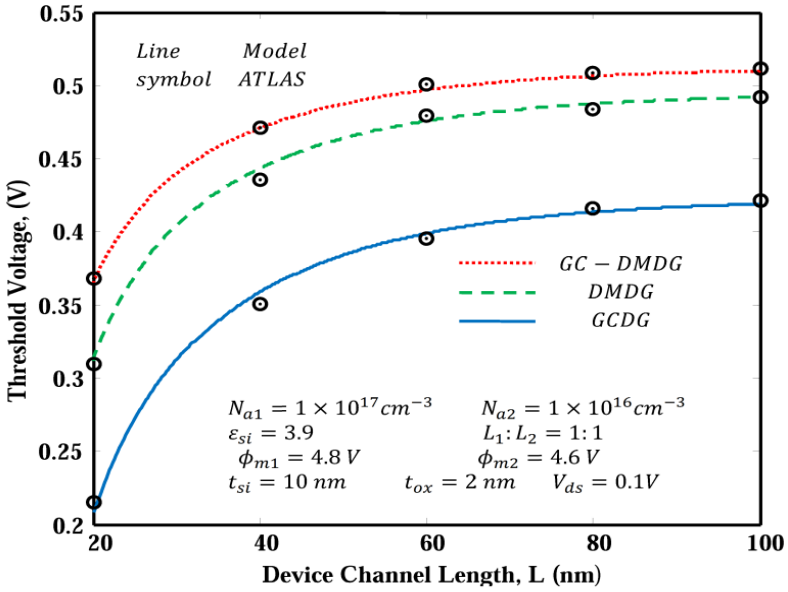

Fig. 2.5: Variation of threshold voltage with channel length for the three different structures.

The variation of threshold voltage against device channel length is plotted in Fig. 2.5 for all of the three MOSFETs considered in this study. The threshold voltage for GCDG MOSFET is found to be the minimum while the GCDMDG MOSFET structures possess the maximum value which is in synchronization with the results of Fig. 2.2. Thus, the off-sate leakage current is expected to be minimum in the GCDMDG MOSFETs among three structures. The largest source-to-channel barrier shown in Fig. 2.2 due to the combined effects of higher work function of the gate-electrode material and higher channel doping near the source end stops the diffusion of unwanted minority carriers into the channel region and reduces the threshold voltage roll-off in the proposed GCDMDG MOSFET structure. Clearly, the GCDMDG MOSFETs possess better control over the SCEs in terms of improved threshold voltage, lower subthreshold current and lower threshold voltage roll-off as compared to that of the DMDG and GCDG MOSFETs.

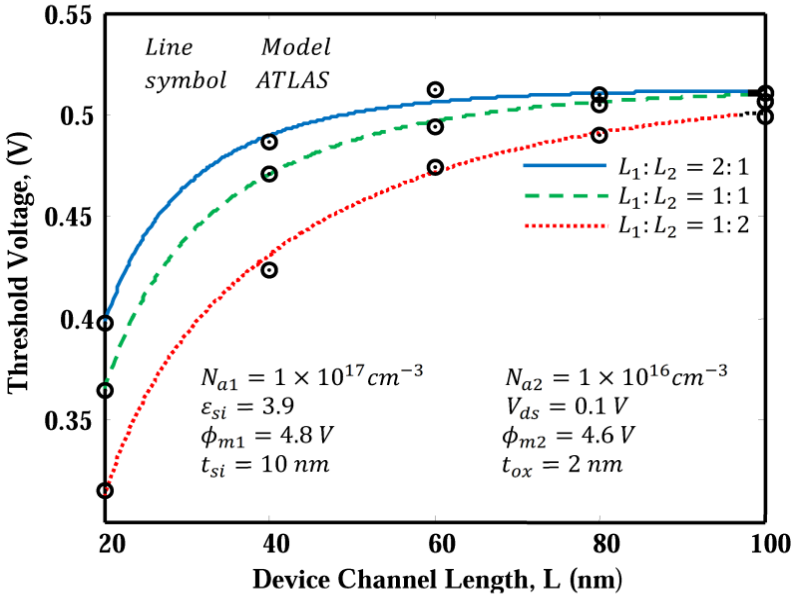

Fig. 2.6: Variation of threshold voltage with channel length for GCDMDG MOSFET for different values of $L_1 : L_2$.

The influence of gate length ratio ($L_1 : L_2$) on the variation of threshold voltage as a function of the channel length for GCDMDG MOSFETs has been shown in Fig. 2.6. It is observed that both the threshold voltage and threshold voltage roll-off are significantly improved (especially in the short-channel lengths below 40nm) with the increase in $L_1 : L_2$ ratio due to the increased source-to-channel barrier already discussed in Fig. 2.3. The effects of channel doping concentration and silicon channel thickness (t_{si})on the threshold voltage have been plotted as a function of channel length in Fig. 2.7 for two different doping concentrations $N_{a1} = 1\times10^{17}$ cm^{-3} and $N_{a1} = 5\times10^{17}$ cm^{-3} of region 1 and a fixed doping $N_{a2} = 1\times10^{16}$ cm^{-3} of region 2, while two different values of silicon channel thickness are taken as $t_{si} = 10nm$ and $t_{si} = 12nm$. Both the threshold voltage and its roll-off

are found to be improved with the increase in the source side doping (N_{a1}) due to the increase in the source-to-channel barrier height. The model results are observed to be well-matched with the ATLAS^{TM} simulation data. Since the threshold voltage can be varied by controlling the $L_1 : L_2$ ratio, gate-electrode-material work functions and doping concentrations of the two regions in the channel, the proposed GCDMDG MOSFETs are observed to provide better flexibility of threshold voltage optimization over the DMDG and GCDG MOS structures considered in this chapter. It is also clear from Fig. 2.7 that as L/t_{si} is decreased due to the increase in t_{si} but with a fixed L, the threshold voltage is degraded due to increased SCEs.

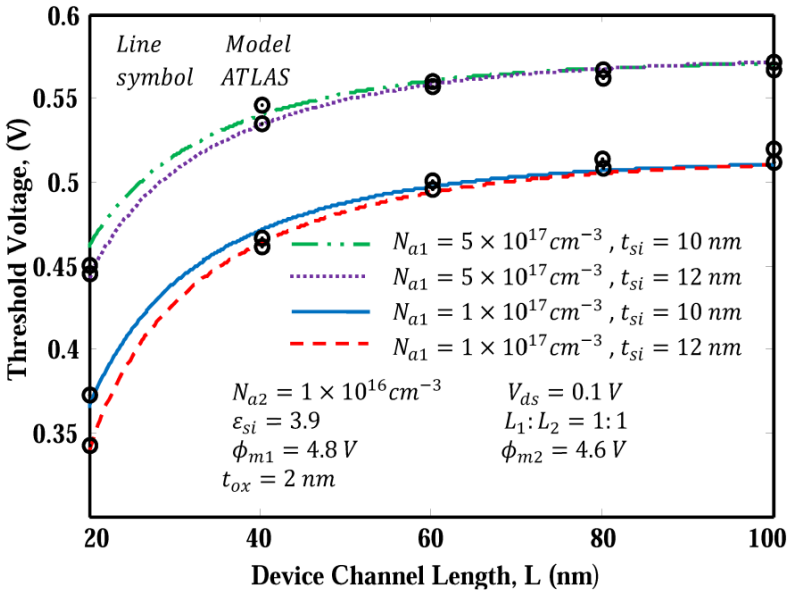

Fig. 2.7: Variation of threshold voltage with channel length for GCDMDG MOSFET for different values of t_{si} and N_{a1} keeping N_{a2} fixed.

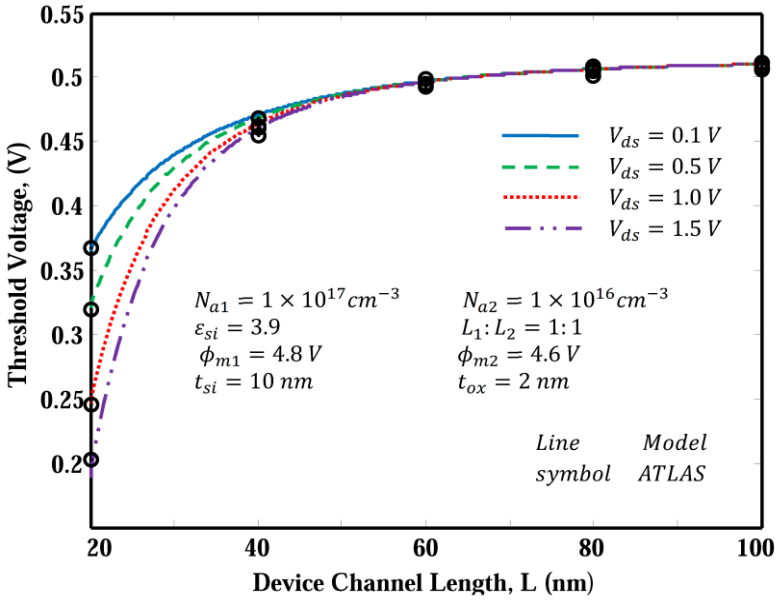

Fig. 2.8: Variation of threshold voltage with channel length for GCDMDG MOSFET for different values of V_{ds}

Fig. 2.8 shows the variation of threshold voltage against device channel length for GCDMDG structure for different values of V_{ds}. Clearly the threshold voltage is observed to be degraded with the increase in the drain-source voltage for smaller channel lengths especially below 40nm due to the well-known DIBL phenomenon.

In Fig. 2.9, the variations of threshold voltage roll-off and DIBL for all of the three considered devices have been compared as a function of the control gate length while maintaining all other device parameters constant. The DIBL has been calculated as the difference in the threshold voltages at two different drain-to-source voltages of 0.5 V and 0.05 V; and the threshold voltage roll-off is estimated as the threshold voltage difference between the long and short channel devices at a fixed drain-to-source voltage of 0.1 V.

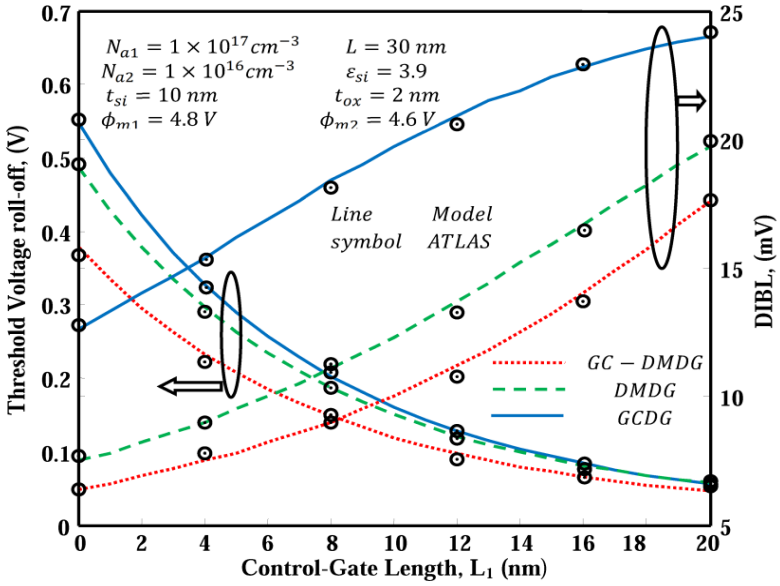

Fig. 2.9: Variation of threshold voltage roll-off and DIBL with control-gate length for the three different structures

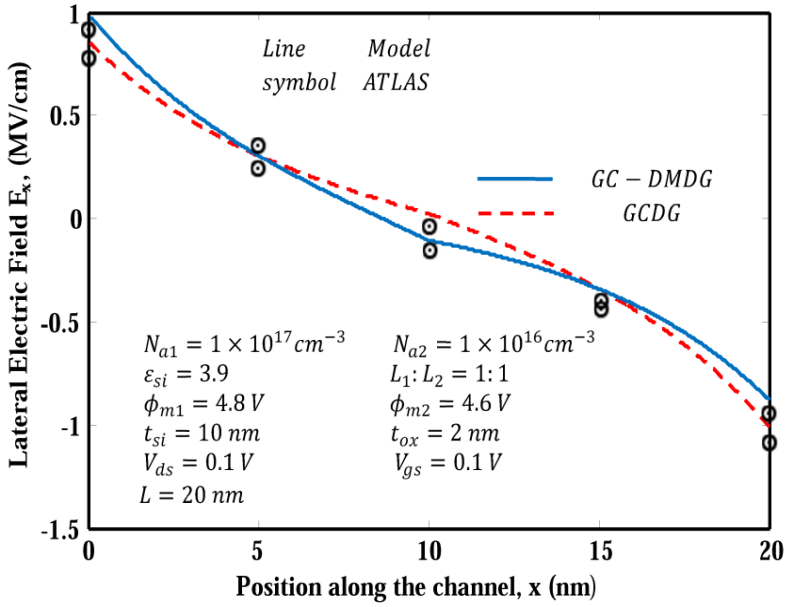

Fig. 2.10: Variation of lateral electric field along the position of the channel

Note that increase in the control-gate length (L_1) while keeping the total channel length (L) constant implies that the ratio ($L_1 : L_2$) is increased. Thus, the results of Fig. 2.9 basically represent the effects of the increased ratio $L_1 : L_2$ on the threshold voltage roll-off and DIBL for the three concerned structures. As discussed in Figs. 2.5 and 2.6, the Fig. 2.9 also clarifies that the threshold voltage roll-off and the DIBL are the lowest for the proposed GCDMDG MOSFETs among the three structures due to having the highest source-to-channel barrier. The lowering of threshold voltage roll-off with the increased length of control gate (L_1) is due to the increasing long channel behavior of the device. The lowest value of the DIBL of the proposed GCDMDG MOSFETs can be attributed to the position of the minimum channel potential closest to source end thereby providing the highest immunity to the detrimental DIBL in the proposed structure. However, DIBL is increased with the increased control gate length similar to Kumar *et al.* [Kumar *et al.* (2013b)] because of the shifting of the minimum surface potential from the source end towards the drain end where the threshold voltage sensitivity to the drain voltage fluctuation is maximum. Thus, the cross over point between the DIBL and threshold voltage roll-off characteristics in Fig. 2.9 can be chosen as the optimum value of gate length ratio for optimizing both the parameters under consideration in the figure. Both of the effects of DIBL and threshold voltage roll-off can be further optimized by selecting suitable values of the control and screen gate-electrode work functions and doping concentrations of the channel regions 1 and 2.

Finally, the variation of the lateral electric field $E_x = \frac{d\psi_{rs}(x)}{dx}$ along the position of the channel of the proposed GCDMDG MOS device is compared with that of the GCDG

MOSFET structure with 20nm gate length in Fig. 2.10 for investigating the merit of the proposed device in terms of the HCEs. It is clearly observed from the figure that the electric field in the proposed device is significantly reduced near the drain end. Thus, there is lower possibility of the velocity saturation near the drain thereby implying lower HCE of the GCDMDG structure over the simple GCDG structure.

2.4 Conclusion

In this chapter, a new analytical model for the surface potential and threshold voltage of short-channel GCDMDG MOSFETs has been presented. The parabolic approximation method has been explored for determining the potential distribution function of the device by solving the Poisson's equation with suitable boundary conditions. A comprehensive analysis has been carried out to investigate the effects of different device parameters on the surface potential profile, threshold voltage and SCEs. The degradations of threshold voltage, DIBL and HCEs with the decrease in the channel length are found to be effectively controlled by selecting the optimized values of the gate length ratio, doping concentrations in the two regions of the channel and the work functions of the control and screen gate electrode materials. It has been found that performance of the DG MOSFETs can be significantly improved in the GCDMDG MOSFETs obtained by combining the graded channel and dual material engineering in a single MOS structure. A reasonably good agreement between the analytical and the simulated results obtained from the 2D ATLAS^{TM} device simulator shows the validity of the model reported in this chapter.