Chapter 1

Introduction and Scope of the Thesis

1.1 Introduction

The discovery of metal-oxide-semiconductor field effect transistors (MOSFET) [Kahng and Atalla (1960)] created a revolutionary growth and development in the integrated circuit (IC) technology. The relentless scaling of the MOS transistors has enabled us to integrate billions of transistors on a single wafer for developing high-performance and low-power ICs for various computing and communication applications. Scaling of MOS devices refers to the miniaturization or reduction of dimensions of the devices by attempting to maintain the electrical characteristics of the devices unchanged. One of the most important objectives of the scaling of MOS transistors is to increase the integration of more and more number of transistors in a unit area of the chip to achieve complex ICs with multifunctional features to reduce the cost per function of the ICs. Further, scaled MOSFETs with smaller gate-lengths provide smaller transit time for charge carriers and hence higher speed of operation of the transistors. They are supposed to provide higher drain current [Streetman and Banerjee (2006)] due to smaller channel length and better switching characteristics due to smaller gate capacitance [Sviličić and Kraš (2006)].

In 1965, Gordon E. Moore made a systematic investigation on the increase in the integration level of transistors in the ICs developed during 1958-1965 and observed that the number of transistors integrated in the ICs was nearly doubled every year. Based on his observation, he predicted that the same trend would continue till 1975 [Moore (1965)]. However, after observing the actual trend in the increase in number of

components per chip upto 1975, Moore modified his prediction by stating that the rate of increase in the number of components per chip would be double in every two years period [Moore (1975)], instead of every year as originally predicted earlier in 1965 [Moore (1965)]. This prediction, commonly known as the *Moore's law*, has become the guiding principle behind the tremendous growth and development of the IC technology in the microelectronics industry which is still valid even after more than four decades. In 1997, most of the leading semiconductor industry had introduced the 250 nm process node. Subsequently, ICs with several technological nodes namely the 180 nm, 130 nm, 90 nm, 65 nm and 45 nm process nodes have been marketed at different times by the semiconductor industries. The 14 nm node based ICs has first shipped to consumers by the Intel in 2014 while the Samsung has released their product based on 10 nm process node in 2017. Recently, the TSMC has announced that they will start the production of 7 nm node based ICs in 2018 [Internet resource (IR1)]. Fig. 1.1 (a) shows the change in the logic transistor density (in million transistors per mm unit) for different technology nodes from 45 nm to 10 nm while the corresponding scaling of the chip area of the Intel logic has been shown in Fig. 1.1 (b).

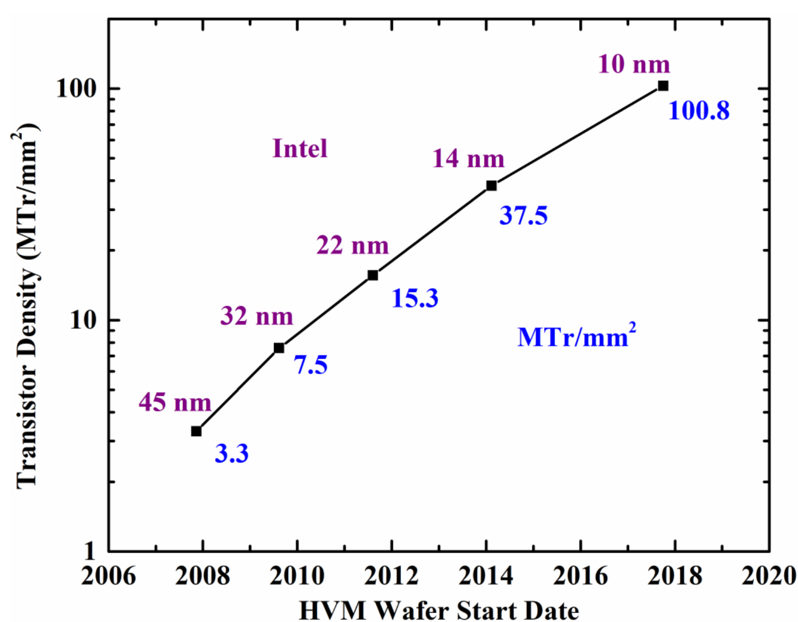

Fig.1.1 (a): Intel logic transistor density

It is important to mention that scaling does not imply the reduction only in the gate length of the MOS transistors but also the reduction in other device parameters such as the oxide thickness, channel thickness, applied bias voltages, threshold voltages etc. Scaling of different parameters mentioned above is done by following rules [Dennard *et al.* (1974), Taur and Ning (1998)]. Some of the important scaling rules are described in brief in the following.

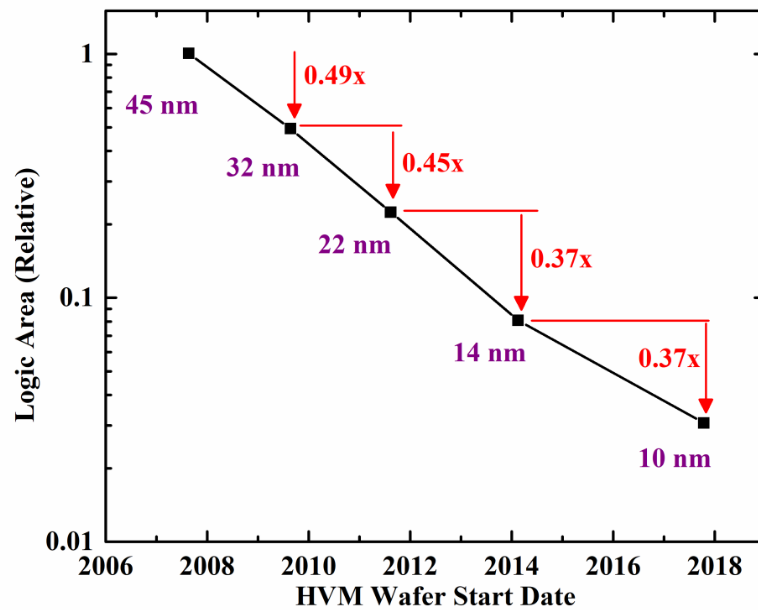

Fig.1.1 (b): Intel logic area scaling

In 1974, Dennard *et al.* [Dennard *et al.* (1974)] has proposed a scaling theory, called the constant field scaling, where electric fields are maintained to be unchanged in the original and the scaled MOS transistors. Under this scaling theory, if the channel length of a MOS device is scaled by a factor 'β', then the source/drain channel junction depth, gate oxide thickness, supply voltages and the threshold voltage are also required to be scaled by the same factor 'β' while the substrate doping is increased by the factor 'β'. The constant field scaling increases the switching speed by the factor of 'β' (by reducing the transit time delay by 'β') and decreases in the power dissipation by a factor

of “1/ β^2”, power-delay product by a factor of “1/ β^3”. The major drawback of this scaling theory is that it reduces the threshold voltage and the bias voltages drastically thereby making them unsuitable for practical applications. To avoid the scaling of the bias voltages, another scaling theory, namely the constant voltage scaling, is proposed by Taur and Ning [Taur and Ning (1998)]. Like the constant field scaling, all the device dimensions are scaled down by the factor ‘β’ with the increase in the doping concentration by the same factor ‘β’ while the supply voltages are kept constant in this scaling method. This scaling principle results in an enhanced speed of the device by a factor of “β^2” at the cost of increased power dissipation by a factor of “β”. Thus the constant voltage scaling is suitable for high-speed applications at the cost of increased power dissipation in the ICs. The effects of constant field and constant voltage scaling on various parameters of the device have been compared in Table 1.1. Note that the increased doping concentration by the factor of “β” in the scaling leads to the degradation of the mobility of carriers due to increased impurity scattering. Further, the higher switching speed is achieved at the cost of increased power dissipation in the constant voltage scaling. Table 1.1 also shows a generalized scaling rules proposed by Taur and Ning [Taur and Ning (1998)] obtained by mixing the principles of the constant field and constant voltage scaling rules for optimizing the device performances for high-speed and low-power applications.

It is clear from the scaling theory that the reduction in gate-length of the MOS transistors improves the speed of operation at the cost of increased power dissipation per unit area. The scaling of gate-oxide thickness increases the oxide capacitance which in turn reduces the threshold voltage of the device. The decrease in threshold voltage with the reduced channel length causes more carriers to overcome the source/channel barrier to result in the increase of subthreshold current (SC) of the transistors. The

increase in substrate doping to enhance the threshold voltage decreases the mobility and hence reducing speed of the device due to increased impurity scattering. There is also possibility that the depletion regions at the source/channel and drain/channel junctions of the conventional bulk MOSFETs may overlap each other (i.e. punch through condition) to cause the carrier flow directly from the source to drain irrespective of the gate voltage of the device. The gradual channel approximation becomes invalid for such small geometry MOS transistors.

Table 1.1 Scaling of device dimensions and circuit parameters [Dennard *et al.* (1974), Baccarani *et al.* (1984), Taur and Ning (1998)]

<table>
<tr><th colspan="2" rowspan="2">Device Parameter</th><th colspan="4">Multiplication Factor, $\beta > 1$
Scaling parameter, α</th></tr>
<tr><th>Constant-field Rules</th><th>Constant-voltage Rules</th><th colspan="2">Generalized Rules</th></tr>
<tr><td rowspan="3">Scaling assumption</td><td>Device dimensions</td><td>$1/\beta$</td><td>$1/\beta$</td><td colspan="2">$1/\beta$</td></tr>
<tr><td>Doping concentration</td><td>β</td><td>β</td><td colspan="2">$\alpha\beta$</td></tr>
<tr><td>Voltage</td><td>$1/\beta$</td><td>1</td><td colspan="2">α/β</td></tr>
<tr><td rowspan="8">Derived scaling behavior of device parameters</td><td>Electric field</td><td>1</td><td>β</td><td colspan="2">α</td></tr>
<tr><td>Depletion Layer width</td><td>$1/\beta$</td><td>$1/\beta$</td><td colspan="2">$1/\beta$</td></tr>
<tr><td>Capacitance</td><td>$1/\beta$</td><td>$1/\beta$</td><td colspan="2">$1/\beta$</td></tr>
<tr><td>Inversion/Layer charge density</td><td>1</td><td>β</td><td colspan="2">1</td></tr>
<tr><td colspan="3"></td><td>Long channel</td><td>Velocity Saturation</td></tr>
<tr><td>Carrier velocity</td><td>1</td><td>β</td><td>A</td><td>1</td></tr>
<tr><td>Drift current</td><td>$1/\beta$</td><td>β</td><td>α^2/β</td><td>α/β</td></tr>
<tr><td>Channel resistance</td><td>1</td><td>$1/\beta$</td><td>α^2/β</td><td>α/β</td></tr>
<tr><td rowspan="4">Derived scaling behavior of circuit parameters</td><td>Circuit delay time</td><td>$1/\beta$</td><td>$1/\beta^2$</td><td>$1/\alpha\beta$</td><td>$1/\beta$</td></tr>
<tr><td>Power dissipation per circuit</td><td>$1/\beta^2$</td><td>β</td><td>α^3</td><td>α^2/β^2</td></tr>
<tr><td>Power density</td><td>1</td><td>β^3</td><td>α^3</td><td>α^2</td></tr>
<tr><td>Power-delay product per circuit</td><td>$1/\beta^3$</td><td>β</td><td colspan="2">α^2/β^3</td></tr>
</table>

In this case, the electric field becomes a two dimensional function which makes the threshold voltage a function of the drain voltage. In brief, the channel lengths below a critical value deteriorates the performance of the MOS transistors severely by increasing the standby power dissipation, drain induced barrier lowering (DIBL) or threshold voltage lowering, threshold voltage roll-off, subthreshold slope roll-up, punch through and many more. All these effects are collectively known as the short-channel-effects (SCEs). The scaling of bulk MOSFET has already reached its bottleneck due to severe SCEs. Thus, researchers have reported several non-conventional MOS transistors by incorporating modifications in the device structure, gate-oxide dielectric, channel material and channel doping profile, source/drain material and structures, gate-electrode materials etc. Some of the important techniques for optimizing the SCEs are discussed in brief in the following.

1.2 Gate Engineering Techniques

The gate engineering techniques basically include any modification in the gate structure of the MOS devices to suppress the SCEs. The gate engineering techniques may include any one or more than one of the following gate structural modifications in the MOS device:

- Replacement of the single gate by multi-gate structures. The use of multiple number of gates in place of the conventional single gate reduces the SCEs by enhancing the gate control over channel of the MOS transistors [Huang *et al.* (1999), Colinge (2004), Doyle *et al.* (2003), Sharma and Vishvakarma (2013), Chiang (2014), Li *et al.* (2011)].
- Replacement of the conventional poly-Si gate electrode material by two or more number of materials of different work functions connected in non-overlapped cascade

manner in the descending order of wok functions from the source to drain side. When the MOSFETs use the combination of two (or three) materials connected in cascade to form the gate electrode, we call them double-material-gate (DMG) (or triple-material-gate (TMG)) MOSFETs [Zhou (2000), Long *et al.* (1999), Kumar and Chaudhry (2004) Reddy and Kumar (2005), Tiwari *et al.* (2010)].

- Replacement of conventional SiO_2 by other high-*k* dielectric materials (i.e. HfO_2, ZrO_2, $ZrSiO_4$, $HfSiO_4$ etc.). The SiO_2/high-*k* stacked gate oxide structures have also been explored by many researchers [Chau *et al.* (2004), Lee *et al.* (2006)].

1.2.1 Multiple-Gate Structure Based MOS Devices

The multiple gate MOS device structures include FinFETs (double-gate) [Huang *et al.* (1999), Colinge (2004)]**,** tri-gate MOSFET [Doyle *et al.* (2003)], quadruple gate MOSFETs [Sharma and Vishvakarma (2013), Chiang (2014)], and gate-all-around (GAA) /cylindrical Gate MOSFETs [Li *et al.* (2011)]. Among the above, the double-gate (DG) MOSFETs are the most widely explored MOS structure for future generation IC technology. It can be planar or vertical depending upon the way of creating the control of the gate over the channel or simply how the gate is wrapped over the channel. In DG planar structure, the gate control is formed at the top and bottom sides of the channel as shown in Fig. 1.2(a) [Park *et al.* (2001), Ferain *et al.* (2011)]. On the other hand, the gate is wrapped on left and right sides of the channel in the vertical DG MOS structure as shown in Fig. 1.2(b) where the gate control is exerted on the channel from the lateral sides of the device. The vertical DG MOSFET is also known as double gate FinFET structure [Huang *et al.* (1999), Colinge (2004), Ferain *et al.* (2011)]. It may be noted that the thick dielectric in the FinFETs prevents the formation of an inversion layer at the top of the silicon fin. Thus, in the tri-gate configuration, the gate control is

also exerted on the channel from the top in additional to the control from the left and right sides in the case of DG structure as shown in Fig. 1.2(c) [Ferain *et al.* (2011)]. The tri-gate effect can also be realized in the Π-gate MOSFET structure where the parallel vertical gate electrodes are inserted to some depth in the buried oxide as shown in Fig. 1.2(d) [Park et al. (2001)]. However, in the Π-gate MOS structure, the gate control over the channel is better than the tri-gate MOSFETs since the electric field from the lateral sides of the gate also exerts some control on the bottom side of the channel. To achieve better gate control than the tri-gate structures, the Ω-gate MOS structure has also been introduced where the gate almost wraps around the body except a small gap at the middle of the bottom channel as shown in Fig. 1.2(e) [Yang et al. (2002)]. The gate control of the bottom of the channel region in the Ω-gate is better than that in the Π-gate MOSFETs. Note that the names Π-gate and Ω-gate simply reflect the shape of the gate structures. In the quadruple-gate MOSFETs, the gate control is provided from all the four sides of the channel of the device. It can be considered as an extended version of the Ω-gate where the bottom gate covers the entire bottom part of the channel. The quadruple-gate MOSFET is supposed to provide better improvement in the SCEs than the double-gate and triple-gate MOSFET structures [Chiang (2014)]. The cylindrical MOS structures [Wegener (1953), Oh *et al.* (2000), Auth, and Plummer (1997)] shown in Fig. 1.2 (g) also provide excellent gate control over the channel. In this structure, the gate electrodes wrap around the channel region to exhibit excellent electrostatic control of the gate on the channel without any floating body effect. Thus, the gate-all-around (GAA) MOS structures are expected to have better scalability with smaller SCEs and subthreshold swing (SS) over the other multi-gate MOS structures. However, fabrication complexities of such non-planner MOS structures are the major limitation for the large scale IC applications.

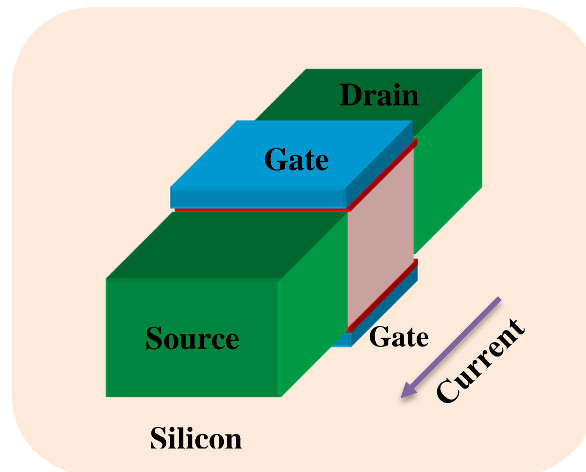

Fig. 1.2(a): Planar Double-Gate MOS structure

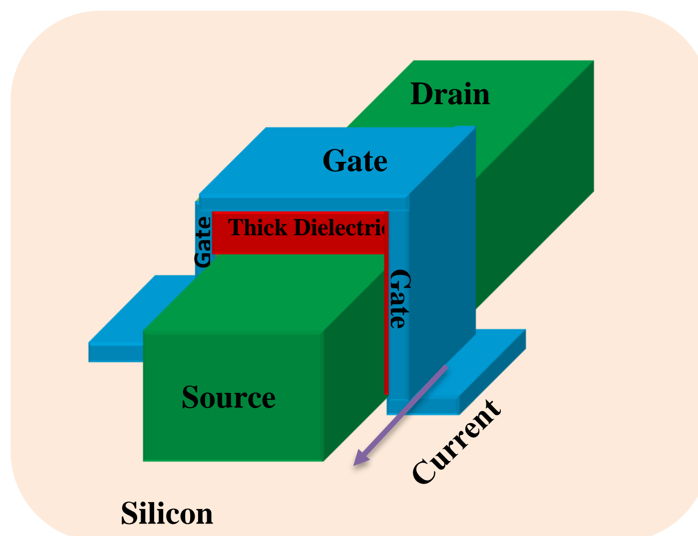

Fig. 1.2(b): FinFET (Double-Gate) MOS structure

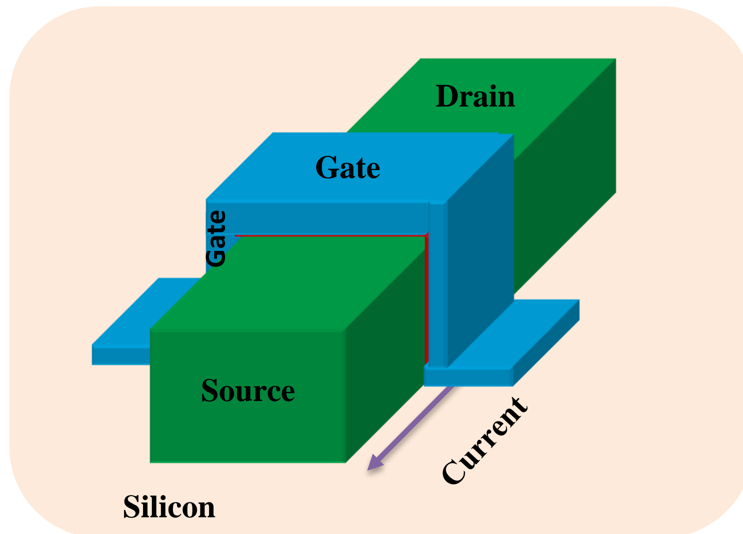

Fig. 1.2(c): Tri-gate MOS structure

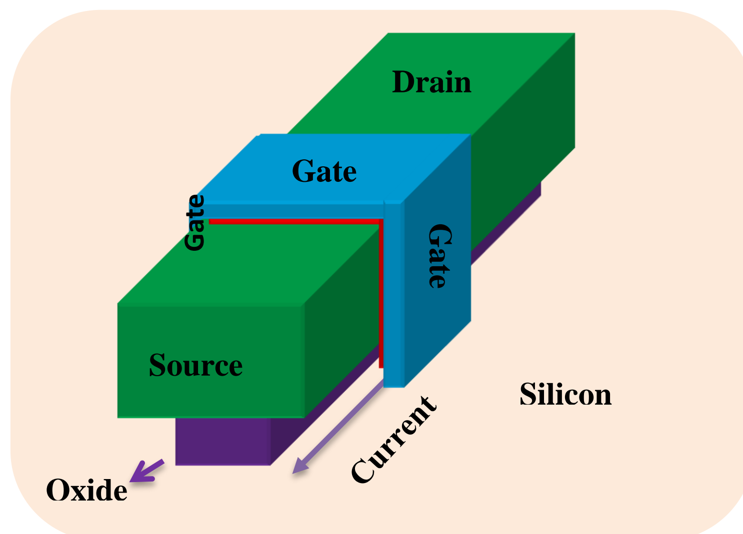

Fig. 1.2(d): Π-gate MOS structure

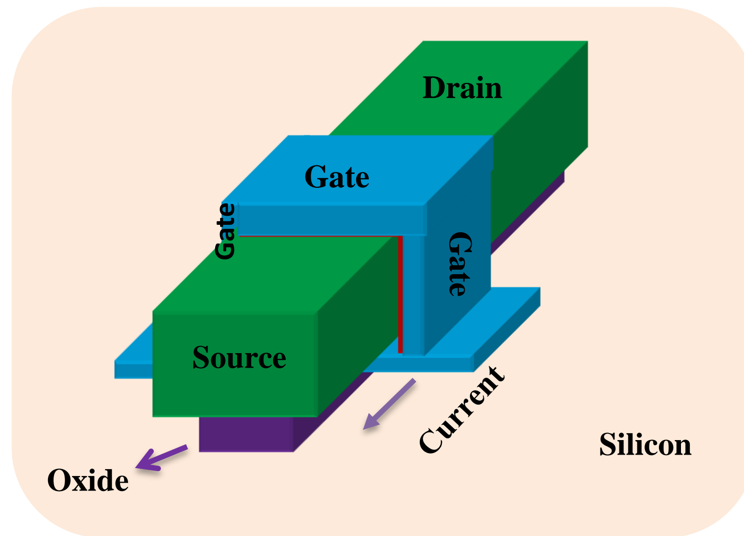

Fig. 1.2(e): Ω-gate MOS structure

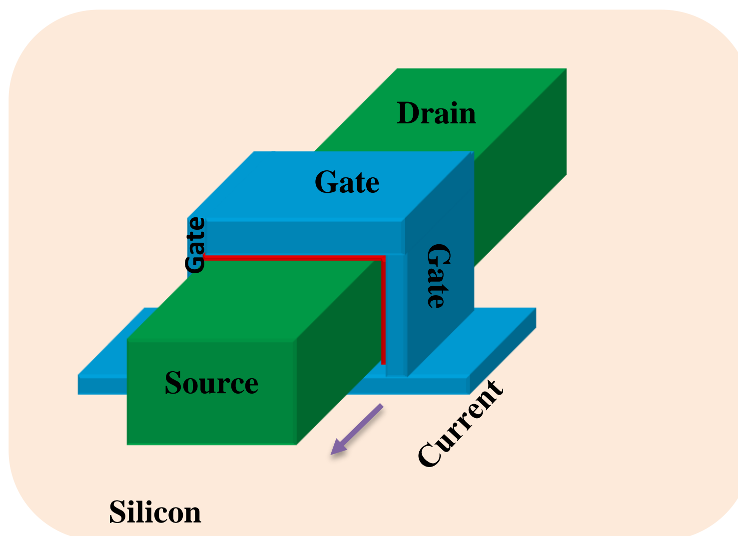

Fig. 1.2(f): Gate-All-Around (GAA) MOS structure

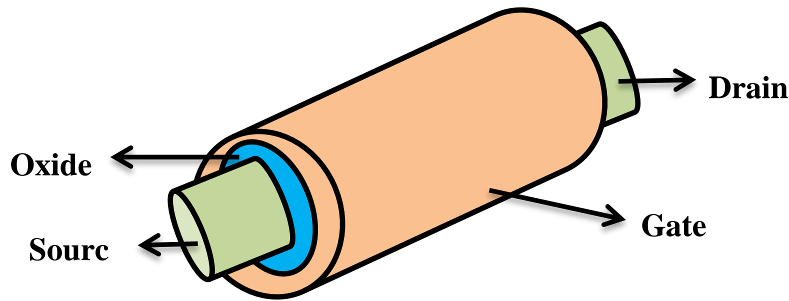

Fig. 1.2(g): Cylindrical Gate MOS structure

1.2.2 Multi-Material (Hetero Material) Gate Electrodes

The principal idea behind using the gate-electrode-material engineering is to tune the channel electric-field profile in such a manner that it becomes large at the source side to accelerate carriers towards the drain but it should be very small at the drain side to reduce the kinetic energy of the carriers to avoid HCEs [Zhou (2000), Long *et al.* (1999), Kumar and Chaudhry (2004), Reddy and Kumar (2005), Tiwari *et al.* (2010)]. The basic idea in the multiple gate-electrode-material based MOS devices is to use more than one metal-like materials with different work functions placed in the non-overlapped manner on the gate-oxide in the descending order of the work function values from the source to drain end so that the material with the highest work function exists at the source side and the material with the lowest work function is at the drain side. The material with the largest work function placed at the source side is called the control gate while the material with the smallest work function at the drain side is called the screen gate in the MOS device. The step-like discontinuities in the channel electric field at the boundary of two different gate-electrode materials are explored to reduce the electric field at the drain side to suppress the SCEs and HCEs [Zhou and Long (1998)]. The DMG is the simplest one which uses only two different materials placed in the cascaded and non-overlapped manner to form the gate electrode of the MOSFET [Zhou (2000), Long *et al.* (1999), Kumar and Chaudhry (2004), Reddy and Kumar (2005)].

Such type of gate electrode structure in the MOS devices reduces the peak electric field at the drain end while maintaining a high average electric field under the gate which increases the gate control over the conductance of the channel thereby increasing the gate transport efficiency of the device [Kumar and Reddy (2004)]. Based on the TCAD simulation, Razavi *et al.* [Razavi and Orouji (2008)] have demonstrated the superiority of the triple-material double-gate (TM-DG) MOSFETs over the double-material double-gate (DM-DG MOSFETs) and conventional DG MOSFETs. Tiwari *et al.* [Tiwari *et al.* (2010)] have theoretically shown the superiority of the TM-DG MOSFETs over the DM-DG MOSFETs.

1.2.3 High-*k* Dielectric Based MOSFETs

The thickness of the SiO_2 gate-oxide in various MOS devices has reached its bottleneck due to continuous reduction through relentless scaling of the MOS transistors over more than four decades. The further decrease in the oxide thickness may increase excessive gate leakage current through quantum mechanical tunnelling of the carriers from the channel to the gate of the device. In order to sustain the scaling, researchers have used dielectrics with higher permittivities than SiO_2 as the gate-oxide in the MOS transistors [Chau *et al.* (2004), Lee *et al.* (2006), Wilk *et al.* (2001)]. The basic objective of using such high-*k* dielectric materials as gate-oxide in the MOS devices is to achieve the same gate-oxide capacitance in the SiO_2 based device at larger oxide thickness in the high-*k* materials based device to optimize the gate leakage current through quantum mechanical tunnelling phenomena. On the other hand, for a fixed oxide thickness, the MOSFET using high-*k* dielectrics will result in higher drain current that the device with SiO_2 as gate-oxide due to larger gate oxide capacitance [Wilk *et al.* (2001)]. Thus, the

high-*k* gate-oxide engineering can be explored for optimizing the gate-leakage current as well as drive current of the MOSFETs [Chau *et al.* (2004), Lee *et al.* (2006)].

1.3 Channel Engineering Techniques

Channel engineering techniques involve the modification of the silicon channel region of the MOS transistors by following methods:

- By using different doping profiles in the channel.
- By using a strained-Si (s-Si) channel to modulate the mobility of the channel carriers in the MOSFETs.

It may be mentioned that an undoped or lightly doped channel in the MOSFETs is always desirable for the high-speed switching applications [Lu *et al.* (2008)] since the increase in doping in the channel reduces the carrier mobility by increased impurity scattering. However, the requirement of increased channel doping is a part and parcle of the scaling to prevent the degradation in the threshold voltage of the device as already discussed earlier. Thus the channel doping engineering can be used for suppressing the SCEs and HCEs in the device. It may also be mentioned that the commonly assumed uniform channel doping in practical MOS transistors are not practically feasible due to various fabrication constrains [Cerdeira *et al.* (2008(a)), Bhattacherjee and Biswas (2008)]. A number of different forms of non-uniform or asymmetric doping profile like halo doping [Din *et al.* (2003)] , retrograde channel doping [Agrawal *et al.* (1996), Gwoziecki *et al.* (1999)], laterally asymmetric channel doping [Yu *et al.* (1997), Taur and Nowak (1997)], graded channel doping [Pavanello *et al.* (2000a), Pavanello *et al.* (2000b), Chen *et al.* (2002), Kaur *et al.* (2007a), Kaur *et al.* (2007b), Kaur *et al.* (2008)] and Gaussian doping profile [Sze (1981), Zhang *et al.* (2008)] have been reported in the literature. In general, additional parameters of the non-uniform channel doping profile

may provide additional flexibilities for optimizing the performance of the MOS transistors [Taur and Ning (1998)]. Some important channel doping engineering techniques are discussed in brief in the following subsections.

1.3.1 Graded Channel Doping Profile

The idea of a graded-channel device was first introduced by DeMassa and Goddard in 1971 [DeMassa and Goddard (1971)] and DeMassa and Catalano in 1973 [DeMassa and Catalano (1973)]. Inhomogeneous channel resistivity profile obtained by using heavier doping near the source than the drain end was predicted to improve the high frequency performance of several field-effect devices without reducing the gate lengths of the device. In 1978, Williams and Shaw [Williams and Shaw (1978)] reported the improved linearity and noise figure of the FET using a graded-channel in the device. The RF-favoured performance of the graded-channel devices over the uniformly doped devices was highlighted in 1980 by Malhi and Salama [Malhi and Salama (1980)] where they reported a higher cutoff frequency for graded-channel FET.

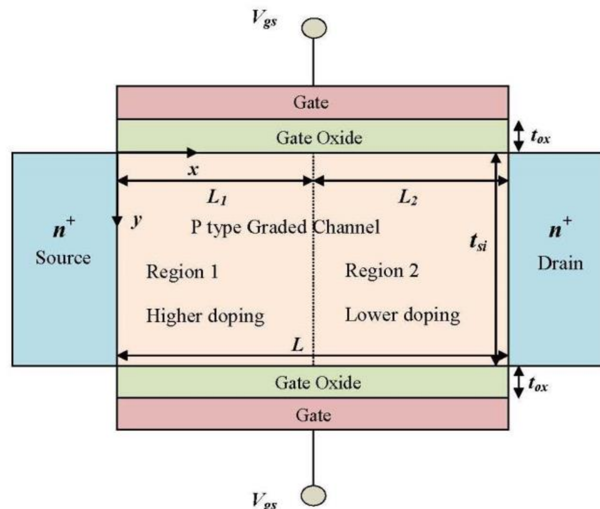

Fig. 1.3: Graded Channel Double Gate MOSFET

The lateral graded-channel (GC) doping engineering in the MOS transistors maintains a high doping near the source end and a low doping at the drain end as shown in Fig. 1.2. The GC doping profile gives improved drive current, reduced SCEs, and reduced HCEs in MOS transistors [Pavanello *et al.* (2000a), Pavanello *et al.* (2000b), Chen *et al.* (2002), Kaur *et al.* (2007a), Kaur *et al.* (2008)]. The low-doped region near the drain end reduces the electric field thereby reducing the impact ionization and, hence the HCEs at the drain side of the MOS devices.

1.3.2 Gaussian Channel Doping Profile

Channel doping profile of practical MOS transistors are nonuniform in nature due to several processing steps like diffusion and ion-implantation involved during the fabrication process of the device [Suzuki *et al.* (2007), Zhang *et al.* (2008)]. Since the threshold voltage of any MOSFET is a function of the channel doping profile, the additional parameters of any nonuniform doping profile in the channel of a MOSFET may provide additional flexibility for optimizing performance of the device. The ion-implantation is widely used for the precise control of the distribution of dopants in the channel of the MOS devices [Wick (1970)]. In general, the ion-implantation results in the Gaussian doping profile, say $N_b(y)$, in the channel [Sze (1981), Zhang *et al.* (2008)] which can be mathematically described by

$$N_b(y) = N_p \, exp\left[-\frac{\left(y-R_p\right)^2}{2\sigma_p^2} \right] \tag{1.1}$$

where σ_p and R_p are called the straggle and projected range and, N_p is the peak doping concentration at $y = R_p$.

The Gaussian profile is considered to be the most general doping profile in semiconductors since a number of different doping profiles can be derived by changing the values of the straggle parameter and the projected range of Gaussian profile [Sze

(1981), Zhang *et al.* (2008)]. However, the major problem with the ideal Gaussian doping profile is that it is a non-integrable function over any finite interval. Note that the integration of a Gaussian function over any finite interval is expressed in terms of the error function which is non-analytic in nature. As a consequence of the above, it is not possible to achieve a closed form analytical solution of the Poisson's equation for obtaining the surface potential function of any MOS transistors with a Gaussian doped channel [Pandey *et al.* (2004), Tiwari and Jit (2010(a)), Tiwari *et al.* (2011(a))]. In order to achieve analytical solution for the potential function of the MOS devices with a Gaussian distributed channel profile, Dasgupta and Lahiri [Dasgupta and Lahiri (1986)] has proposed a new function which is closely resembled the Gaussian function and can be integrated twice over any finite interval. We call this as the Gaussian-like doping function which can be expressed as [Dasgupta and Lahiri (1986)]

$$N_b(y) \cong N_p\, c\left((a + 2b\alpha Y)^2 - 2b\right)\exp\left(-a\alpha Y - bY^2\right) \tag{1.2}$$

where, $Y = \dfrac{y - R_p}{y_b}$, R_p being the projected range, $y_b = \sqrt{2}\,\sigma_p$ where σ_p is the straggle of the Gaussian profile; N_p is the peak doping concentration at $x = R_p$; a , b and c are the fitting constants having values $a = 1.786, b = 0.646$ and $c = 0.56$; $\alpha = +1$ for $y \geq 0$ and -1 for $y \leq 0$, involved in the Gaussian-like function. Figure 1.4 shows a comparison between the actual Gaussian (green line) and Gaussian-like functions (red line). Thus, for achieving a simplified but yet accurate enough analysis of the MOSFET characteristics with an ion-implanted channel, the analytic Gaussian-like function may be treated as an excellent approximation for the actual Gaussian doping profile in the channel of the device.

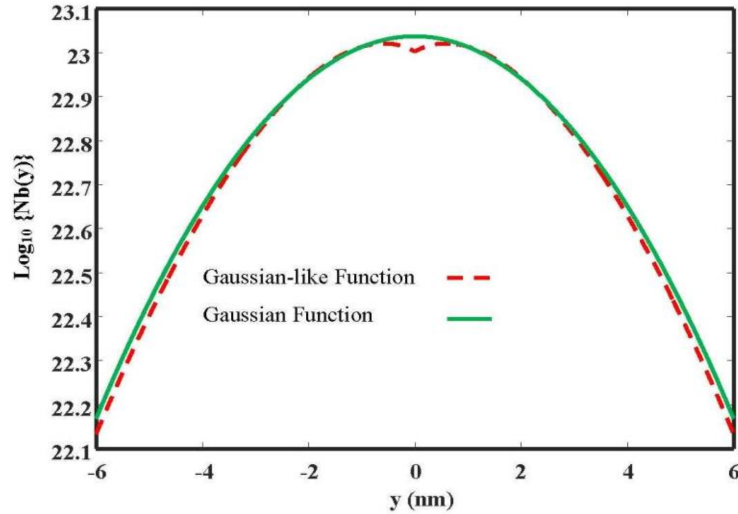

Fig. 1.4: Actual Gaussian function versus Gaussian-like function for $N_p = 1\times10^{17}\,cm^{-3}$, $R_p = 0$ and $\sigma_p = 3nm$ [Dasgupta *et al.* (1986)].

1.3.3 Strained-Si (s-Si) Channel Engineering in MOS Transistors

Strained Si (s-Si) channel engineering is used to enhance the speed of operation of the MOS transistors by enhancing the mobility of the channel carriers of the device. Welser *et al.* [Welser *et al.* (1992)] has fabricated N- and P-channel MOSFETs using the s-Si channel on a relaxed $Si_{1-x}Ge_x$ layer. The mobility of electron in the channel of such MOS devices is achieved due to the strain-induced band splitting. Vogelsang and Hofmann [Vogelsang and Hofmann (1993)] have reported significant improvements in electron drift velocities due to enhancement in the mobility of the electrons. Rim *et al.* [Rim *et al.* (2003a)] have fabricated the strained Si MOSFET compatible with CMOS technology. They [Rim *et al.* (2003a)] have observed significant increase in the drain current due to the increase in the electron mobility in the channel. They [Rim *et al.* (2003a)] have demonstrated that the Si channel grown on the relaxed SiGe layer creates a biaxial tensile strain in the Si layer due to the lattice mismatching between Si and SiGe. The amount of strain in Si is approximately 4.2*x*% where *x* is the Ge mole fraction in the SiGe layer [Rim *et al.* (2003a)]. In another work, Rim *et al.* [Rim *et al.*

(2003b)] have fabricated the s-Si directly-on-Insulator (SSDOI) MOSFETs by transferring the tensile-strained Si layer directly on the insulator substrate. The tensile strain lifts the 6-fold degeneracy in the Δ ellipsoidal valleys in the conduction band of the silicon and the degeneracy between the heavy and light hole bands in the valence band. This results in the suppression of the inter-valley/band scattering which, in turn, enhances the mobilities of electrons and holes in s-Si channel by reducing the effective transport masses of the channel carriers [Rim *et al.* (2003b)].

1.3.3.1 Classification of Strains in MOS Technology

In order to obtain the desired strain characteristics in the channel of MOS transistors, three approaches namely "Global", "Local" and "Mechanical" are used [Maiti *et al.* (2001)]. Local and global techniques of generating strain give rise to uniaxial and biaxial strain respectively. The idea of using mechanical strain to boost MOSFET performance came out very early. Most of the researchers use the generation of biaxial and uniaxial strain technology in the MOS devices by growing the Si channel on the SiGe substrate.

The local strain is a process-induced uniaxial strain created only in the longitudinal direction. High-stress capping layers are deposited on MOSFETs to introduce/induce this unidirectional local strain/stress into the channel [Shimizu *et al.* (2001), Ito et al. (2000), Thompson *et al.* (2006)]. Mahato *et al.* presented a simulation study to understand the strain distribution in the source/drain regions of strain-engineered MOSFETs by incorporating SiC, SiGe, and SiGeC films as stressors. The SiC stressors are found to produce tensile strain in the channel (suitable for n-MOSFETs) while SiGe and SiGeC stressors are observed to produce the compressive strain (suitable for p-MOSFETs) [Mahato *et al.* (2006)]. However, the uniaxial strain is better in many ways than biaxial strain:

(i) The uniaxial stress provides significantly larger holes mobility enhancement at low strain than the biaxial strain. Further, it creates higher vertical electric field in the channel due to the differences in the warping of the valence band under strain [Thompson *et al.* (2004a), Thompson *et al.* (2004b)]. Large mobility enhancement at low strain is important since the high strain is generally not used to avoid yield loss via dislocations.

(ii) The uniaxial (as compared to biaxial) stress enhanced mobility provides larger drive current improvement for nanoscale short-channel MOS devices [Shimizu *et al.* (2001), Ito et al. (2000), Thompson *et al.* (2006)].

(iii) The process-induced uniaxial stress causes approximately five times smaller n-channel threshold voltage shift. However, the performance of the uniaxially strained device is not well predictable due to its strong dependence on the device geometry [Gamiz *et al.* (2002)].

The biaxial global strain is created in the thin Si channel by growing the channel on the relaxed silicon–germanium (SiGe) substrates [Manasevit *et al.* (1982), People *et al.* (1984)] [Ungersboeck *et al.* (2006)]. The approach depends largely on materials engineering rather than the device design engineering [Cressler (2007)].

1.3.3.2 Global Biaxial Strain in Silicon Channel

As discussed earlier, the global approach to generate the biaxial strain in the silicon is to grow a thin Si film on the silicon-germanium ($Si_{1-x}Ge_x$) substrate [Manasevit *et al.* (1982), People *et al.* (1984), Barraud *et al.* (2005)], where x is the mole fraction of Ge in SiGe compound. The mole fraction x can be varied to vary the level of strain in the Si film. The silicon germanium lattice is much more spread out than just pure silicon. When the new layer of silicon is deposited on the top of the SiGe layer, the pure silicon

lattice tries to get aligned with the relaxed SiGe. In this process, the silicon lattice also "stretches out" or, as they term it, becomes "strained" as shown in Fig. 1.5 [Mahato *et al.* (2006)]. Electrons or holes move faster in the strained silicon layer. It is reported that electrons flow in the s-Si is 70% faster than that in the non-strained silicon channel [Kuchipudi and Mahmoodi (2007)] and the the ICs designed using s-Si channel MOSFETs can be made 35% faster than the conventional ICs designed with conventional MOSFETs [Kuchipudi and Mahmoodi (2007)].

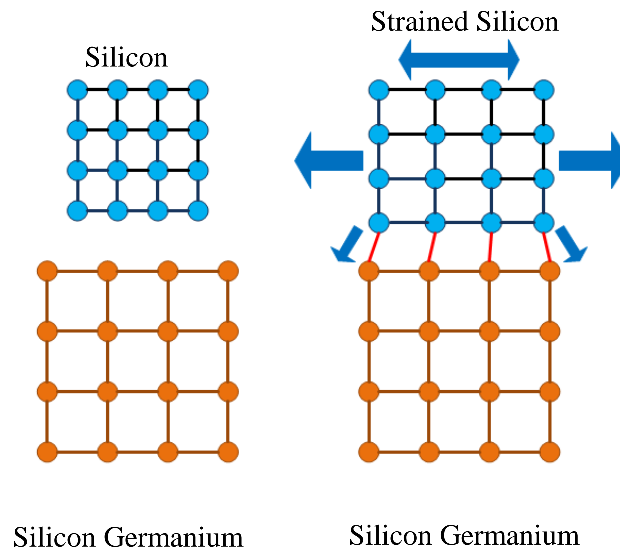

Fig. 1.5: Strained silicon layer process [Ong (2010)]

The amount of strain (ε) induced in Si layer can be defined in terms of the lattice constant of Si (a_{s-Si}) and SiGe layer (a_{SiGe}) as

$$\varepsilon = \frac{a_{s-Si}}{a_{SiGe}} - 1, \tag{1.3}$$

where, $a_{SiGe} = (1-x)a_{Si} + xa_{Ge}$ (1.4)

From the above equation, it is clear that the strain in Si layer is proportional to the Ge mole fraction (x) in SiGe layer [Maiti *et al.* (2001)].

It may be mentioned that the s-Si layer created on the SiGe layer can be transferred on other substrates for using as the channel of a double-gate MOSFET as reported by Rim

et al. [Rim *et al.* (2003b)]. In this method, a thin Si layer is first grown on a relaxed $Si_{(1-x)}Ge_{(x)}$ buffer layer grown on an SOI substrate to introduce the biaxial tensile strain in the Si layer. It is finally transferred to the top of buried oxide layer of the SOI substrate by removing the $Si_{(1-x)}Ge_{(x)}$ layer by selective etching. As a result, the strain in the Si layer becomes a function of x (i.e. Ge mole fraction) of the relaxed $Si_{(1-x)}Ge_{(x)}$ in the similar manner as observed in the s-Si layer directly grown on the relaxed $Si_{(1-x)}Ge_{(x)}$ layer [Langdo *et al.* (2003), Langdo *et al.* (2004)]. Drake *et al.* [Drake *et al.* (2003)].

1.3.3.3 Effects of Biaxial Strain on Silicon Band Structure

The strain in the silicon material is a form of piezoelectric effect which is a well-known phenomenon first reported by Smith [Smith (1954)]. The uniaxial tension may cause a change of resistivity in silicon and the complete tensor piezoresistance can be expressed in terms of the pressure coefficient of resistivity and two simple shear coefficients [Smith (1954)]. It is also reported that the mobility for the n-type Si is increased when a tensile strain is applied in the direction of the flow of carriers in the Si material [Zhao (2006)]. In particular, the biaxial strain may result in destroying the degeneracy of conduction and valence bands through band splitting of Si under the influence of biaxial tensile strain. The conduction band of Si has the 6-fold degeneracy which splits into 2-fold (Δ_2) and 4-fold (Δ_4) degenerate valleys when it is grown on the relaxed SiGe layer [Roldan and Gamiz (2004)]. Similar splitting is observed between the bands of light and heavy holes in the valence band of the Si. The in-plane Δ_2 valley shifts down to a lower energy level, whereas out-of-plane Δ_4 valley shifts up to a high energy level [Smith (1954)]. This amount of shifting in valleys in the energy scale is proportional to the strain in Si or Ge mole fraction in SiGe strain template layer [Gamiz *et al.* (2002)]. The band with lower energy is preferentially occupied by carriers which results in the

reduction of the carriers' effective mass and inter-valley scattering rates [Roldan and Gamiz (2004)]. The band splitting has been demonstrated in Fig. 1.6 and 1.7.

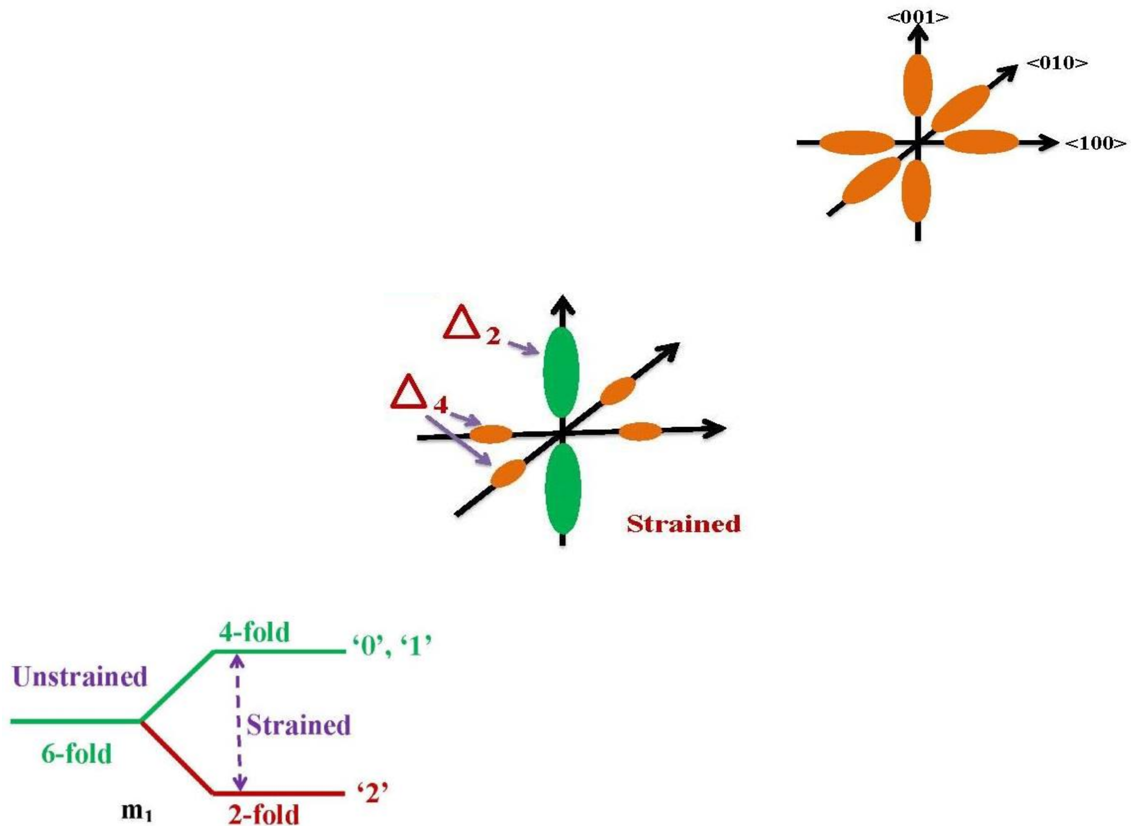

Fig. 1.6: Change in band structure of Si due to strain [Internet resource (IR2)]

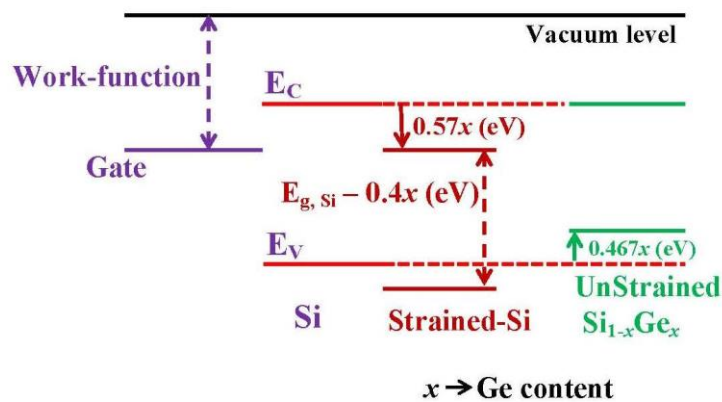

Fig. 1.7: Strain induced shift in conduction and valence bands [Numata *et al.* (2005)]

It may be mentioned that the scattering time, and energy relaxation time are increased while the channel resistance is reduced with the increase in strain in Si channel [Takagi

(2007)]. Further, the conductivity effective mass (m_C^*) is also reduced due to the reduction in the carriers' population in the Δ_4 valley [Takagi (2007)]. The effect of strain on Si band structure can be modeled as [Zhang and Fossum (2005), Numata *et al.* (2005)]:

$$(\Delta E_C)_{s-Si} = 0.57x \tag{1.5}$$

$$(\Delta E_g)_{s-Si} = 0.40x \tag{1.6}$$

$$V_T \log\left(\frac{N_{v,Si}}{N_{v,s-Si}}\right) = V_T \log\left(\frac{m_{h,Si}^*}{m_{h,s-Si}^*}\right) \approx 0.075x \tag{1.7}$$

$$(\Delta V_{bi})_{s-Si} = \frac{-(\Delta E_g)_{s-Si}}{q} - V_T \ln\frac{N_{V,Si}}{N_{V,s-Si}} \tag{1.8}$$

where, x is the Ge mole fraction in the $Si_{1-x}Ge_x$ substrate; $(\Delta E_C)_{s-Si}$ is the increase in electron affinity of silicon due to strain; $(\Delta E_g)_{s-Si}$ is the decrease in the band gap of silicon due to strain; V_T is the thermal voltage; m_h^* is the hole effective mass; $(\Delta V_{bi})_{s-Si}$ is the change in built-in voltage; $N_{v,Si}$ and $N_{v,s-Si}$ are the density of states in the valance band in normal and strained silicon, respectively and q is the electronic charge.

The energy band parameters for $Si_{1-x}Ge_x$ substrate have been estimated as follows [Zhang and Fossum (2005), Numata *et al.* (2005)]:

$$(\Delta E_g)_{SiGe} = 0.467x \tag{1.9}$$

$$N_{vSiGe} = (0.6x + 1.04(1-x)) \times 10^{19}\, cm^{-3} \tag{1.10}$$

$$\varepsilon_{SiGe} = 11.8 + 4.2x \tag{1.11}$$

where, $(\Delta E_g)_{SiGe}$ is the decrease in the band gap of $Si_{1-x}Ge_x$; $N_{v,SiGe}$ is the density of states in the valance band of the relaxed $Si_{1-x}Ge_x$ film and ε_{SiGe} is the permittivity of the $Si_{1-x}Ge_x$.

1.4 Review of Some State-of-the-Art Research Works on Channel Engineered DG MOSFETs

We have already mentioned that the characteristics of the MOS transistors can be optimized by using a graded channel and strained silicon (s-Si) channel in the device. In this section, we will briefly review of some state-of-the-art researches in the area of the channel engineered MOS transistors as discussed below.

1.4.1 Review of Some Laterally Asymmetric or Graded Channel MOS Structures

The idea of a graded-channel device was first introduced by DeMassa and Goddard in 1971 [DeMassa and Goddard (1971)] and DeMassa and Catalano in 1973 [DeMassa and Catalano (1973)] as already explained earlier. They observed that by using higher doping near the source than the drain end, the high frequency performance of several field-effect devices was found to be improved without reducing the gate lengths of the device. In 1978, Williams and Shaw [Williams and Shaw (1978)] reported the improved linearity and noise figure of the FET using a graded-channel in the device. In 1996, Agrawal *et al.* [Agrawal *et al.* (1996)] and Gwoziecki *et al.* [Gwoziecki *et al.* (1999)] have proposed a simple laterally asymmetric channel doping profile i. e. retrograde channel doping in the channel and observed minimized short-channel-effects (SCEs). Yu *et al.* [Yu *et al.* (1997)] have reported reduced short-channel effects with improved device performance lightly doped drain (LDD) MOSFET structures with a lateral channel-engineering in the form of a pocket or halo implant. The MOS devices with vertically and laterally nonuniform super-halo doping profiles are reported to be effective controlling the SCEs in sub 50 nm channel length regime [Taur and Nowak (1997)].

Pavanello *et al.* [Pavanello *et al.* (2000a)] demonstrated that the graded-channel MOS devices have reduced parasitic bipolar effects with improved breakdown voltage and hence reduced impact ionization in the high electric field region of the device. They [Pavanello *et al.* (2000b)] have also compared the performances of the single-transistor operational transconductance amplifiers (OTAs) implemented using graded-channel (GC) MOSFETs and conventional (uniform channel doping) SOI NMOSFETs. They have reported that GC MOSFET based OTA has resulted in much higher gain-bandwidth product with improved unity-gain frequency and DC gain than the OTA implemented using uniformly doped SOI MOSFETs.

Akturk *et al.* [Akturk *et al.* (2001)] have reported that the use of highly doped halo implant around either the source or drain doping in the channel can improve DC and transient performance of the device in deep submicron region.

Chen *et al.* [Chen *et al.* (2002)] experimentally investigated the performance of the asymmetric channel doping based NMOSFETs by using the conventional single-step ion implantation to form the graded doping profile in the channel. They have observed the reduction in the DIBL and subthreshold current when a higher doping near the source than the drain is maintained. They have also observed the improved hot-carrier reliability due to the suppressed longitudinal electric field near the drain in such MOS structures.

In 2003 Din *et al.* [Din *et al.* (2003)] observed improved threshold voltage roll-off, excellent dc output characteristics, improved ac transconductance and lower DIBL by using the halo doping in the MOS transistors.

Narasimhulu *et al.* [Narasimhulu *et al.* (2003)] have compared the analog performance of the scaled lateral asymmetric channel (LAC) MOSFETs with that of the conventional MOSFETs for mixed-signal applications. They [Narasimhulu *et al.* (2003)] have

observed improvements in the device gain and drive current for analog applications of the LAC MOSFETs with gate lengths down to the 70nm.

Based on simulation based study of the single halo doped DG SOI MOSFETs, Reddy and Kumar [Reddy and Kumar (2004)] have reported the reduction in the DIBL and threshold voltage roll-off of the device. For the first time, they reported the existence of a step function in the surface potential due to the presence of the single halo on the source side. This step function is observed to reduce the DIBL by screening the source side of the structure from the drain voltage variations.

The modeling, simulation and experimental studies of the laterally asymmetric channel (i.e. the graded channel (GC)) DG SOI MOSFETs have been carried out by Kranti *et al.* [Kranti *et al.* (2004)]. They have observed high values of the saturation drain current, intrinsic DC gain of 70–80 dB for L_{eff}=1.64 μm and exceptionally high values of the Early voltage (>1600 V).

Mohapatra *et al.* [Mohapatra *et al.* (2005)] have investigated the performance reliability issues of laterally diffused MOS (LDMOS) transistors for a uniform as well as single halo doped MOS structures. They have reported better reliability with better DC and high frequency performance of the single halo doped LDMOS transistors than LDMOS with a uniformly doped channel.

Kumar *et al.* [Kumar *et al.* (2005)] have investigated the short channel performance of a single halo doped channel MOSFETs. They have observed superior performance over the conventional MOS devices for gate lengths in the sub-100-nm regime. They have also demonstrated that the OPAMP layout with conventional MOS devices will require more chip area than that designed with the laterally asymmetric channel (LAC) MOS devices.

Cerdeira *et al.* [Cerdeira *et al.* (2005)] have compared the quasi-linear current–voltage characteristics of the conventional and graded-channel (GC) fully depleted SOI MOSFETs. They have observed a decrease in the on-resistance of the GC SOI MOSFETs with the increase in the length of the low doped region in the channel. An improvement in the third-order harmonic distortion in the GC MOSFETs over the uniformly doped channel MOSFETs has also been reported by Cerdeira *et al.* [Cerdeira *et al.* (2005)].

Through a simulation study, Ma and Kaya [Ma and Kaya (2005)] have investigated the RF performance of the GC SOI MOSFETs. They have compared the intrinsic gain, cut-off frequency, distortion/linearity and gm/Id performance parameters of the GC SOI MOSFETs for different channel geometries and doping considerations.

Chauhan *et al.* [Chauhan *et al.* (2006)] have developed a new charge-based analytical compact model for the lateral non-uniformly doped MOSFET and investigated the impact of the lateral doping gradient in the intrinsic MOS on the high voltage operations of the MOSFETs.

Mudanai *et al.* [Mudanai *et al.* (2006)] have developed an analytical derivation of the output resistance of the laterally nonuniformly doped MOSFETs with halo implants. They have assumed the complete channel as two uniformly doped transistors connected in series for their analysis. The model has assumed the lower doped region at the source side and the higher doped halo transistor at the drain side.

For the first time, Chakraborty *et al.* [Chakraborty *et al.* (2007)] carried out a simulation study to show the effects of double-halo and single-halo doping on the subthreshold analog performance of 100nm CMOS devices. Results show that the CMOS amplifiers made with the halo implanted MOS devices have higher voltage gain over the amplifiers designed with the conventional MOSFETs. An improvement of more than

100% in the voltage gain can be achieved when LAC doping is used in both of the p- and n-channel MOS devices in the CMOS circuits used for designing the amplifiers.

Kaur *et al.* in 2007 [Kaur *et al.* (2007a)] have theoretically investigated the influence of graded channel on cylindrical/surrounding gate MOSFETs. They have reported the two-dimensional (2D) analytical models for the surface potential, electric field, threshold voltage and subthreshold swing of the device obtained by solving the 2D Poisson's equation in cylindrical coordinate systems. They [Kaur *et al.* (2007a)] have shown that the introduction of a step doping profile in the channel can lead to the suppression of the SCEs and reduction in the peak electric field at the drain end which can be explored for reducing the impact ionization and HCEs of the device. In another work, Kaur *et al.* [Kaur *et al.* (2007b)] have modelled the drain current, transconductance and drain conductance of the graded channel cylindrical/surrounding gate MOSFETs. Kaur *et al.* [Kaur *et al.* (2008)] have also studied the effect of gate engineering (asymmetric gate stack) on the graded channel cylindrical gate MOSFETs. They [Kaur *et al.* (2008)] have reported that the combination of gate engineering (asymmetric gate stack) and channel engineering (graded channel) in the MOS structure can improve the carrier transport efficiency by increasing the average electric field in the channel while suppressing both the SCEs and HCEs.

A new design approach for CMOS device using channel engineered MOSFETs has been proposed by Lim *et al.* [Lim *et al.* (2008)] for improving the high frequency noise performance over the conventional CMOS technology. The intrinsic noise correlation coefficient of ~0.4 or lower of the conventional CMOS can be enhanced to as high as ~0.9 which improves the noise performance of the device. By using the conformal mapping transformation approach, Sharma *et al.* [Sharma *et al.* (2008a)] have demonstrated through simulation and theoretical analysis that the use a graded channel

in the MOSFETs can reduce the gate misalignment effect in the DG MOS structures. In another study, Sharma *et al.* [Sharma *et al.* (2008b)] have used ATLAS 3D device simulator to analyse the capacitive behavior and hence the cut-off frequency of the graded channel MOS devices. Danneville *et al.* [Danneville *et al.* (2008)] have reported that the microwave noise performance of the Si MOSFETs can be improved by replacing the uniform doping by a laterally asymmetric channel doping. Through RF measurements, Emam *et al.* [Emam *et al.* (2009a)] have shown significant reduction in the noise figure of the graded-channel MOS transistors over the classical MOSFET transistors. Emam *et al.* [Emam *et al.* (2009b)] have demonstrated the superior performance of graded channel (GC) MOSFET over classical MOSFET in the nanoscale regime. They have also shown that the effects of scaling on the dc and analog performances of the GC MOS devices are smaller than their conventional counterparts. Further, the GC MOSFETs have better high temperature and high frequency performances over the uniformly doped MOS devices. Rengel *et al.* [Rengel *et al.* (2009)] have reported a simulation based comparative study of the static and high-frequency performances of the LAC MOSFETs and conventional MOS devices. They have shown that the GC MOS devices have higher transconductance, higher cut-off frequency, and better values for the main noise circuital figures of merit than those of the conventional uniformly doped MOSFETs. Chen *et al.* [Chen *et al.* (2009)] have investigated the linearity behavior of the RF power output of the laterally diffused (LD) MOS devices with graded channel doping profiles. They have reported that a third-order intermodulation distortion can be achieved by controlling the parameters of the lateral channel doping.

Abdi *et al.* [Abdi *et al.* (2009)] have reported a 2D analytical threshold voltage model of the graded channel stacked-gate DG MOSFET to suppress the SCEs and improve the

subthreshold performances. Mohankumar *et al.* [Mohankumar *et al.* (2010)] have investigated the combined effects of the halo doping profile in the channel and dual-metal gate (DMG) on the analog and RF performances of DG MOSFETs. As compared to the single-metal gate (SMG) DG MOSFETs with a uniformly doped channel, they [Mohankumar *et al.* (2010)] have reported an increase in the gain by 45% and 35% in the gate engineered (i.e. with a DMG) and channel engineered (i.e. with a GC doping) MOS devices respectively.

Emam *et al.* [Emam *et al.* (2010)] have reported a fabrication process for the graded channel MOS devices by using the fully-depleted 0.15 μm SOI CMOS technology to improve the RF noise performance of the device gate length in the deep submicron regime.

Kaur *et al.* [Kaur *et al.* (2010)] have reported an analytical model for the channel potential, threshold voltage and electric field of a laterally asymmetric channel gate stack (LACGAS) surrounding gate MOSFET by using parabolic approximation method for solving the Poisson's equation in the cylindrical coordinate system. They have reported that their proposed structure suppresses SCEs significantly while enhancing the carrier transport efficiency due to the gate stack architecture. Further, the LACGAS structure have better current drivability and transconductance characteristics as compared to the conventional and laterally asymmetric channel (LAC) MOS devices.

Based on the Monte Carlo simulation, Martín *et al.* [Martín *et al.* (2011)] investigated the electrical characteristics of the Graded Channel (GC) Silicon-On-Insulator (GCSOI) MOSFETs. They have analysed the influence of the length of the lightly-doped (LLD) region of the channel on the microscopic transport properties of the device. The have concluded that there exists an optimum LLD value for different GC doping techniques

which may determine the maximum improvements in performance parameters of the GC MOSFETs over the uniformly doped MOS devices.

Islam and Khan [Islam and Khan (2009)] have reported a surface potential model for a pocket implanted asymmetric n-channel MOSFET by assuming the continuity of potential function and electric field in the lateral direction of the device. They have also investigated the dependence of the surface potential on different device parameters and biasing conditions of the device.

Panigrahy and Sahu [Panigrahy and Sahu (2013)] have reported the superiority of the graded channel MOSFET over the conventional DG MOSFET in terms of different electrical parameters such as the threshold voltage, DIBL etc. Recently, Chattopadhyay *et al.* [Chattopadhyay *et al.* (2016)] have investigated the performance analysis of the graded channel DG MOSFETs with gate stack architectures. Swain et al. [Swain *et al.* (2016)] have reported the performance optimization of the graded channel gate stack DG MOSFETs with different high-*k* materials as gate oxides.

The above literature survey thus clearly demonstrates that the graded-channel (GC) MOSFETs have superior capability of suppressing the SCEs and HCEs as compared to the conventional uniformly doped MOSFETs. Further, the GC MOSFETs have better RF and analog performance characteristics over the uniformly doped MOS devices

1.4.2 Review of Some Strained-Silicon Channel MOSFETs

After reviewing some important literature on the channel doping engineering in the above subsection, we will now survey on some important state-of-the-art research related to the strain-engineered silicon channel based MOS transistors. The fabrication of both the n- and p-channel MOSFETs with a strained-Si (s-Si) channel was reported first time by Wesler *et al.* [Wesler *et al.* (1992)]. They used buried strained-Si and

surface strained-Si layers to demonstrate the enhanced electron mobility in both types of strained-Si MOS devices. Nayak *et al.* [Nayak *et al.* (1993)] has reported the fabrication of p-channel enhancement mode MOSFET on a biaxially strained Si layer. They have observed a 50% increase in the mobility of channel carriers in the strained Si P-MOSFET with respect to the channel carrier mobility of an identically processed conventional Si P-MOSFET. Rim *et al.* [Rim *et al.* (1995)] has experimentally investigated the performance of a p-MOSFET with a surface strained-silicon channel fabricated on the relaxed $Si_{1-x}Ge_x$ layer. They have observed enhancement of both the hole mobility and drive current almost linearly with Ge mole fraction in the relaxed $Si_{1-x}Ge_x$. They [Rim *et al.* (1998)] have also shown an improved transconductance in the strained-Si N-MOSFETs even in the case high channel doping and high vertical effective fields in the channel. Mizuno *et al.* [Mizuno *et al.* (1999)] [Mizuno *et al.* (2000)] have studied the performance of the strained-Si p-MOSFETs on a strained-Si/SiGe-on-Insulator substrate (SSGOI). They have reported a higher hole mobility in the p-channel SSGOI MOS devices. The enhancement in the mobilities of electrons and holes with the strain in the strained-Si n-and p- channel MOSFETs on SiGe virtual substrates has been reported by Currie *et al.* [Currie *et al.* (2001)]. With respect to conventional MOSFETs, they have observed the increase in the mobilities of the electrons and holes up to 1.8 and 1.6 times in the n- and p-channel devices respectively. Based on the experimental data, Wang *et al.* [Wang *et al.* (2007)] have shown a trade-off between the control of SCEs and enhanced mobility in the strained-Si MOS structures.

After the experimental demonstration of the strained-Si channel based MOS devices by Wesler *et al.* [Wesler *et al.* (1992)], a number of theoretical and analytical studies on the strained-Si MOSFETs have also been reported in the literatures by many researchers.

Oberhuber *et al.* [Oberhuber *et al.* (1998)] have theoretically investigated the hole mobility as a function of strain in the p-channel MOSFETs with a strained-Si on a relaxed SiGe substrate. Nayfeh *et al.* [Nayfeh *et al.* (2004)] have developed a physics based analytic model for the threshold voltage of the long-channel strained-Si $Si_{1-x}Ge_x$ N-MOSFETs. They [Nayfeh *et al.* (2004)] have observed that the threshold voltage difference between the strained- and unstrained-Si channel devices is increased with the channel doping. Bufler *et al*. [Bufler *et al*. (2004)] have observed the on-state current of the strained-Si single-gate (SG) MOSFETs nearly same as that of the unstrained-Si channel based double-gate (DG) MOSFETs with a gate length of 25 nm in both the devices. Chandrasekaran *et al.* [Chandrasekaran *et al.* (2005)] have developed a unified model valid for the accumulation, depletion and strong inversion regime of operations of the strained-Si MOSFETs. Zhang *et al.* [Zhang *et al.* (2005)] have presented an improved threshold voltage model for the strained-Si-$Si_{1-x}Ge_x$ MOSFETs. A simulation based study has been reported by Numata *et al.* [Numata *et al.* (2005)] for showing the improved control of the threshold voltage and SCEs in the ultrathin strained-SOI MOSFETs beyond 100-nm regime. In another work, Numata *et al.* [Numata *et al.* (2006)] have studied the 35-nm gate-length based strained-SOI MOSFETs on SiGe-on-insulator (SGOI) substrates. They have successfully employed the back-gate bias to control current drive in the device.

Kumar *et al.* [Kumar *et al.* (2006)] have developed an analytical model for the threshold voltage of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs. Zainuddin *et al.* [Zainuddin *et al.* (2007)] have proposed a semi-analytical model for the electrostatic properties of the strained-Si on relaxed SiGe layer NMOS devices. The model has explicitly incorporated the discontinuity of the dielectric constant across the strained-Si/SiGe interface. Both Kumar *et al.* [Kumar *et al.* (2007)] and Venkataraman

et al. [Venkataraman *et al.* (2007)] have first theoretically investigated the impacts of strain or Ge content on the threshold voltage of nanoscale strained-Si/SiGe MOSFETs. Using the Non-Equilibrium Green's Functions (NEGF) simulation technique, Kalna *et al.* [Kalna *et al.* (2008)] have investigated the effect of biaxial strain on the performance of the short-channel DG MOSFETs. Wang *et al.* in 2009 [Wang *et al.* (2009)] have used a 3D TCAD simulation tool to invetsigate performance characteristics of the strained Si CMOS devices with silicon-based alloy stressors and stressed contact etching stop layer (CESL). They have observed that the drive current in the strained-Si NMOS is dominated by the tensile stress along the transport direction while it is dominated by the compressive stress along the growth direction in larger width strained-Si NMOS devices.

Jin *et al.* [Jin *et al.* (2010a)] have developed a two-dimensional analytical model for the surface potential for fully depleted dual-material gate (DMG) strained-Si-on-insulator (SSOI) MOSFETs. They have investigated the impact of different values of work functions, channel length, the drain bias voltage and Ge mole fraction in the relaxed SiGe buffer on their proposed device characteristics. They have observed the reduction in the SCEs, HCEs and DIBL due to the enhanced carrier transport efficiency in their proposed device [Jin *et al.* (2010a)]. The major observation includes the existence of a step in the surface potential profile which is demonstrated to be responsible for the suppression of SCE, HCE and DIBL. In an another work, Jin *et al* [Jin *et al.* (2010b)] has reported the 2D modeling of the surface potential, threshold voltage, subthreshold current (SC) and subthreshold swing (SS) for gate stack symmetrical double-gate (DG) s-Si MOSFETs.

Shan *et al.* [Shan *et al.* (2010)] have developed analytical expressions for the threshold voltage of a dual-channel (one of which is a buried strained-Si channel and the other is a

surface strained-Si channel) strained p-type Si/strained $Si_{1-x}Ge_x$/relaxed $Si_{1-y}Ge_y$ (s-Si/s-SiGe/$Si_{1-y}Ge_y$) P-MOSFET. Since the hole mobility in the buried channel is higher than that in the surface channel, they have assumed that the strong inversion appears earlier in the buried channel due to compressive strained SiGe than that in the surface channel due to tensile strain. The variations of the threshold voltage due to the changes in Ge mole fraction, s-Si layer thickness, and doping concentration in the channel have been analysed in details by them [Shan *et al.* (2010)].

Xia *et al*. [Xia *et al*. (2011)], for the first time, have investigated the impact of strain on the surface potential and threshold voltage characteristics of a double-gate (DG) fully depleted MOSFET. They have reported some basic guidelines for improving the immunities against the SCEs and DIBL of the nano-scaled CMOS-based devices through the strain in the Si channel of the MOS devices.

Kumar *et al*. [Kumar *et al*. (2013a)] have reported the influence of strain in the channel on the subthreshold characteristics of the s-Si on SGOI MOSFETs for different gate lengths. They have observed that the SS is increased by 14.73% for 30 nm gate length, 2.94% for 50nm gate lengths and 0.8% for 70 nm gate lengths when the Ge mole fraction is increased from 0 to 0.3. In an another work, Kumar *et al.* [Kumar *et al.* (2013b)] have developed analytical models for the threshold voltage of double-material-gate (DMG) strained-Si (s-Si) on Silicon-Germanium-on-Insulator (SGOI) MOSFETs. The threshold voltage model has been developed by using the "virtual cathode" concept [Dubey *et al.* (2010a)]. The effects of various device parameters like Ge mole fraction, Si film thickness, SiGe thickness and gate-length ratio on the threshold voltage of the device have been demonstrated. They have theoretically demonstrated that the threshold voltage and DIBL can be controlled by changing the gate length ratios and Ge mole fraction in the device. Kumar *et al.* [Kumar *et al.* (2013c)] have also proposed the

surface potential based 2D analytical models of the SC and SS of nanoscale DMG strained-Si (s-Si) on Silicon-Germanium-on-Insulator (SGOI) MOSFETs. The effects of various device parameters such as the Ge mole fraction, Si film thickness, gate-length ratio and various combinations of control/screen gate work-functions on the SC and SS have also been discussed.

Rawat *et al.* [Rawat *et al.* (2014a)] have purposed an analytical surface potential based threshold voltage model of ion-implanted fully-depleted short-channel strained-Si-on-Insulator (SSOI) MOSFETs using parabolic approximation method. The threshold voltage is expressed as a function of the device dimensions as well as doping profile parameters (e.g. straggle, projected range and peak doping concentration). Rawat *et al.* [Rawat *et al.* (2014b)] have also reported the analytical modeling of SC and SS of short channel fully-depleted strained-Si-on-insulator (SSOI) MOSFETs with a vertical Gaussian-like doping profile in the channel. The effects of strain in the channel and various other device parameters on the subthreshold characteristics have been analysed by them [Rawat *et al.* (2014a)] [Rawat *et al.* (2014b)].

1.4.3 Summary of the Literature Review: Motivation behind the Present Thesis

After reviewing of some important state-of-the-art research works related to the modeling and simulation of MOSFET structures with laterally asymmetric channel profile (specifically graded channel profile) and MOSFET structures with strained-silicon channel in above sections, we will summarize some observations of the literature survey as outlined in the following.

- As compared to the conventional uniformly doped MOS devices, the graded channel MOS devices [Chen *et al.* (2002), Ma and Kaya (2005), Kaur *et al.* (2007a), Kaur *et al.* (2007b), Sharma *et al.* (2008a), Rengel *et al.* (2009),

Panigrahy and Sahu (2013)] have better hot carrier reliability due to the suppressed longitudinal electric field near the drain. Further, the graded-channel MOSFETs have higher transconductance [Kaur *et al.* (2007b)], improved cut-off frequency [DeMassa and Catalano (1973), Malhi and Salama (1980)], and improved subthreshold characteristics [Kaur *et al.* (2007a), Kaur *et al.* (2008)] over the conventional MOSFETs. Moreover, the introduction of graded channel may reduce the gate misalignment effect on the device characteristics of the DG MOS structures [Sharma *et al.* (2008a)].

- A number of theoretical models [Kranti *et al.* (2004)], Kaur *et al.* (2007a), Kaur *et al.* (2007b), Kaur *et al.* (2008), Sharma *et al.* (2008a)] have been reported for the subthreshold characteristics of graded channel MOSFET structures. However, to the best of our knowledge, no theoretical investigation has been carried out to study the effect of dual-material gate (DMG) structure on the graded channel MOSFETs.
- Strained-silicon channel MOS devices [Nayak *et al.* (1993), Rim *et al.* (1995), Rim *et al.* (1998), Kumar *et al.* (2007), Venkataraman *et al.* (2007),] have improved speed of operation, enhanced drive current, improved transconductance (and hence improved carrier transport efficiency) due to the enhanced channel carrier mobility of the device. However, the subthreshold swing is reported to be increased with the strain for decreasing gate lengths [Kumar *et al*. (2013c)].
- Strained-Si MOSFETs with a DMG structure [Jin *et al.* (2010a), Jin *et al.* (2010b), Kumar *et al.* (2013b), Kumar *et al.* (2013c)] show a step in the surface potential profile which can be explored for reducing the SCEs, HCEs and DIBL with enhanced carrier transport efficiency. The degradation in the threshold

voltage with increased strain [Kumar, and G. V. Reddy (2004)] can be improved by increasing the length of control gate for a given channel length [Kumar *et al.* (2013a), Kumar *et al.* (2013b)].

- As compared to the uniformly doped MOSFETs, the DG MOSFETs with a vertical Gaussian doping profile created by the ion-implantation method [Sze (1981), Zhang *et al.* (2008)] may provide better flexibility for controlling the subthreshold characteristics (i.e. threshold voltage, subthreshold swing, subthreshold current, DIBL etc.) [Dubey *et al.* (2010a), Dubey *et al.* (2010b) Dubey *et al.* (2011), Rawat *et al.* (2014a), Rawat *et al.* (2014b)] due to the additional two doping profile parameters namely the straggle and projected range in addition to the peak doping value of the Gaussian profile. However, the analytical modeling of the device characteristics of such devices become difficult due to the nonintegrable nature of the Gaussian function over any finite interval [Pandey *et al.* (2004), Tiwari and Jit (2010(a)), Tiwari and Jit (2010(b)), Tiwari *et al.* (2011(a))]. A vertical Gaussian-like double-integrable analytic function proposed by Dasgupta and Lahiri [Dasgupta and Lahiri (1986)] can be used for the simplicity of analytical modeling of the subthreshold characteristics of the short-channel ion-implanted MOSFETs [Dubey *et al.* (2010a), Dubey *et al.* (2011), Rawat *et al.* (2014a), Rawat *et al.* (2014b)].
- A number of models have been reported on the effects of either DMG structure or Gaussian-like channel doping on the subthreshold characteristics of the s-Si channel MOSFETs. However, to the best of our knowledge, no study has been reported for investigating the combined effects of DMG and Gaussian-like channel doping profile on the subthreshold characteristics of s-Si channel based DG MOSFETs.

Thus, there are ample opportunities for the theoretical modeling and simulation of the subthreshold characteristics of dual-material (DM) DG MOSFETs with different graded channel doping profiles (including the Gaussian profile) with and without including the effects of strain in the silicon channel of the short-channel MOS devices. Based on the above observations from the literature, the scopes of the present thesis have been outlined in the following section.

1.5 Scope of the Thesis

The basic objective of this thesis is to carry out some theoretical and simulation based investigations of the subthreshold characteristics of the two types of channel engineered dual-material (DM) double-gate (DG) MOSFETs. In the first kind of channel engineering, the channel profile has been divided into two non-overlapped regions: a high-doped region under the control gate (near the source side) and a relatively lower-doped region (than that of the source side) under the screen gate (near the drain side). In the second case, a vertical Gaussian-like doping profile for ion-implanted channel has been considered in the DM DG strained-Si MOS structures. In the first MOS device, the combined effects of the DM and graded channel (GC) on the subthreshold characteristics (i.e. surface potential, threshold voltage, subthreshold current and subthreshold swing characteristics) have been theoretically investigated while the combined effects of Gaussian channel profile engineering, the strained-channel engineering and DM engineering on the subthreshold characteristics of the short-channel MOSFETs have been investigated in the second case. The thesis consists of SIX Chapters including the present one. The contents of the remaining FIVE chapters of the thesis are outlined as follows:

Chapter-2 deals with the two-dimensional (2D) analytical modeling and ATLAS™ based TCAD simulation of the surface potential and the threshold voltage of the graded-channel dual-material double-gate (GCDMDG) MOSFETs. The surface potential model has been obtained by solving the 2D Poisson's equation using the parabolic approximation method. The surface potential has then been used to model the threshold voltage, DIBL and channel electric fields of the proposed MOS structure. The effects of different device parameters on the device characteristics have been investigated to check the figure-of-merit of the proposed GCDMDG MOS structure over the graded-channel double-gate (GCDG) and dual-material double-gate (DMDG) MOS structures. To validate the proposed model, the theoretical results have been compared with the simulation data obtained by the commercially available ATLAS™ TCAD tool.

Chapter-3 presents the modeling and ATLAS™ based simulation of the subthreshold current (SC) and subthreshold swing (SS) characteristics of the graded-channel dual-material double-gate (GCDMDG) MOSFETs considered in Chapter-2. The concept of effective conduction path in the DG MOSFETs has been explored for modeling the SS of the proposed device. The potential model developed in Chapter-2 has been directly used in this chapter for modeling the SC and SS of the device. The variations of SC and SS against different device parameters have been studied in details. The SC and SS characteristics of the GCDMDG MOS transistor have been compared with those of the DMDG and GCDG MOS structures. The results of the developed model have been compared with the ATLAS™ TCAD simulator data for the validation of the proposed models developed in this chapter.

Chapter-4 reported the analytical modeling of the surface potential and threshold voltage of ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs with vertical Gaussian-like doping function in the channel. The 2D potential

distribution function has been derived by solving the 2D Poisson's equation using the parabolic approximation method as considered in Chapter-2. The novelty of the proposed device structure lies in the amalgamation of the advantages of both the strained-Si channel and double-material double-gate MOS structures with a non-uniform vertical Gaussian-like doping profile. The effects of different device parameters (e.g. channel length, gate length ratios, germanium mole fraction etc.) and doping profile parameters (i.e. peak doping concentration, projected range, straggle parameter of the vertical Gaussian-like channel doping profile) on the potential and threshold voltage of the proposed structure have been investigated in details. The model results have been verified by comparing them with the ATLAS™ based TCAD simulation data.

Chapter-5 presents the modeling and simulation of the subthreshold current (SC) and subthreshold swing (SS) characteristics of the ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs considered in Chapter-4. The surface potential model derived in Chapter-4 and the concept of effective conduction path, have been explored for the modeling of the SS of the device. The dependence of SC and SS of the proposed device on various device parameters such as gate length ratio, Ge mole fraction, peak doping concentration, projected range, straggle parameter etc. has been studied. The model results have been verified by comparing them with the simulation data obtained by the 2D ATLAS™ simulator.

Chapter-6 includes the summary and conclusions of the thesis. The major findings of the present study are summarized in this chapter. Finally, some future scopes of research in the related areas of the present thesis have also been outlined in the last section of this chapter.