Chapter 3

3.1 Introduction

Gate dielectric insulator is one essential and primary component of thin-film transistor (TFT), which has a key role in fabricating high-performance devices.[3, 112, 113] Electrical charges of such dielectric material shift from their average equilibrium position when the gate potential is applied across the dielectric thin film, causing the dielectric polarization. This dielectric polarization can arise from different factors, including electronic polarization, ionic polarization, molecular orientation, chain relaxation or free counter ions polarization, space charges polarization, electrode, or electric double-layer (EDL) polarization.[3] For a given semiconducting material and geometrical parameter of a TFT, increasing the capacitance of the gate dielectric is an approach to achieve high saturated drain current (I_D) with lower gate voltage (V_G), which is required for reducing the operating voltage of the device.[3] Therefore, fabrication of large area and the high capacitive film is one essential requirement to develop low cost and low voltage TFT. This capacitance of the gate dielectric thin film is proportional to the dielectric constant of the material and inversely proportional to the thickness of the film. Consequently, to fabricate low voltage TFT, a number of efforts have been given either to develop new high dielectric constant (high-κ) material or to fabricate ultra-low thin film dielectric.[3, 112, 114]

High-κ dielectric are mostly inorganic oxide materials. Among them oxide insulators like Ta_2O_5[115], Y_2O_3[116], TiO_2[117, 118], ZrO_2[119, 120], HfO_x[121], $HfLaO_x$[122], $LaAlO_3$[123], silicates[124, 125], etc. have been reported for the fabrication of high-

performance TFT. For developing high-κ dielectric, both vapor phase deposition and solution-processed technique have been employed. The most commonly used vapor phase deposition methodologies for depositing high-k inorganic films include chemical vapor deposition (CVD), atomic layer deposition (ALD), sputtering, pulsed laser deposition (PLD) and e-beam evaporation (vide infra).[3, 112, 113] Although these methods produce high-quality inorganic films, these methods are time-consuming and expensive. Therefore, in order to achieve low-cost and roll-to-roll fabrication, dielectric films processed from solution precursors is a unique approach that includes different coating and printing methodologies such as spin-coating, spray coating, inkjet printing, and gravure printing.[3, 113] Recently, a number of solution-processed ion-conducting gate dielectric have been developed that show excellent performance in the race of low voltage high-performance metal oxide TFT.[126-130] The most dominating factor for dielectric polarization of these ionic gate dielectric is the 'ionic polarization,' which enables it to fabricate high capacitive thin-film even with higher film thickness.[126, 130] Until now, all of these reported ions conducting gate dielectrics are based on Li or Na ion-containing Al_2O_3 class of ceramic materials that have a large optical band gap. Since the dielectric constant of a material varies inversely with its optical band gap, further research is required to develop a lower band gap ion-conducting gate dielectric that can enable us to fabricate higher performance TFT. The Li_2O ceramics have been recently studied and used as a gate dielectric.[131] However, these ceramics are noticeably hygroscopic and react simply with CO_2.[132] On the other hand, Zinc oxide use as a multifunctional material due to its unique chemical and physical properties, and Li doped ZnO is very thermodynamically, stable, and environmentally friendly material.[133] Therefore, the Li-Zn-O system can serve as a stable dielectric of TFT fabrication.

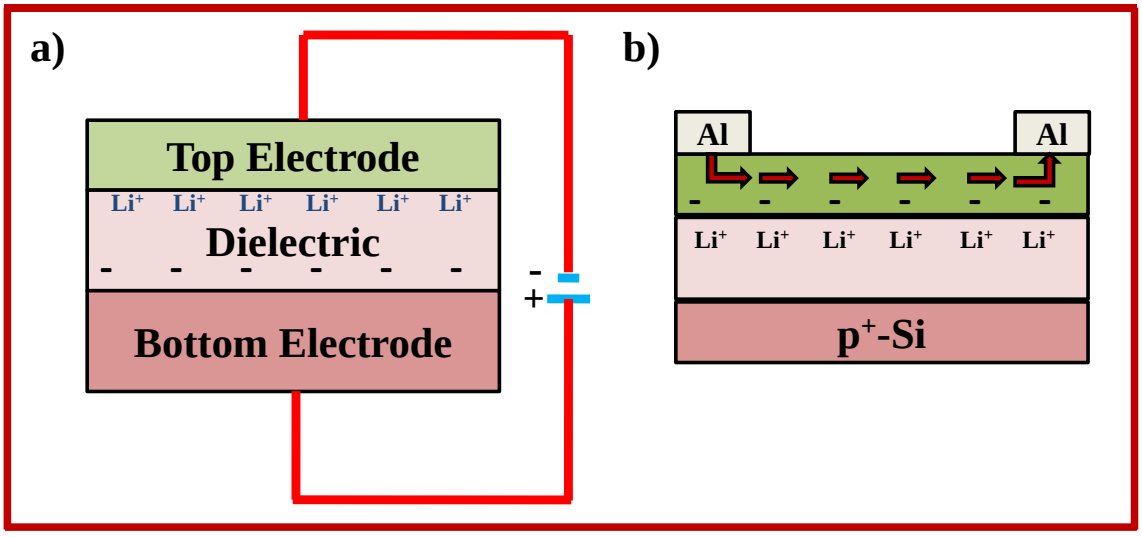

Figure 3.1: *Schematic diagram of* ***a)*** *charge polarization of the Li_2ZnO_2 ionic dielectric thin film due to Li^+ ion shift under the external bias and* ***b)*** *influence of that dielectric on the flow of electron in an active channel at low voltage.*

In this thesis chapter, I have described the synthesis method of a crystalline ionic phase lithium zincate (Li_2ZnO_2) by a sol-gel technique, which requires 500 ^oC processing temperature, and for the first time, it is successfully utilized as a gate dielectric of a metal oxide TFT. Although zinc oxide (ZnO) is the most studied metal oxide semiconductor, however crystalline Li_2ZnO_2, is an electronic insulator with an optical band gap of 3.3 eV.[134-136] Earlier Li-doped ZnO has been utilized for many applications, including higher mobility TFT semiconductor, electrodes for solar cells, field emission materials, and catalytic application.[135, 137, 138] It has been reported that the size of the unit cell of ZnO and Li/ZnO structures increases in the order: ZnO→ LiZnO→ Li_2ZnO_2 where Li^+ ions are present outside the cells, and their number is the highest in the case of Li_2ZnO_2.[139] Therefore, to achieve the optimum ionic polarization effect in the dielectric thin film, Li_2ZnO_2 has been chosen for the gate dielectric of a TFT. To realize the TFT device performance with Li_2ZnO_2 gate dielectric, two different types of devices were fabricated. One of them with Li_2ZnO_2 and the other with reference Li_2O gate dielectric, and both of

them have been synthesized by the sol-gel technique. Solution-processed tin oxide (SnO_2) has been used as a semiconductor for both devices by keeping all geometrical parameters of the TFT same. It is observed that both of these TFTs show excellent device performance at a low operating voltage ($\leq$ 2V). However, the highest carrier mobility was obtained from the TFT fabricated with the Li_2ZnO_2 dielectric. The variation in device performance between these two TFTs is very significant, which indicates the superior behavior of this new Li_2ZnO_2 gate dielectric.

3.2 Result and discussion

3.2.1 Thermal Analysis

To determine the crystallization temperature of this Li_2ZnO_2 material, thermal gravimetric analysis (TGA) and differential thermal analysis (DTA) were performed simultaneously. As mentioned earlier, the powder sample for the DTA-TGA experiment was prepared by removing the solvent of the precursor solution of Li_2ZnO_2. **Figure 3.2** shows the thermal behavior of the Li_2ZnO_2 that has been obtained with initial precursor powder materials. The experiment has been performed under the nitrogen atmosphere with a 20 ^oC/ min flowing rate. The wide weight loss was observed on the powder sample from 280 ^oC to 410 ^oC, which initially appears due to the dehydroxylation and removal of other organic impurity followed by thermal decomposition of metal hydroxide and complex ligand. A sharp exothermic DTA peak is observed at 410 ^oC, which is associated with the crystallization of sol-gel powder that forms Li_2ZnO_2. There is no significant weight loss observed in the temperature range of 450-700 ^oC. Thus the TGA and DTA analysis are in agreement with the crystallization temperature of the film.

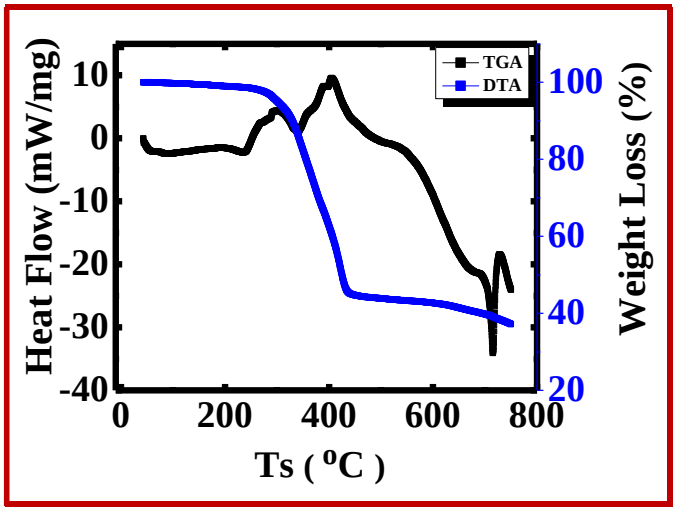

***Figure 3.2**: TGA and DTA of the precursor powder of Li_2ZnO_2.*

3.2.2 Structural Properties of the thin film and powder of Li_2ZnO_2

To confirm Li_2ZnO_2 crystal formation, the XRD study was conducted on the powder gel sample heated at 500 ^oC for two hours, and the data is shown in **figure 3.3 a)**. The data shows a clear Li_2ZnO_2 crystal formation indicating that at this temperature, lithium acetate and zinc acetate decomposes into lithium oxide (Li_2O) and zinc oxide (ZnO) respectively followed by solid-state reaction of these two individual oxides to form Li_2ZnO_2. The diffraction peaks at the 2θ angles of 33.5, 34.9, 42, and 56.7^o corresponding to the plane of reflections of (120), (112), (013), and (033) respectively corroborates the hexagonal crystal phase of Li_2ZnO_2 (JCPDS, No. 37-1160).

Grazing Incidence X-ray Diffraction (GIXRD) analysis was also performed to check the degree of crystallinity of as-deposited thin film on the glass substrate and is presented in **figure 3.3 b)**. There is no significant deviation in XRD and GIXRD data. Clear peaks from (120) and (112) reflections were observed supporting the presence of Li_2ZnO_2 thin film.

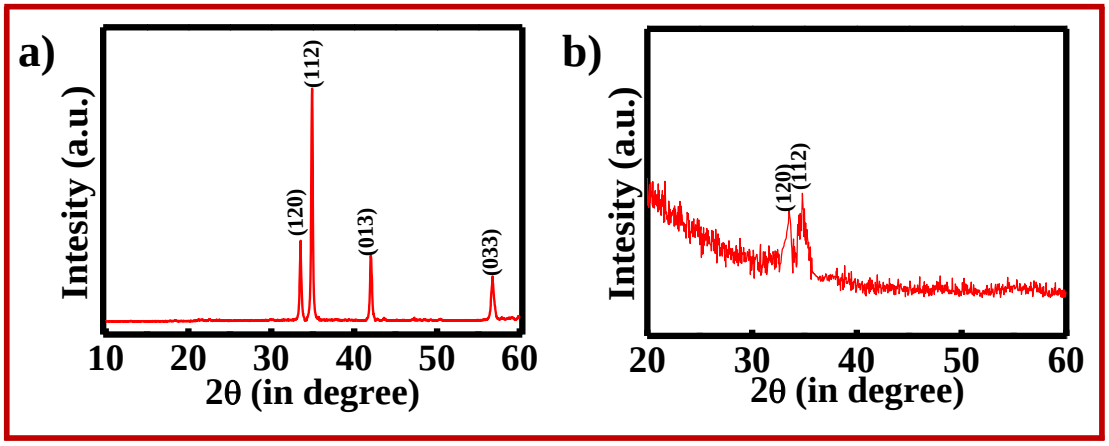

***Figure 3.3**: **a)** XRD analysis of Li_2ZnO_2 powder annealed at 500 °C and **b)** GIXRD analysis of Li_2ZnO_2 thin film annealed at 500 °C.*

XRD study of SnO_2 powder has been done to check the crystalline phase of the oxide semiconductor. The sample was prepared by heating a powder gel sample at 500 °C for one hour. **Figure 3.4 a)** shows the clear crystalline phase of SnO_2 with diffraction peaks at an angle 2θ of 26.6, 33.9, 38, 38.9, 42.5, 51.8, 54.7, and 57.8 corresponds the plane of reflections of (110), (101), (200), (111), (210), (211), (220), and (002) respectively, justify the tetragonal crystal phase of SnO_2 (JCPDS 88-0287). GIXRD has been done on the thin film sample, which is shown in **figure 3.4 b)**, also supports the crystalline phases of SnO_2 with clear peaks from (110), (101), (111), and (211) reflections.

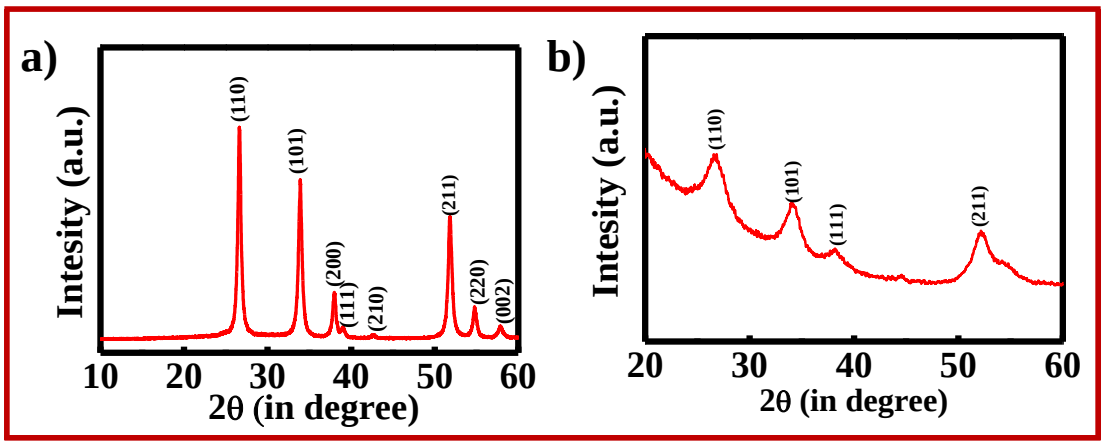

***Figure 3.4: a)** XRD analysis of SnO_2 powder annealed at 500 °C and **b)** GIXRD analysis of SnO_2 thin film annealed at 500 °C.*

3.2.3 Optical Properties of Li_2ZnO_2 Thin Films

The optical transmission spectrum of solution-processed thin-film Li_2ZnO_2 coated on a quartz substrate is shown in **figure 3.5 a)**. The Li_2ZnO_2 thin-film exhibits an average transmittance of over 94% in the visible region (400-700 nm). The higher transmittance of this thin film occurs due to very low-level scattering from the smooth surface. On the other hand, higher transmittance of the thin film in the visible region indicates that the film contains very low-level impurity, voids, and defects. In general, voids and defect-free thin film helps to mitigate the leakage current, which is a very crucial parameter for high-performance thin-film transistors. Hence, Li_2ZnO_2 thin-film with such kind of low-level defect and voids is beneficial for fabricating high-performance thin-film transistors. The optical band gap was extracted by extrapolating the linear region of the square of the absorption coefficient (αhν) to the x-axis, as shown in **figure 3.5 b)**. It is observed that the band gap of the Li_2ZnO_2 thin film is 3.3 eV, as reported earlier.

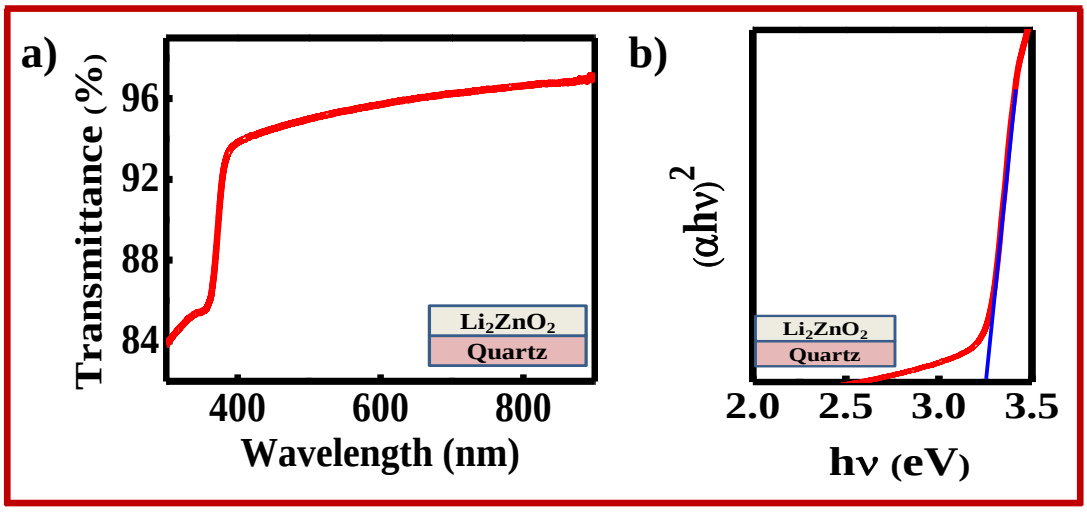

Figure 3.5: a) *Optical transmittance spectra of the solution-processed Li_2ZnO_2 dielectric thin film annealed at 500 °C for Li_2ZnO_2/quartz(inset)* ***b)****Tauc's plot corresponding to Li_2ZnO_2 thin film.*

3.2.4 X-Ray Photoelectron Spectroscopy

In order to confirm the chemical composition of the elements present in the Li_2ZnO_2, thin film samples were investigated by XPS, as shown in **figure 3.6**. To adjust the charge-induced shift, all the XPS spectra are aligned by taking C 1s (284.6 eV) as the reference. **Figure 3.6 a)** shows Li 1s XPS spectrum of Li_2ZnO_2 dielectric film. Due to asymmetry in the spectrum, Li 1s peak has been deconvoluted into two sub-peaks. These peaks are found to be centered at 54.6 and 56.0 eV, respectively. The high binding energy (B.E.) peak located at 56.0 eV is mainly due to the Li-O metal bond. **Figure 3.6 b)** represents the O 1s core-level spectrum of Li_2ZnO_2 dielectric film. The oxygen spectrum is deconvoluted into three pseudo-voigt sub-peaks centered at 530, 531.7, and 534.3 eV, referring to different oxygen environments. The low binding energy peak located at 530 eV is due to lattice oxygen ions in Li_2O.[131] The second peak at 531.7 eV may be attributed to O^{2-} ion in oxygen-deficient regions in a lattice, usually having oxygen vacancies within the matrix of ZnO.[140] The peak located at 534.3 eV shows a very small contribution and has been ignored thereof. **Figure 3.6 c)** indicates the Zn 2p spectra of Li_2ZnO_2 dielectric film. The peaks centered at binding energies of 1022.3 and 1045.3 eV correspond to Zn $2p_{3/2}$ and Zn $2p_{1/2}$ orbitals with an energy difference of approx. 23 eV under spin-orbit coupling. The above data indicates that the presence of lithium does not change the valence state of Zn supporting the existence of Zn atom in +2 oxidation state.[141-143]

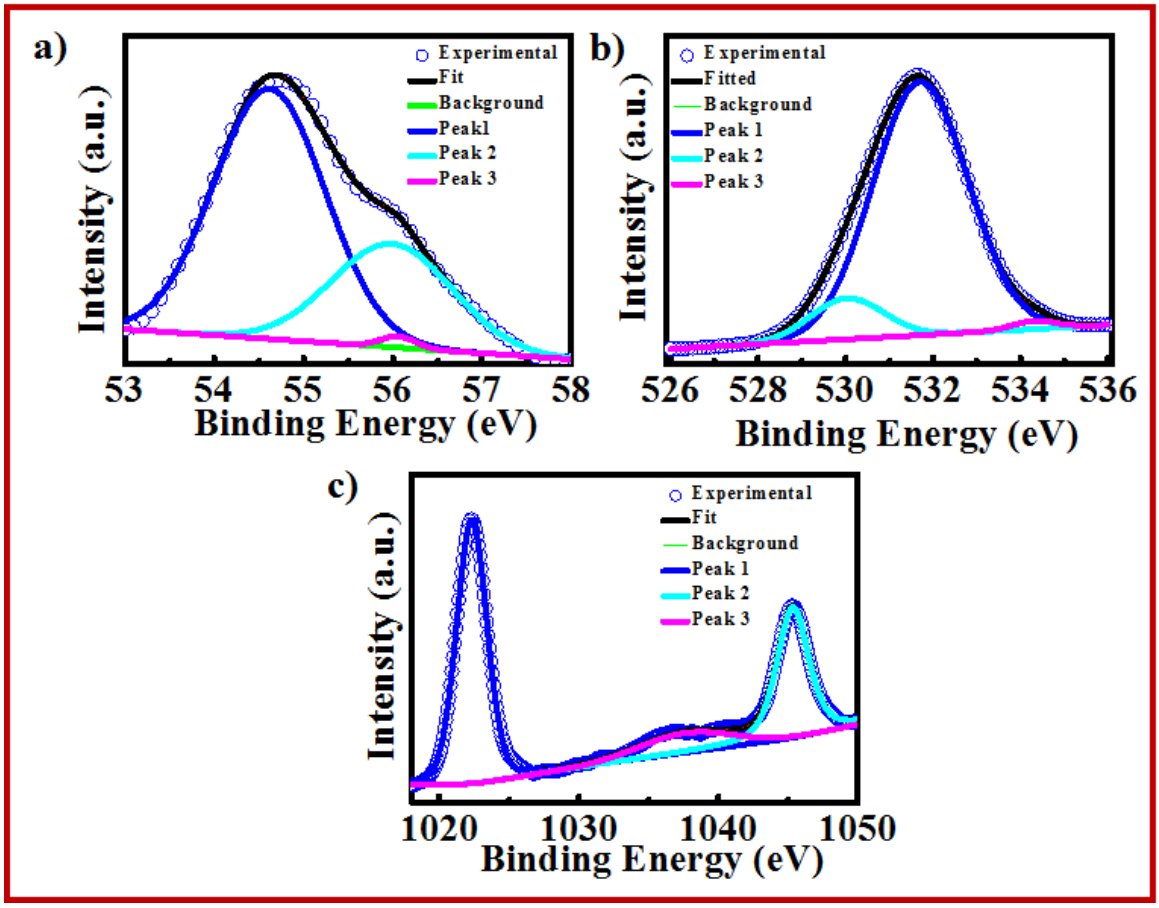

Figure 3.6: *XPS spectra of a different metal element present in Li_2ZnO_2 dielectric thin film* ***a)*** *Li 1s,* ***b)*** *O 1s, and* ***c)*** *Zn 2p from the sample of p^+-Si/Li_2ZnO_2 annealed at 500 ^oC, respectively.*

3.2.5 Surface Morphology

Since the dielectric/semiconductor interface plays an essential role in the performance of the thin-film transistors, the characterization of surface morphology of dielectric thin film is very crucial. As it is known that the rough interface (dielectric/semiconductor) always acts as transport barriers and hinders the transportation of charge carriers in semiconductors, it is essential to fabricate high-quality dielectric thin film with very low roughness. If the dielectric surface is rough, then the charge carriers require much energy to cross the interface; hence the overall mobility of TFT gets suppressed. Therefore, the surface morphology of p^+-Si/ Li_2ZnO_2 and p^+-Si/ Li_2O dielectric thin films annealed at 500 ^oC were

investigated by atomic force microscopy (AFM). The roughness of dielectric Li_2ZnO_2 and Li_2O annealed at 500 ^oC are 3.95 nm and 5.42 nm, respectively, which is admissible for thin-film transistors. However, the higher roughness of Li_2O dielectric may produce a significant variation of carrier mobility of the device mainly due to surface trap states. The 500 ^oC temperature is effective to diminish the complex ligand and to form dense metal-oxygen-metal bonds. Li_2ZnO_2 and Li_2O films are dense and void-free, as evident from 3-D images (AFM). Therefore, this smooth Li_2ZnO_2/SnO_2 and Li_2O/SnO_2 interface are suitable for thin-film transistors with high performance.

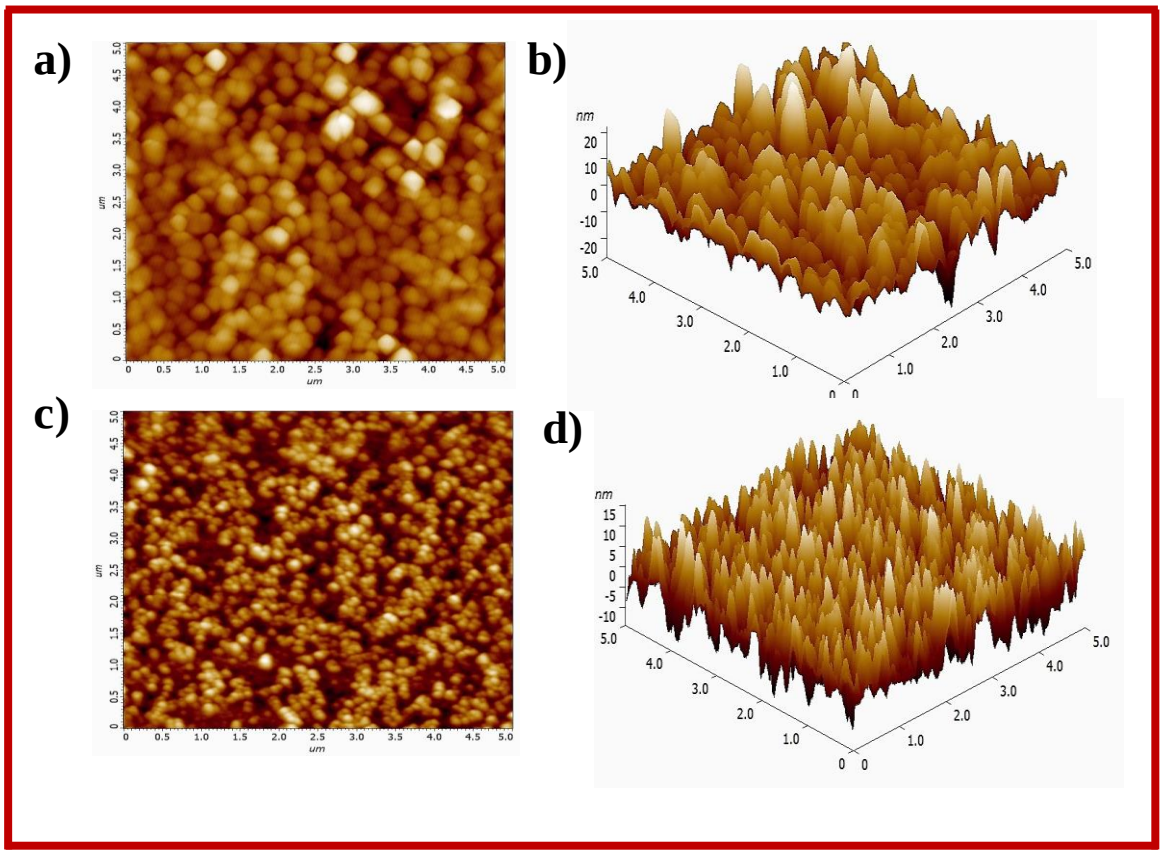

Figure 3.7: *2-D Surface morphology(scan area 5 x 5 µm) of Li_2ZnO_2/p^+-Si annealed at the temperature of* ***a)****500 ^oC(2D topography),* ***b)*** *500 ^oC (3D topography) and Li_2O/p^+-Si annealed at the temperature of* ***c)****500 ^oC (2D topography) and* ***d)*** *500 ^oC (3D topography)(scan surface area 5 x 5 µm), respectively.*

3.2.6 Dielectric and Electrical Measurements

To understand the electrical properties of as-deposited Li_2ZnO_2 film, we have performed current-voltage (I-V) measurements using a metal-insulator-metal device architecture (p^+-Si/Li_2ZnO_2/Al). The leakage current density of Li_2ZnO_2 dielectric at an annealing temperature of 500 ^oC is 2×10^{-7} A cm^{-2} at the operating voltage of 2 V, as shown in **figure 3.8 a)**. This leakage current density is less compared to the other reported dielectric based TFTs.[144] This low leakage current density may be attributed to the unavailability of carriers in the valence or the conduction band of Li_2ZnO_2 dielectric instead of having a lower band gap (3.3 eV). Additionally, due to a very less number of trap state and pinhole density, the amount of sidestepping current is also very less. It is observed that the breakdown is around 8-9 times higher than the normal operating voltage of the device (≥ 2V). Hence, this voltage of Li_2ZnO_2 thin film is ~ 17 V, which results suggested that the solution-processed ionic Li_2ZnO_2 dielectric is appropriate to use as a gate dielectric layer for the fabrication of TFTs.

Furthermore, to examine in detail the dielectric behavior of Li_2ZnO_2, frequency-dependent capacitance (C-*f*) measurement has been performed within the range of 20 Hz to 1 MHz, which is shown in **figure 3.8 b)**. The capacitance of a p^+-Si/Li_2ZnO_2/Al device decreases with frequency as expected from such kind of dielectric. Since the capacitance of this Li_2ZnO_2 thin film depends mainly on ionic polarization, which is a slower process resulting in a decrease in capacitance at a higher frequency range. However, the capacitance up to 10 kHz is within a 10% range of the DC capacitance value, implying the uniform device performance under the limited frequency region. The measured capacitance value of Li_2ZnO_2 thin film is 302 nF cm^{-2} at 50 Hz, which is significantly larger compared to that of the

conventional thermally grown SiO_2. Therefore, Li_2ZnO_2 thin film is a good alternative to be used as a gate dielectric for TFT fabrication.

On the other hand, Li_2O dielectric thin film shows higher leakage current and capacitance as compared to Li_2ZnO_2 dielectric. **Figure 3.8 c)** presents the I-V measurements with a metal-insulator-metal device structure (p^+-Si/Li_2O/Al). The leakage current density at 2V is 1×10^{-6} A cm^{-2}, which is large as compared to Li_2ZnO_2 dielectric. **Figure 3.8 d)** shows the capacitance vs. frequency within the range of 20 Hz to 1 MHz. At 50 Hz, the measured capacitance value is 435 nF cm^{-2}. From the above data, we suggest that Li_2ZnO_2 dielectric is better than Li_2O.

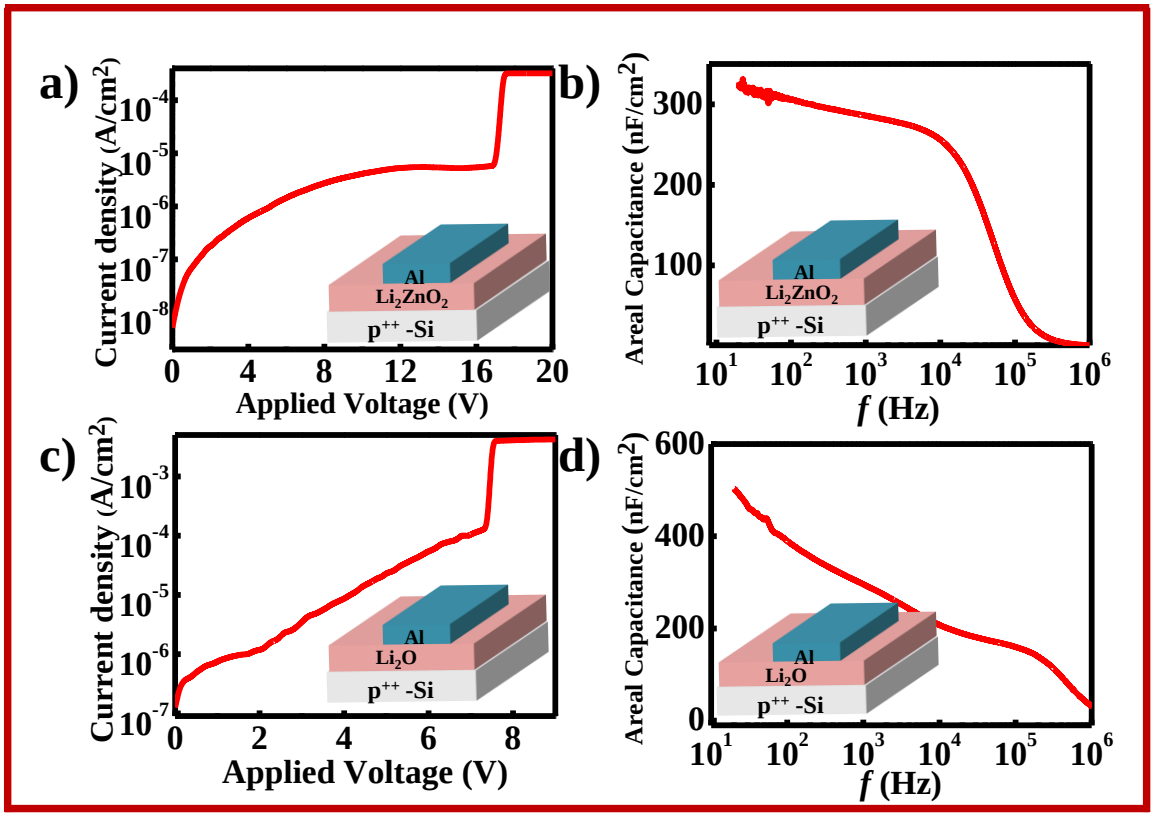

Figure 3.8: a) *Leakage current density vs. applied voltage of Li_2ZnO_2 and* ***c)*** *Li_2O thin film;* ***b)*** *capacitance vs. frequency curves of solution-processed ionic dielectric Li_2ZnO_2 and* ***d)*** *Li_2O thin film, respectively.*

3.3 Device Fabrication

In all of our experiments, bottom-gate top-contact thin-film transistors were fabricated on heavily doped (p^+-Si) silicon substrate. To fabricate such kind of devices, at first, p^+-Si wafers (15 mm x 15 mm) were cleaned by soap solution and then cleaned by water, acetone, and isopropanol for 30 min each in an ultra-sonication bath. After cleaning, the wafers were dried by passing dry air. Finally, all the substrates cleaned by the oxygen-plasma cleaner to make them hydrophilic, which is a very crucial step for sol-gel film fabrication because it allows high uniformity of the thin film by making it pinhole-free, less trap state. After the cleaning process, the precursor sol of Li_2ZnO_2 was spin-coated on silicon substrates at 4000 rpm for 60s under ambient atmospheric conditions. Spin coated samples were immediately kept on a preheated hot plate at 80 ^oC for two minutes to remove the solvent and make it dry. After drying, the samples were annealed at the temperature of 350 ^oC in the furnace for 30 minutes. Then this process was repeated two more times and finally annealed the thin film at 500 ^oC for 30 minutes under the ambient atmospheric condition to obtain the polycrystalline phase of Li_2ZnO_2. For semiconductor deposition, a 300 mM solution of SnO_2 was coated on top of Li_2ZnO_2 coated p^+-Si substrate at 3000 rpm followed by a drying process on a preheated hot plate at 120 ^oC for 5 minutes. These dried samples were immediately transferred to a preheated high-temperature furnace at 500 ^oC to anneal the sample for 30 minutes that form polycrystalline SnO_2 film on Li_2ZnO_2 dielectric layer. The same procedure was followed for Li_2O dielectric based SnO_2 TFT fabrication. Finally, aluminum source and drain electrode were deposited by thermal evaporator on top of the SnO_2 layer under a pressure of 6.0 x 10^6 Pa with a shadow mask to complete the TFT fabrication.

3.4 Transistor Characterization

To realize the quality of Li_2ZnO_2 as a gate dielectric, TFT has been fabricated on highly doped silicon (p^+-Si) with a bottom gate top contact device geometry. Sol-gel derived SnO_2 has been used as a semiconductor channel, whereas Interdigitated aluminum metal electrodes have been used as a source and drain contact. The width to channel ratio of the device is 118 (23.6 mm/ 0.2 mm). Because of the grain boundary effect, the choice of W/L ratio is important to avoid the overestimation of mobility. **Figure 3.9 a) and b)** show the output and transfer characteristics of TFT fabricated with solution-processed Li_2ZnO_2 dielectric. The applied drain and gate voltage were swept from 0V to 2V and -0.5V to 2V, respectively. These characteristics indicate that the device is a typical n-channel transistor with a clear linear and current saturation region within the voltage range of 2V. Similarly, **figure 3.9 c) and d)** show the output and transfer characteristics of TFT with solution-processed Li_2O dielectric indicating the clear low voltage operation. However, the current level and on/off ratio are significantly poorer with respect to that of the Li_2ZnO_2 based device.

Effective carrier mobility (μ) and sub-threshold swing (SS) of TFT has been calculated from the following equations.

$$\mathbf{I_D} = \mu \mathbf{C} \frac{\mathbf{W}}{\mathbf{2L}} (\mathbf{V_G} - \mathbf{V_T})^{\mathbf{2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$\boldsymbol{SS} = \left[\frac{\boldsymbol{d(log\, I_D)}}{\boldsymbol{dV_G}}\right]^{\boldsymbol{-1}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

Where I_D is saturation drain current, C is the capacitance per unit area, V_G is gate voltage, and V_T is the threshold voltage. The extracted carrier mobility, on/off ratio, and subthreshold swing for Li_2ZnO_2-based TFT are 23 $cm^2\ V^{-1}\ s^{-1}$, 6×10^3, and 390 mV $dec^{-1,}$ respectively. The capacitance at low frequency (50 Hz) is considered for the mobility calculation to avoid the

overestimation since a direct voltage was used in the TFT operation. This carrier mobility is much higher than that of the previously reported SnO_2 TFT.[145] However, the extracted carrier mobility, on/off ratio, and subthreshold swing for Li_2O based TFT are 4 cm^2 V^{-1} s^{-1}, 2× 10^2, and 470 mV $dec^{-1,}$ respectively, which clearly indicates the advantages of Li_2ZnO_2 dielectric for TFT fabrication. The comparative device parameters of these two devices are presented in **Table 3.1**.

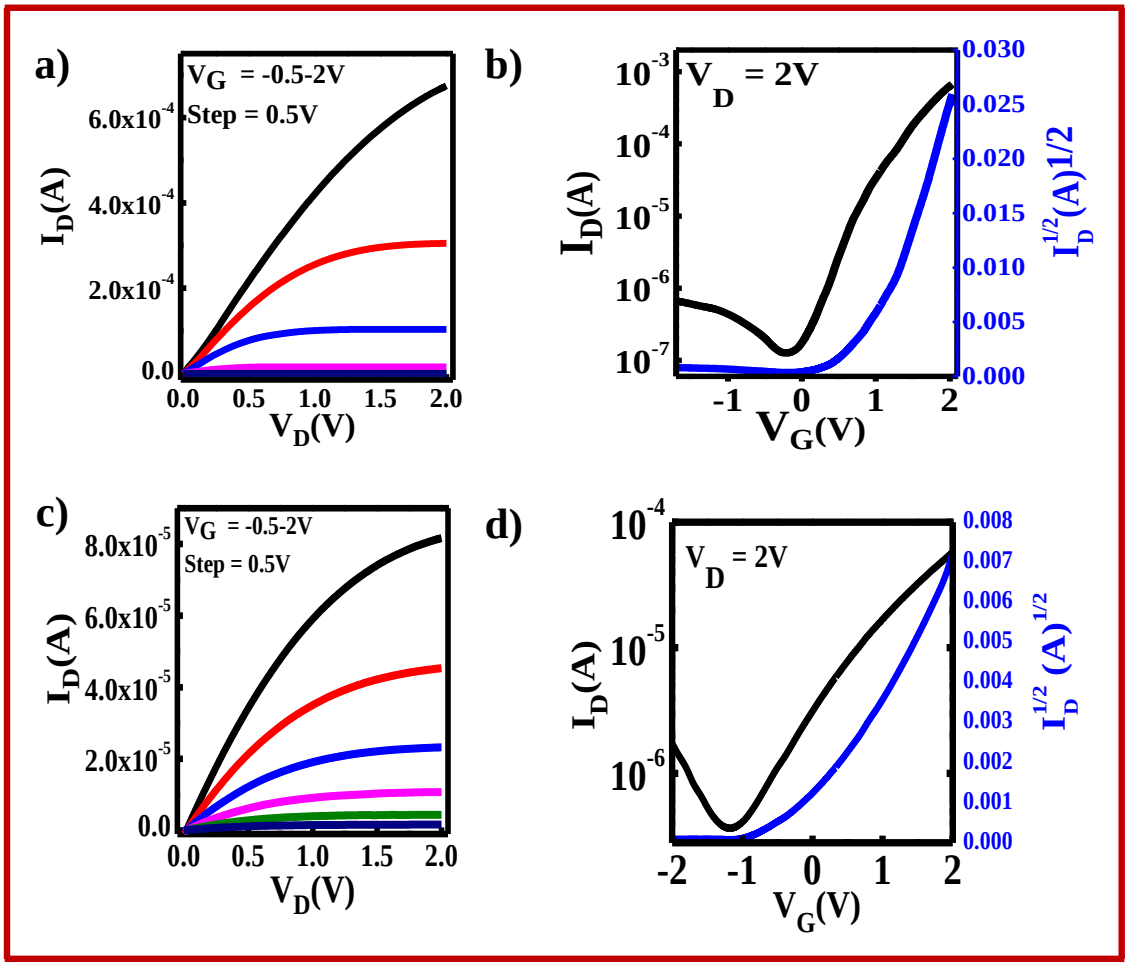

Figure 3.9: a) *Output,* ***b)*** *transfer characteristics of the SnO_2 TFT with Li_2ZnO_2 dielectric;* ***c)*** *Output and* ***d)*** *transfer characteristics of the SnO_2 TFT with Li_2O dielectric annealed at 500 ^oC with device architecture p^+-Si/Li_2ZnO_2/ SnO_2/Al and p^+-Si/Li_2O/ SnO_2/Al, respectively.*

Table 3.1: The summary of different parameters of SnO_2 TFTs using two different types of dielectric.

Sr. No.	Dielectric	Dielectric Annealed temperature	C (nF/cm^2) at 50 Hz	V_{Th} (V)	ON/OFF	Density of interfaces states (N_{ss}^{max})(cm^{-2})	Subthreshold swing (SS) (mV/decade)	Electron Mobility (μ) ($cm^2\ V^{-1}\ sec^{-1}$)
1.	Li_2ZnO_2	500 °C	302	0.4	6x 10^3	5.2 x10^{12}	390	23
2.	Li_2O	500 °C	435	-0.5	2 x 10^2	1.7 x10^{13}	470	4

The maximum density of the interface states (N_{ss}^{max}) is calculated from subthreshold swing (SS) data of output characteristics by using the following equation.[146]

$$N_{SS}^{max} = \left[\frac{SS \times \log e}{kT/q} - 1\right]\frac{C}{q} \qquad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where k is Boltzmann constant and q is electronic charge. The maximum density of the interface states $\boldsymbol{N_{ss}^{max}}$ was calculated for Li_2ZnO_2 and Li_2O dielectrics are 5.2×10^{12} and 1.7 x $10^{13,}$ respectively, which are significantly low for solution-processed metal oxide TFT.[119] The small $\boldsymbol{N_{ss}^{max}}$ values indicates that the dielectric-semiconductor interface for both types of TFTs are very smooth to achieve high carrier mobility. Overall, in addition to low operating voltage, Li_2ZnO_2 ionic dielectric forms a coherent and well-matched interface with the SnO_2 semiconducting layer with the lower number of interfacial traps that result in reasonably high carrier mobility of TFT.

'Bias stress stability' test was performed to measure the effect of Li^+ ion on the stability of the device. The repeated transfer characteristics experiment was performed for 30 minutes, keeping an interval of 3 minutes to check the effect of Li^+ ion diffusion. **Figure 3.10 a) and b)** shows the I_D-V_G data for the devices with Li_2ZnO_2 and Li_2O dielectric. The device with

Li_2ZnO_2 dielectric thin film shows no significant variation in transistor parameters such as on/off ratio, mobility, and subthreshold swing. However, the device with Li_2O dielectric thin film shows a small variation in these parameters.

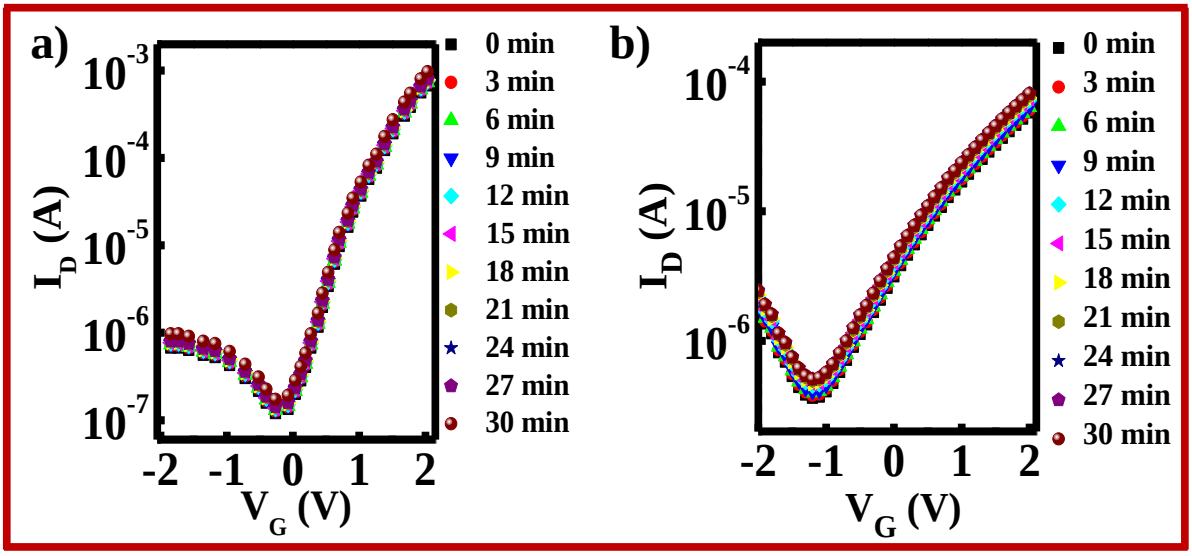

Figure 3.10: *Operational Stability of the ionic dielectric and evolution of the transfer curves of an ionic dielectric* ***a)*** *Li_2ZnO_2/SnO_2 TFT and* ***b)*** *Li_2O/SnO_2TFT at a fixed V_D of 2V during the stress test.*

3.5 Conclusions

In summary, a new low bandgap ion-conducting gate dielectric, Li_2ZnO_2, has been developed by a low-cost solution-processed technique and successfully used for TFT fabrication. This sol-gel derived film was annealed at 500 ^oC to achieve the crystalline phase of Li_2ZnO_2. To ensure optical and electrical properties of this material, a thin film of Li_2ZnO_2 has been fabricated on quartz and p^+-Si substrate at 500 ^oC. The film is highly transparent in the visible region due to less scattering at the interface, and it shows high electrical insulating nature indicating Li_2ZnO_2 as a suitable gate dielectric for TFT application. To realize the applicability of this dielectric thin-film, solution-processed SnO_2 TFT was fabricated. It is observed that the TFT requires 2V or less to operate the device as expected from the ion-conducting dielectric. The TFT shows very high electron mobility of 23 $cm^2 V^{-1} s^{-1}$, which is

much higher than that of the previously reported SnO_2 TFT.[145, 147] Moreover, the device shows a high on/off ratio (~ 10^4) with a low subthreshold swing (390 mV dec^{-1}). In addition, the Li_2ZnO_2 film requires a processing temperature of 500 ^oC to obtain the crystalline phase of the dielectric, which is compatible with any glass or silicon substrate. This device performance has been compared with sol-gel derived reference Li_2O dielectric, which clearly indicates the superiority of Li_2ZnO_2 dielectric for TFT fabrication.