Chapter 6

Conclusion and Future Scopes

6.1 Summary of Major Findings of the Thesis

The main objective of this thesis is to investigate device and circuit-level performances of source pocket engineered (SPE) GaSb/Si heterojunction (HJ) vertical TFETs (VTFETs). The effects of three different engineering techniques such as the gate-oxide stacking engineering, source pocket engineering, and heterojunction engineering on the device and circuit-level performance parameters of the VTFET architectures have been investigated in the present thesis. Major findings of the thesis are listed below.

Chapter-2 discusses the effects of source pocket engineering on the DC and analog/RF performance parameters of the SPE GaSb/Si HJ VTFETs. The TCAD simulation results show that SPE GaSb/Si HJ VTFET has lower SS (~26 mV/dec), smaller threshold voltage (~0.31 V) and higher I_{ON}/I_{OFF} ratio ($7.5x10^{11}$) than their corresponding values (of 43 mV/dec, 0.45V and $6.87x10^{11}$) of the GaSb/Si HJ VTFET (without any source pocket). The proposed SPE GaSb/Si HJ VTFET also shows a better temperature stability over the GaSb/Si HJ VTFET. The SPE GaSb/Si HJ VTFET has 1.22×g_m, 3.5×f_T, 3.5×f_{max}, 4.3×GBP, 1.79× TGF and 3.6×TFP with respect to their corresponding values of g_m, f_T, f_{max}, GBP, TGF and TFP of the GaSb/Si HJ VTFET.

Chapter-3 investigates the effect of lateral and vertical HfO_2/Al_2O_3 gate-oxide stacking on the performance parameters of SPE GaSb/Si HJ VTFET considered in Chapter-2. The HfO_2/Al_2O_3 lateral gate-oxide stacking shows higher ON-current, higher I_{ON}/I_{OFF} ratio, lower SS, higher g_m, g_d, f_T, GBP, TGF, TFP, gm2, and gm3 than

those values obtained for the SPE GaSb/Si HJ VFET and SPE GaSb/Si HJ VTFET with only Al_2O_3 as gate oxide (without any gate stacking). Higher intrinsic gate capacitances are observed in the laterally stacked gate-oxide structure than the capacitances obtained for the vertical stacking and VTFET with only Al_2O_3 as gate oxide. The higher intrinsic gate capacitances of the laterally stacked oxide based SPE GaSb/Si HJ VTFETs may degrade the performance of the device at higher frequencies.

Chapter-4 investigates the effect of lateral and vertical HfO_2/Al_2O_3 gate-oxide stacking (discussed in Chapter-3) on the performance of 8T SRAM cells. The circuit-level performance analysis of the 8T SRAMs have been carried out using CADENCE Virtuoso tool by virtue of 2-D look up table-based Verilog A code after exporting the data related to I-V and C-V characteristics of the proposed TFETs from SILVACO ATLAS^{TM} 3-D TCAD tool. The SRAMs designed with laterally stacked gate-oxide based SPE GaSb/Si HJ VTFETs show higher read signal-to-noise-margin (SNM), higher write margin, and lower write delay as compared to those of the SRAMs designed with vertically stacked VTFET and VTFETs with only Al_2O_3 as gate oxide based VTFETs.

Chapter-5 compares the device and circuit level performance characteristics of SPE GaSb/Si HJ VTFET with those of the most commonly used SPE Ge/Si HJ VTFET. The SPE Ge/Si HJ VTFETs show improved drive current (ON-current), transconductance (g_m), cut-off frequency (f_T), and transconductance generation factor (TGF) than their corresponding values of the SPE GaSb HJ VTFETs. However, their sub-threshold slopes are observed to be nearly same. The I_{ON}/I_{OFF} ratio of the GaSb/Si based VTFET is found to be larger than the Ge/Si based VTFET. In addition, I_{OFF} and intrinsic gate capacitances are found to be smaller in the GaSb/Si based VTFET than those of the Ge/Si based VTFET.

The circuit level analysis has been invested by simulating the inverter circuits and 8T SRAM cells using the two devices. Better static and time varying characteristics of the inverter and SRAM cells designed with GaSb/Si VTFETs are observed as compared to corresponding characteristics obtained in the Ge/Si VTFET based inverter and SRAM. This is attributed to lower intrinsic gate capacitances/Miller capacitances and higher I_{ON}/I_{OFF} ratio of the SPE GaSb/Si HJ VTFET than the Ge/Si based VTFETs.

The research carried out in the present thesis suggest that both the laterally and vertically stacked Al_2O_3/HfO_2 gate oxide based SPE GaSb/Si VTFETs are better candidate for RF and digital logic circuit applications than the commonly used Ge/Si VTFETs. However higher intrinsic capacitance in the stacked gate-oxide based devices result in higher read delays in 8T SRAM than that obtained for the 8T SRAM designed with a single gate-oxide based VTFETs.

6.2 Future Scope of Work

In this thesis, we have presented the device and circuit-level performance analysis of SPE GaSb/Si HJ VTFET by considering its applications in some basic circuits like digital inverter and 8T SRAMs. In this section, we will outline some future scopes of research related to the present thesis which are given as follows:

- The presented SPE GaSb/Si HJ VTEFTs should be verified experimentally to analyze the impact of bulk traps at heterojunction interface between GaSb and Si on device and circuit level performances.
- Research related to the development of equivalent circuits models of the proposed devices for SPICE simulations may be carried out.
- The preset research deals with the SPE HJ VTFET with channel lengths above 25 nm due to issues related to the SILVACO ATLAS TCAD tool. The present

research can be extended to sub-25 nm channel length SPE HJ VTFET structures to match with the present technology node. Further, rigorous theoretical investigations are also required for sub-25 nm SPE GaSb/Si HJ VTFETs by considering all the quantum mechanical effects for better physical insight of the device operations.

- The present study can be extended to other structures like Tri-gate, quadrupole gate, FIN-TFET considering GaSb/Si heterojunction to analyze both device and circuit level performances in lateral device too as this heterojunction based TFET has been reported in this thesis for the first time.
- Low frequency noise analysis can be made for our proposed GaSb/Si HJ TFET to analyze the device performance in the presence of noise.
- The circuit level simulation is implemented using CADENCE virtuoso tool based on 2D look up table-based Verilog-A model. Compact model can also be developed to implement circuit simulation for the proposed device.
- Circuit level performance analysis here in this thesis is limited to some basic important circuit like digital logic inverter and 8T SRAM for IoT related applications. The concept can be extended to the analysis of other analog circuits like differential amplifier, current mirror, comparator and digital circuits like DRAM, full adder, level shifter etc. designed using the proposed SPE GaSb/Si HJ VTFETs considered in this thesis. In addition, neuromorphic computing related applications based analog integrated circuits can also be implemented using the proposed SPE GaSb/Si HJ VTFETs.