Preface

Low-power memory circuits are essential for all internet of things (IoT)/ artificial intelligence (AI) enabled processors and sensors. The tunnel field effect transistor (TFET), also known as the green transistor, is a potential device for replacing the conventional metal oxide field effect transistor (MOSFET) for low-power VLSI applications due to its extremely low OFF-state current and low subthreshold swing (SS) (much below the theoretical Boltzmann limit of 60 mV/decade at room temperature applicable for the conventional MOS devices). However, the low ON-state current and ambipolar conduction are the major drawbacks of the TFETs. Several techniques such as the source pocket engineering (*i.e.,* sandwiching a thin heavily doped layer known as source pocket in between source and channel regions of the TFET), gate-dielectric engineering (*i.e.,* high-*k* dielectrics in place of silicon dioxide (SiO_2) either in the form of single dielectric or lateral/vertical stacked gate oxide, SiO_2/high-*k* etc.), multi-gate engineering (*i.e.,* double-gate, tri-gate, gate all around), band gap engineering (*i.e.,* narrow band-gap materials such as germanium (Ge), indium arsenide (InAs), indium antimonide (InSb) in the place of silicon (Si) channel, use of low band-gap materials such as Ge and InAs as a source, so as to form heterojunction at source(drain)/ channel interface) have been explored by the researchers to overcome the above mentioned drawbacks. Many researchers have projected the vertically grown TFET (VTFET) as the better structure over its conventional planner structure due to its easier fabrication, better integration density, lower leakage current and smaller trapping related issues. However, TFETs present some challenges for their circuit-level applications due to their low ON current, different current -voltage (I-V) and capacitance-voltage (C-V) characteristics than those of the MOSFET due to asymmetric types of doping in the source and drain regions, super linear onset along with high saturation voltage of device output characteristics, and Miller effects associated with the typically high gate–drain capacitances. In view of the above, the present thesis deals with some technology computer aided design (TCAD) based simulation studies of the device and circuit-level performance characteristics of source pocket engineered (SPE) and gate-oxide structure

engineered gallium antimonide (GaSb)/ silicon (Si) heterojunction (HJ) VTFETs for the first time. The overall chapter-wise layout of the thesis is given below:

Chapter-1 presents a brief introduction of TFETs and their properties for low power applications. Various reported techniques used for improving the drive current of the TFETs have also been discussed. A general review of various state-of-the-art related to device and circuit-level simulation works on the TFETs been briefly discussed. Finally, based on the literature survey, the scopes of the present thesis have been outlined at the end of this chapter.

Chapter-2 investigates the DC and RF performance of GaSb/Si HJ VTFET with and without a source pocket. For the first time GaSb with low bandgap has been used in the source region to enhance carrier tunneling through the source (GaSb)-channel (Si) interface. The effects of temperature on sub-threshold swing (SS) and I_{ON}/I_{OFF} ratio are investigated for the presented vertical TFETs with and without source pocket. In addition to this, different analog/RF figures of merit (FOMs) such as transconductance (g_m), output conductance (g_d), gate to drain capacitance (C_{gd}), gate to source capacitance (C_{gs}), cut-off frequency (f_T), gain bandwidth product (GBP), maximum frequency (f_{max}), transit time (τ), transconductance generation factor (TGF) and transconductance frequency product (TFP) are also analyzed for the GaSb/Si HJ VTFETs with and without a source pocket. Device-level performance parameters of the proposed VTFETs have been compared with some recently reported non-conventional TFET structures. In addition, performance characteristics of the proposed VTFET have been compared with those of an All-Si VTFET with source pocket. The effects of temperature on sub-threshold swing (SS) and I_{ON}/I_{OFF} ratio is thoroughly investigated and compared for both the presented TFET. Along with the DC parameters, different analog/RF parameters are also extensively studied for both the TFETs. The commercially available SILVACO ATLAS^{TM} 3-D TCAD tool has been used for simulating the presented VTFETs.

Chapter-3 presents the impact vertical and lateral HfO_2/Al_2O_3 gate oxide stacking on the device level performance of the SPE GaSb/Si HJ VTFET considered in Chapter-2. In the vertical gate oxide stacking, the high-*k* (HfO_2) is placed over the low-*k* (Al_2O_3) to form the effective gate oxide structure of the proposed TFET. On the other hand, the high-*k* (HfO_2) oxide is placed near the source side and the low-*k* (Al_2O_3) oxide near the drain sided in a cascaded manner to form the resultant gate-oxide structure of the proposed

device. The effect of later/vertical HfO_2/Al_2O_3 on the sub-threshold swing (SS), I_{ON}/I_{OFF} ratio along, intrinsic capacitances and analog/RF figures of merit (FOMs) such as transconductance, output conductance, cut-off frequency, gain bandwidth product, transconductance generation factor (device efficiency), and transconductance frequency product have also been analyzed for the proposed gate oxide and source pocket engineered GaSb/Si HJ VTFETs under study. The commercially available SILVACO ATLAS^{TM} 3-D TCAD tool has been used for the present study.

Chapter-4 reports the performance analysis of 8T SRAM cell designed by our proposed lateral/vertical HfO_2/Al_2O_3 gate oxide stacking based SPE GaSb/Si HJ VTFETs considered in Chapter-3. The circuit level simulations have been performed by using 2D look up table-based Verilog-A model in the CADENCE Virtuoso tool. The effects of the lateral/vertical gate-oxide stacking on various performance parameters such as the write margin, read margin, write delay and read delay of the proposed 8T SRAM cells have been investigated in details. The effect of gate oxide stacking on intrinsic gate capacitance so as on the performance of 8T SRAM cell has been thoroughly analyzed.

Chapter-5 reports a comparative study of the device and circuit level performances of the SPE GaSb/Si HJ VTFETs and SPE Ge/Si HJ VTFETs. First, the DC and RF performances of the two devices have been compared. Then the performances of a digital logic inverter and 8T SRAM cell designed by GaSb/Si and Ge/Si heterojunction VTFETs have been compared. Device simulation has been carried out using commercially available SILVACO ATLAS^{TM} 3-D TCAD tool whereas the circuit simulation has been performed using 2D look up table-based Verilog-A model in the CADENCE Virtuoso tool.

Chapter-6 is devoted to summarize the major observations and findings of the thesis. Finally, some future scopes of research related to the thesis have been briefly discussed at the end of this chapter.