Analytical Modeling and Simulation of Some Engineered Cylindrical-Gate JAM MOSFETs

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by

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Conclusion and Future Scope

7.1 Introduction

The main objective of this thesis is to investigate the performance of some engineered cylindrical gate (CG) JAM MOSFETs through theoretical modeling and TCAD analysis. 2-D analytical models have been developed for investigating the effects of three different engineering techniques namely the gate-material engineering, gate-oxide engineering, and channel doping engineering on the electrical performance characteristics of the CG-JAM MOSFETs have been studied in this thesis. A compact DC model has also been proposed for the stacked gate oxide structure based CG JAM MOSFETs. Further, an attempt has been made to develop a unified DC compact model valid for both the CG JAM MOSFET and inversion mode CG MOSFETs. Finally, the device and circuit level performance of a Gaussian doped CG JAM MOSFET have been carried out using commercial TCAD tools from COGENDA^{TM}. The present chapter is used to summarize the major findings of this thesis. Finally, some future scopes of research related to the area of the present thesis have been outlined at the end of this thesis.

7.2 Chapter-wise summary and conclusion

Chapter-1 introduces the CMOS scaling rules, their advantages and adverse effects on the performance parameters of the MOS devices. Various non-classical MOSFET structures have been briefly introduced to mitigate the short-channel effects (SCEs) resulting from technology scaling. The junctionless (JL)/JAM MOSFETs have been introduced as the next generation non-classical MOS transistor for low-power VLSI applications due to their ease in fabrication,

lower SCEs, and low OFF-state current. However, classical JL MOSFET suffers from low ON-current. Therefore, its modified structure called the junctionless accumulation mode (JAM) has been introduced to enhance the ON-current. The JAM MOSFETs are discussed to have increased HCEs and leakage currents like GIDL and gate leakage currents. Various methods such as gate-material engineering, gate-oxide engineering, and channel engineering techniques have been introduced to mitigate these effects in the JAM MOSFETs have been discussed. A detailed literature survey has been carried out for analyzing various techniques for the performance improvement of the JAM MOSFETs. Cylindrical gate (CG) JAM MOSFET with various device engineering techniques are observed to be having the minimum SCEs, maximum drain current, and minimum GIDL and leakage currents due to its maximum control over the channel of the device. Finally, based on the findings of the literature survey, the scopes of the thesis have been outlined at the end of this chapter.

Chapter-2 presents a 2-D analytical model for the electrical characteristics of a gate material and graded channel engineered CG JAM (CG DMGC JAM) MOSFET using the superposition principle for solving the Poisson's equation including only the depletion charges. The 2-D potential function has been used to model the electric fields in the channel. The threshold voltage has been modeled using the minimum central potential method. The roll-off and DIBL have been formulated. The GIDL and gate leakage currents of the proposed engineered CG JAM MOSFET have also been modeled. Further, the results of electrical characteristics of the proposed CG GCDM JAM MOSFET structure have been compared with those of the CG DM JAM MOSFET for various device parameters. The validity of the model results has been established by comparing the model results with their corresponding commercially available TCAD simulation data. The major contributions and observations of this chapter are listed below:

- To the best of our knowledge, the proposed 2-D analytical model for the CG GCDM JAM MOSFET has been formulated for the first time in the literature.
- Analytical modeling for the GIDL and gate leakage currents of proposed CG JAM MOSFET structure has also been formulated probably for the first time.
- GCDM CG-JAM MOSFET is shown to outperform the GC and DM engineered CG-JAM MOSFETs.
- Compared to CG DM JAM MOSFET shows slightly better performance over the CG GC JAM MOSFET.
- The proposed CG GCDM JAM MOSFET is shown to have smaller GIDL and gate leakage currents than GC and DM engineered CG JAM MOSFETs.

Chapter-3 presents the 2-D analytical modeling for the electrical characteristics of a laterally stacked HfO_2/SiO_2 hetero-dielectric (HD) gate-oxide, and graded channel (GC) engineered CG JAM MOSFET. The expressions for the 2-D potential and electric fields have been obtained following similar methods described in Chapter-2. The Poisson-Schrodinger equation has been solved for threshold voltage correction by considering quantum well approximation. Threshold voltage has been formulated by the minimum central potential method and considering quantum correction for ultrathin devices. A total drain current model including current at negative bias has been developed. The expressions for the transconductance (g_m) and drain conductance (g_d) have also been derived. The electrical characteristics of the proposed CG HDGC JAM MOSFET have been compared with CG-GC JAM MOSFET and CG-JAM MOSFET for various device parameters. The major contributions and observation of this chapter are given below:

- The 2-D analytical model for the CG HD-GC JAM MOSFET has been formulated for the first time.

- Analytical modeling of the threshold voltage by considering quantum corrections in CG JAM MOSFET structure has been obtained probably for the first time.
- The performance of the CG HD-GC JAM MOSFET is shown to excel over the CG GC JAM MOSFETs and simple CG JAM MOSFETs in terms of the electrical characteristics and lower HCEs.
- The roll-off and threshold voltage variations with respect to the drain bias are observed the minimum in the CG HD-GC JAM MOSFET.
- The effect of quantum confinement shown to increase both the threshold voltage and roll-off in ultrathin CG JAM MOSFETs. Further, the difference between classical and quantum-confined threshold voltage is shown to be increased with the decrease in the radius of the CG JAM MOSFETs.
- I_{ON}, $g_{m,}$ and g_d are found to be the highest whereas I_{OFF} is found the lowest in the CG HDGC JAM MOSFET among all the structures considered in this chapter.
- A very good matching of the model results with TCAD simulation data confirms the validity of the proposed models.

Chapter-4 presents a 2-D compact DC analytical model valid for the depletion and accumulation regimes of operation of an HD-DM-GC engineered CG-JAM MOSFET. The Poisson's equation considering both the depletion and accumulation charges has been solved using the superposition principle. The effects of both quantum confinements (described in chapter-3) and electrical confinement on the device characteristics have been considered. The threshold voltage has been formulated using depletion approximation and minimum central potential method. The drain current, g_m, and g_d have been modelled for all the operating regimes of the proposed device. The effects of temperature and trapped charges have also been included in this model. Further, the performance of the CG HDGCDM JAM MOSFET has

been compared with that of the CG JAM MOSFET for various device parameters. The major contributions and observations of this chapter are as follows:

- DC compact drain current model including GIDL has been developed for the DM, HD and GC engineered CG JAM MOSFETs has been considered for the first time.
- The 2-D analytical potential model valid for both the depletion and accumulation regimes for any doped CG MOS device has been developed possibly for the first time.
- The performance of the CG HDGCDM JAM is shown to be better than that of the simple CG JAM MOSFET structure.
- Both drain current and threshold voltage are observed to be decreased with the increase in operating temperature of the proposed structure.
- The effect of interface trapped charges on the performance of the proposed CG HDGCDM JAM MOSFET structure is smaller than the simple CG-JAM MOSFET.
- The potential model could be valid for the HDGCDM engineered conventional inversion mode (IM) MOSFETs.
- The validity of the proposed models have been established by comparing the model results with the commercially available TCAD simulation data.

Chapter-5 reports a unified 2-D quasi-ballistic continuous analytical model for the electrical characteristics of both the CG-JAM and IM MOSFET. This model is simpler than our previous model described in chapter-4. The model is continuous across the depletion and accumulation regimes of operation. The Poisson's equation considering both the depletion and accumulation charges has been solved using the superposition principle. Threshold voltage has

been modeled using the minimum central potential method. The continuous drain current model valid for both the depletion and accumulation regimes is developed by using the quasi-ballistic velocity correction method. The backscattering and ballistic effects are also considered. The major contributions and observations from this chapter are as follows:

- The unified 2-D DC compact model valid for both the depletion and accumulation regimes of operation of both the CG-JAM MOSFET and IM MOSFET has been reported possibly for the first time.

- The quasi-ballistic drain current model is formulated for the first time in this chapter for the CG JAM MOSFET. This is possibly also the first quasi-ballistic model for any doped-channel MOSFETs.

- The SCEs and OFF-current of the CG JAM MOSFETs are found to be smaller than those of the IM MOSFET. However, the drive current, g_m and g_d are of the IM MOSFET are higher than their corresponding values of the CG JAM MOSFETs.

- The good matching of the proposed analytical model results with the TCAD simulation data confirms the validity of the model.

Chapter-6 presents a TCAD based simulation study of the DC and RF performances of a Gaussian doped channel engineered and vertically stacked SiO_2/HfO_2 gate-oxide engineered CG JAM MOSFET. The laterally stacked gate oxide structure considered in the chapters 2, 3, and 4 are replaced by the vertically stacked structure. The proposed CG JAM MOSFETs are then used to design an inverter and a 6T SRAM circuits using a look-up table-based Verilog-A model in the Cadence^{TM} TCAD tool. Various static and dynamic characteristics of the inverter and 6T SRAM are analyzed in details. The major contributions and findings of this chapter are given below:

- The device and circuit level performance analysis of a Gaussian doped channel engineered CG JAM MOSFET has been carried out for the first time.

- Performance analysis of the proposed engineered CG JAM MOSFET based 6T SRAM cell with a vertical Gaussian doping in the channel and vertically stacked gate-oxide is reported for the first time in this chapter of the thesis.

- The proposed structure provides better flexibility in optimizing the performance of the CG JAM MOSFETs due to additional parameters peak position and straggle parameter of the channel engineering profile.

- The DC metrics like threshold voltage, intrinsic gain and I_{ON}/I_{OFF} ratio are improved for smaller values of straggle parameter. However, the I_{ON} and g_m are decreased with the increased value of the straggle parameter.

- RF metrics like f_T, GBW, f_{max}, TFP, transit time and capacitance are better for smaller values of straggle parameter.

- The smaller values of the straggle parameter reduces the power dispassion and increases the noise margin of the inverter circuit. However, it increases the delay and overshoot of the inverter.

- The reduced straggle parameter value increases the read stability, write ability but decreases the RAT and WAT of SRAM circuit.

7.3 Future Scope of Work

Some future scopes of research related to the works of present thesis are briefly described in the following:

- Although we have developed a 2-D DC compact model but a full compact model that also contains both AC and DC is much desired. Therefore, in this respect, a full 2-D compact model that will contain modeling of capacitances will further develop this field of study and effectively create an environment to develop a small signal and high-frequency circuit model of the device.
- The SHDGCDM JAM with a small nanogap near the drain area of the channel could be used to modulate capacitance and can be effectively used as a bio-sensor. The study and analysis of bio-sensor using this device could be interesting.
- We have included the effects of quantum confinement in the vertical direction. Further, a quasi-ballistic correction for devices up-to 10 nm has also been developed. Devices below 10 nm have full ballistic transport for which 3-D quantum effects need to be incorporated, which will be a much-desired model in the present scenario.
- JAM MOSFETs can work in impact ionization mode at a certain biasing condition, which provides a SS<60 mV/dec. Although the on-current of these devices is high the off-current is also high. Therefore, somehow if we could limit this off-current, these would the next-generation devices for ultra-scaling.

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