

## References

---

- J. E. Lilienfeld, "Method and apparatus for controlling electric current" US Patent, 1925.
- D. Kahng, and M. M. Atalla. "Silicon-Silicon Dioxide Field Induced Surface Devices." *In IRE Solid-State Device Res. Conf.*, Carnegie Institute of Technology, Pittsburgh., 1960.
- Gordon E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 114–117, April 19, 1965.
- R. H. Dennard, F. H. Gaenssle., H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuit.*, vol. 9, pp. 256-268, 1974.
- G. E. Moore, "Progress in Digital Integrated Electronics," Technical Digest 1975: *IEEE International Electron Devices Meeting*, pp. 11-13, 1975.
- Kamata, T., Tanabashi, K. and Kobayashi, K. (1976) 'Substrate current due to impact ionization in MOS-FET', *Japanese Journal of Applied Physics*, 15(6), pp. 1127–1133. doi: 10.1143/JJAP.15.1127.
- Poorter, T. and Zoestbergen, P. (1984) 'HOT CARRIER EFFECTS IN MOS TRANSISTORS T. Poorter and P. Zoestbergen Philips Research Laboratories P.O.Box 80.000, 5600 JA Eindhoven, The Netherlands', *Time*, pp. 100–103.
- Baliga, B. J., Syau, T. and Venkatraman, P. (1992) 'The Accumulation-Mode Field-Effect Transistor: A New Ultralow On-Resistance MOSFET', *IEEE Electron Device Letters*, 13(8), pp. 427–429. doi: 10.1109/55.192780.
- N. D. Arora, "MOSFET Models for VLSI Circuit Simulations: Theory and Practice," *Springer-Verlog Wien*, New York, 1993.
- Arora N. "Modeling Hot-Carrier Effects. In: MOSFET Models for VLSI Circuit Simulation". Computational Microelectronics, Springer, Vienna, 1993
- Omura, Y. *et al.* (1993) 'Quantum-Mechanical Effects on the Threshold Voltage of Ultrathin-

- SOI nMOSFET's', *IEEE Electron Device Letters*, 14(12), pp. 569–571. doi: 10.1109/55.260792.
- Schroeder D. “MOSFET Gate. In: Modelling of Interface Carrier Transport for Device Simulation”, Computational Microelectronics, Springer, Vienna, 1994.
- Takeuchi, K. and Fukuma, M. (1994) ‘Effects of the Velocity Saturated Region on MOSFET Characteristics’, *IEEE Transactions on Electron Devices*, 41(9), pp. 1623–1627. doi: 10.1109/16.310116.
- Bouhdada A, Bakkali S, and Touhami A. (1997) ‘Modelling of gate-induced drain leakage in relation to technological parameters and temperature’ *Microelectronics Reliability*, 37(4), pp. 649–652. doi: 10.1016/S0026-2714(96)00062-5.
- Y. Taur, and T. H. Ning, “Fundamentals of Modern VLSI Devices” Cambridge University Press, 1998.
- X. Zhou and W. Long, “A Novel Hetero-Material Gate (HMG) MOSFET for Deep-Submicron ULSI Technology,” *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2546-2548, 1998.
- Hareland, S. A. *et al.* (1998) ‘Computationally efficient models for quantization effects in MOS electron and hole accumulation layers’, *IEEE Transactions on Electron Devices*, 45(7), pp. 1487–1493. doi: 10.1109/16.701479.
- W. Long, H. Ou, J-M. Kuo, and K. K. Chin, “Dual-Material Gate (DMG) Field Effect Transistor,” *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 865–870, 1999.
- Xing Zhou, “Exploring the Novel Characteristics of Hetero-Material Gate Field-Effect Transistors with Gate-Material Engineering,” *IEEE Trans. Electron Device*, vol. 47, no.1, pp. 113-120, Jan. 2000.
- Chen, J. H., Wong, S. C. and Wang, Y. H. (2001) ‘An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET’, *IEEE Transactions on Electron Devices*, 48(7), pp. 1400–1405. doi: 10.1109/16.930658.
- Taur, Y. (2001) ‘Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs’, *IEEE Transactions on Electron Devices*. IEEE, 48(12), pp. 2861–2869. doi: 10.1109/16.974719.

- Pavanello, M. A., Martino, J. A. and Flandre, D. (2001) ‘Analog circuit design using graded-channel SOI nMOSFETs’, *Proceedings - 14th Symposium on Integrated Circuits and Systems Design, SBCCI 2001*, (158), pp. 130–135. doi: 10.1109/SBCCI.2001.953015.
- Wang, J. and Lundstrom, M. (2002) ‘Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?’, *Technical Digest - International Electron Devices Meeting*, pp. 707–710. doi: 10.1109/iedm.2002.1175936.
- J. Vasi, V. R. Rao, B. Cheng, and J. C. S. Woo, “Optimization and Realization of Sub-100-nm Channel Length Single Halo p-MOSFETs,” *IEEE TED*, vol. 49, no. 6, pp. 1077–1079, 2002, doi:10.1109/TED.2002.1003752.
- Lin, R. *et al.* (2002) ‘An adjustable work function technology using Mo gate for CMOS devices’, *IEEE Electron Device Letters*. IEEE, 23(1), pp. 49–51. doi: 10.1109/55.974809.
- Sung-Mo Kang, Yusuf Leblebici, “CMOS DIGITAL INTEGRATED CIRCUITS ANALYSIS & DESIGN” TATA McGRAW Hill EDITION, 2002
- Park Jong-Tae, Colinge J-P (2002). ‘Multiple-gate SOI MOSFETs: device design guidelines’. *IEEE Trans Electron Devices*, 49(12):2222–9.
- Yeo, Y. C., King, T. J. and Hu, C. (2003) ‘MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations’, *IEEE Transactions on Electron Devices*, 50(4), pp. 1027–1035. doi: 10.1109/TED.2003.812504.
- Jung-Hoon Rhew, “Physics and Simulation of Quasi-Ballistic Transport In Nanoscale Transistors,” *Ph.D. Thesis*, Purdue University, 2003, doi: 10.16309/j.cnki.issn.1007-1776.2003.03.004.
- Yeo, Y. C., King, T. J. and Hu, C. (2003) ‘MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations’, *IEEE Transactions on Electron Devices*, 50(4), pp. 1027–1035. doi: 10.1109/TED.2003.812504.
- Jiménez, D. *et al.* (2004) ‘Continuous analytic I-V model for surrounding-gate MOSFETs’, *IEEE Electron Device Letters*, 25(8), pp. 571–573. doi: 10.1109/LED.2004.831902.
- B. Meyerson, *Semico Impact Conference*, Taiwan, January 2004.
- Lowalekar, V. and Raghavan, S. (2004) ‘Etching of zirconium oxide, hafnium oxide, and

- hafnium silicates in dilute hydrofluoric acid solutions', *Journal of Materials Research*, 19(4), pp. 1149–1156. doi: 10.1557/JMR.2004.0149.
- Anurag Chaudhry and M. Jagadesh Kumar, "Controlling Short-channel Effects in Deep Submicron SOI MOSFETs for Improved Reliability: A Review", *IEEE Trans. on Device and Materials Reliability*, Vol.4, pp.99-109, 2004.
- Curatola, G., Fiori, G. and Iannaccone, G. (2004) 'Modelling and simulation challenges for nanoscale MOSFETs in the ballistic limit', *Solid-State Electronics*, 48(4), pp. 581–587. doi: 10.1016/j.sse.2003.09.029.
- Elgharbawy, W. M. and Bayoumi, M. A. (2005) 'Leakage sources and possible solutions in nanometer CMOS Technologies', *IEEE Circuits and Systems Magazine*. IEEE, 5(4), pp. 6–16. doi: 10.1109/MCAS.2005.1550165.
- Fuchs, E. *et al.* (2005) 'A new backscattering model giving a description of the quasi-ballistic transport in nano-MOSFET', *IEEE Transactions on Electron Devices*, 52(10), pp. 2280–2288. doi: 10.1109/TED.2005.856181.
- Eminente, S. *et al.* (2005) 'Understanding quasi-ballistic transport in nano-MOSFETs: Part II - Technology scaling along the ITRS', *IEEE Transactions on Electron Devices*, 52(12), pp. 2736–2743. doi: 10.1109/TED.2005.859566.
- Jong-Ho Lee (2005) 'DOUBLE-GATE FINFET DEVICE AND FABRICATING METHOD THEREOF' United States Patent', 2(12).
- Song, J. Y. *et al.* (2006) 'Design Optimization of Gate-All-Around ( GAA ) MOSFETs', 5(3), pp. 186–191.
- E. Grossar, M. Stucchi, K. Maex, W. Dehaene, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, 2006, doi: 10.1109/JSSC.2006.883344.
- Tsuchiya, H. *et al.* (2006) 'A quantum-corrected Monte Carlo study on quasi-ballistic transport in nanoscale MOSFETs', *IEEE Transactions on Electron Devices*, 53(12), pp. 2965–2971. doi: 10.1109/TED.2006.885672.
- B. G. Streetman, and S. K. Banerjee, *Solid State Electronic Devices*, Pearson Prentice Hall India, 2006.

- P. Nilsson, "Arithmetic Reduction of the Static Power Consumption in Nanoscale CMOS," *IEEE Int. Conf. on Electronics, Circuits and Systems*, pp. 656-659 2006.
- B. Sviličić, and A. Kraš, "CMOS technology: chalanges for future development", Pomorstvo, *Journal of Maritime Studies*, vol. 20, no. 2, pp. 97-104, 2006.
- B. H. Lee, J. Oh, H. H. Tseng, R. Jammy, and H. Huff, "Gate stack technology for nanoscale devices Scaling of the gate stack has been a key to enhancing the performance," *materials today*, vol. 9, no. 6, pp. 32–40, 2006, doi: 10.1016/S1369-7021(06)71541-3.
- Wang, L. (2006) 'QUANTUM MECHANICAL EFFECTS ON MOSFET SCALING LIMIT QUANTUM MECHANICAL EFFECTS ON MOSFET SCALING'.
- P. Packan, "Device and Circuit Interactions," *IEEE International Electron Device Meeting (IEDM '07) Short Course: Performance Boosters for Advanced CMOS Devices*, December 2007.
- S. M. Sze and Kwok K. Ng, "Physics of Semiconductor Devices, 3rd Edition " John Wiley & Sons, Inc, 2007.
- El Hamid, H. A., Iñíguez, B. and Roig Guitart, J. R. (2007) 'Analytical model of the threshold voltage and subthreshold swing of undoped cylindrical gate-all-around-based MOSFETs', *IEEE Transactions on Electron Devices*, 54(3), pp. 572–579. doi: 10.1109/TED.2006.890595.
- Xiao-ju, Z. *et al.* (2007) 'Corner effects in double-gate/gate-all-around MOSFETs' *Chin. Phys.*, vol. 16(3): 812-816, doi: 10.1088/1009-1963/16/3/042.
- Lin, S. H. *et al.* (2007) 'A rigorous surface-potential-based I-V model for undoped cylindrical nanowire MOSFETs', *2007 7th IEEE International Conference on Nanotechnology - IEEE-NANO 2007, Proceedings*, pp. 889–892. doi: 10.1109/NANO.2007.4601326.
- Yu, B. *et al.* (2007) 'Explicit continuous models for double-gate and surrounding-gate MOSFETs', *IEEE Transactions on Electron Devices*, 54(10), pp. 2715–2722. doi: 10.1109/TED.2007.904410.
- Ray, B. and Mahapatra, S. (2008) 'Modeling and analysis of body potential of cylindrical gate-all-around nanowire transistor', *IEEE Transactions on Electron Devices*, 55(9), pp. 2409–2416. doi: 10.1109/TED.2008.927669.

- M. Samson and M. B. Srinivas, "Analyzing N-Curve Metrics for Sub-threshold 65nm CMOS SRAM," *2008 8th IEEE Conference on Nanotechnology*, Arlington, TX, USA, pp. 25–28, 2008, doi: 10.1109/NANO.2008.16.
- Martinie, S., Munteanu, D., *et al.* (2008) 'New unified analytical model of backscattering coefficient from low- to high-field conditions in quasi-ballistic transport', *IEEE Electron Device Letters*, 29(12), pp. 1392–1394. doi: 10.1109/LED.2008.2007305.
- S. Martinie, G. Le Carval, D. Munteanu, S. Soliveres, and J. L. Autran, "Impact of ballistic and quasi-ballistic transport on performances of double-gate MOSFET-based circuits," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2443–2453, 2008, doi: 10.1109/TED.2008.927656.
- Kenji Natori. (2008) 'Compact modeling of the subthreshold characteristics of junctionless double-gate FETs including the source/drain extension regions', *Solid-State Electronics*. Elsevier, 156(December 2018), pp. 48–57. doi:10.1016/j.apsusc.2008.02.150.
- C. Hu, "Green Transistor as a Solution to the IC Power Crisis," in *Proc. 9th Int. Conf. Solid-State Int. Circuit Technol.*, pp. 16–20, 2008.
- Ghoggali, Z. *et al.* (2008) 'An analytical threshold voltage model for nanoscale', *Proceedings - 2008 3rd International Design and Test Workshop, IDT 2008*, 12(5), pp. 93–97. doi: 10.1109/IDT.2008.4802474.
- N-K. Cho, S-H. Choi, N-H. Kim, S-H. Kim and Y-S. Yu, "Continuous Analytic Current Voltage (I-V) Model for Long-Channel Doped Surrounding-Gate MOSFETs (SGMOSFETs) .," 2008 International Conference on Advanced Technologies for Communications, no. 1, pp. 315–318, 2008, doi:10.1109/ATC.2008.4760585.
- Tsormpatzoglou, A. *et al.* (2009) 'A compact drain current model of short-channel cylindrical gate-all-around MOSFETs', *Semiconductor Science and Technology*, 24(7). doi: 10.1088/0268-1242/24/7/075017.
- Lee, C. W. *et al.* (2009) 'Junctionless multigate field-effect transistor', *Applied Physics Letters*, 94(5), pp. 13–15. doi: 10.1063/1.3079411.

- Song, J. *et al.* (2009) ‘A review on compact modeling of multiple-gate MOSFETs’, *IEEE Transactions on Circuits and Systems I: Regular Papers*, 56(8), pp. 1858–1869. doi: 10.1109/TCSI.2009.2028416.
- Colinge, J. *et al.* (2010) ‘Nanowire transistors without junctions’, *Nature Nanotechnology*. Nature Publishing Group, (February). doi: 10.1038/nnano.2010.15.
- Colinge, J. P., Lee, C. W., Afzalian, A., *et al.* (2010) ‘Nanowire transistors without junctions’, *Nature Nanotechnology*. Nature Publishing Group, 5(3), pp. 225–229. doi: 10.1038/nnano.2010.15.
- Colinge, J. P., Lee, C. W., Ferain, I., *et al.* (2010) ‘Reduced electric field in junctionless transistors’, *Applied Physics Letters*, 96(7), pp. 23–26. doi: 10.1063/1.3299014.
- Kranti, A. *et al.* (2010) ‘Junctionless 6T SRAM cell’, *Electronics Letters*, 46(22), pp. 1491–1493. doi: 10.1049/el.2010.2736.
- Lee, C. *et al.* (2010) ‘High-Temperature Performance of Silicon Junctionless MOSFETs’, *IEEE Transactions on Electron Devices*. IEEE, 57(3), pp. 620–625. doi: 10.1109/TED.2009.2039093.
- Lee, C. W. *et al.* (2010) ‘Performance estimation of junctionless multigate transistors’, *Solid-State Electronics*. Elsevier Ltd, 54(2), pp. 97–103. doi: 10.1016/j.sse.2009.12.003.
- Tocci, G. (2010) “Performance estimation and Variability from Random Dopant Fluctuations in Multi-Gate Field Effect Transistors: a Simulation Study”. Available at: <http://kth.diva-portal.org/smash/record.jsf?pid=diva2:515805>.
- Martinez, A. *et al.* (2010) ‘Variability in Si nanowire MOSFETs due to the combined effect of interface roughness and random dopants: A fully three-dimensional NEGF simulation study’, *IEEE Transactions on Electron Devices*. IEEE, 57(7), pp. 1626–1635. doi: 10.1109/TED.2010.2048405.
- Choi, S. J. *et al.* (2011) ‘Sensitivity of threshold voltage to nanowire width variation in junctionless transistors’, *IEEE Electron Device Letters*. IEEE, 32(2), pp. 125–127. doi: 10.1109/LED.2010.2093506.
- Dura, J. *et al.* (2011) ‘Analytical model of drain current in nanowire MOSFETs including

- quantum confinement, band structure effects and quasi-ballistic transport: Device to circuit performances analysis', *International Conference on Simulation of Semiconductor Processes and Devices, SISPAD*. IEEE, pp. 43–46. doi: 10.1109/SISPAD.2011.6035045.
- Colinge, J. P. *et al.* (2011a) 'Junctionless Nanowire Transistor (JNT): Properties and design guidelines', *Solid-State Electronics*, 65–66(1), pp. 33–37. doi: 10.1016/j.sse.2011.06.004.
- Colinge, J. P. *et al.* (2011b) 'Junctionless Nanowire Transistor (JNT): Properties and design guidelines', *Solid-State Electronics*, 65–66(1), pp. 33–37. doi: 10.1016/j.sse.2011.06.004.
- Duarte, J. P., Choi, S. J. and Choi, Y. K. (2011) 'A full-range drain current model for double-gate junctionless transistors', *IEEE Transactions on Electron Devices*, 58(12), pp. 4219–4225. doi: 10.1109/TED.2011.2169266.
- Gnani, E. *et al.* (2011) 'Theory of the junctionless nanowire FET', *IEEE Transactions on Electron Devices*, 58(9), pp. 2903–2910. doi: 10.1109/TED.2011.2159608.
- Sallese, J. M. *et al.* (2011) 'Charge-based modeling of junctionless double-gate field-effect transistors', *IEEE Transactions on Electron Devices*, 58(8), pp. 2628–2637. doi: 10.1109/TED.2011.2156413.
- Singh, P. *et al.* (2011) 'Gate-all-around junctionless nanowire mosfet with improved low-frequency noise behavior', *IEEE Electron Device Letters*. IEEE, 32(12), pp. 1752–1754. doi: 10.1109/LED.2011.2169645.
- Ferain, I., Colinge, C. A. and Colinge, J. P. (2011) 'Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors', *Nature*, 479(7373), pp. 310–316. doi: 10.1038/nature10676.
- Barraud, S. *et al.* (2012) 'Scaling of trigate junctionless nanowire MOSFET with gate length down to 13 nm', *IEEE Electron Device Letters*, 33(9), pp. 1225–1227. doi: 10.1109/LED.2012.2203091.
- Mysore, O. (2012) 'Compact modeling of circuits and devices in Verilog-A'. Available at: <http://dspace.mit.edu/handle/1721.1/77441>.



- K. Dhanumjaya and M. Sudha, "Cell Stability Analysis of Conventional 6T Dynamic 8T SRAM Cell in 45NM Technology," *International Journal of VLSI design & Communication Systems (VLSICS)*, vol. 3, no. 2, pp. 41–51, 2012, doi: 0.5121/vlsic.2012.3204.
- Chiang, T. K. (2012) 'A new quasi-2-D threshold voltage model for short-channel junctionless cylindrical surrounding gate (JLCSG) MOSFETs', *IEEE Transactions on Electron Devices*, 59(11), pp. 3127–3129. doi: 10.1109/TED.2012.2212904.
- Duarte, J. P. *et al.* (2012) 'A nonpiecewise model for long-channel junctionless cylindrical nanowire FETs', *IEEE Electron Device Letters*, 33(2), pp. 155–157. doi: 10.1109/LED.2011.2174770.
- Goto, K. I. *et al.* (2012) 'Mobility and screening effect in heavily doped accumulation-mode metal-oxide-semiconductor field-effect transistors', *Applied Physics Letters*, 101(7), pp. 1–3. doi: 10.1063/1.4745604.
- Gundapaneni, S. *et al.* (2012) 'Effect of band-to-band tunneling on junctionless transistors', *IEEE Transactions on Electron Devices*, 59(4), pp. 1023–1029. doi: 10.1109/TED.2012.2185800.
- Lou, H. *et al.* (2012) 'A junctionless nanowire transistor with a dual-material gate', *IEEE Transactions on Electron Devices*, 59(7), pp. 1829–1836. doi: 10.1109/TED.2012.2192499.
- Te-Kuang Chiang. (2012) 'A Quasi-Two-Dimensional Threshold Voltage Model for Short-Channel Junctionless', *IEEE Transactions on Electron Devices*, 59(9), pp. 2284–2289.
- Najmzadeh, M. *et al.* (2012) 'Accumulation-mode gate-all-around si nanowire nMOSFETs with sub-5 nm cross-section and high uniaxial tensile strain', *Solid-State Electronics*. Elsevier Ltd, 74, pp. 114–120. doi: 10.1016/j.sse.2012.04.021.
- Najmzadeh, Mohammad *et al.* (2012) 'Local Volume Depletion/Accumulation in GAA Si Nanowire Junctionless nMOSFETs', *IEEE Transactions on Electron Devices*, 59(12), pp. 3519–3526. doi: 10.1109/TED.2012.2220363.

- Rudenko, T. *et al.* (2012) ‘Mobility enhancement effect in heavily doped junctionless nanowire silicon-on-insulator metal-oxide-semiconductor field-effect transistors’, *Applied Physics Letters*, 101(21). doi: 10.1063/1.4767353.
- Liu, L. L. and Li, Z. C. (2012) ‘A quantum-confinement model for surrounding-gate MOSFETS from subthreshold to strong-inversion regions’, *Science China Information Sciences*, 55(10), pp. 2399–2408. doi: 10.1007/s11432-012-4641-4.
- Trevisoli, R. D. *et al.* (2012) ‘Surface-potential-based drain current analytical model for triple-gate junctionless nanowire transistors’, *IEEE Transactions on Electron Devices*. IEEE, 59(12), pp. 3510–3518. doi: 10.1109/TED.2012.2219055.
- Darbandy G (2012). Compact modeling of gate tunneling leakage current in advanced nanoscale SOI MOSFETS Ph.D, Department of Electronic, Electrical and Automatic Control Engineering. Tarragona: Universitat rovera i virgili.
- Chen, Y. *et al.* (2013b) ‘Junctionless MOSFETs with laterally graded-doping channel for analog/RF applications’, *Journal of Computational Electronics*, 12(4), pp. 757–764. doi: 10.1007/s10825-013-0478-3.
- Gadhe, A. and Shirode, U. (2013) ‘Read stability and Write ability analysis of different SRAM cell structures’, 3(1), pp. 1073–1078.
- Lee, G., Jang, J. S. and Choi, W. Y. (2013) ‘Dual-dielectric-constant spacer hetero-gate-dielectric tunneling field-effect transistors’, *Semiconductor Science and Technology*, 28(5). doi: 10.1088/0268-1242/28/5/052001.
- Koziel, S. *et al.* (2013) ‘Reliable reduced cost modeling and design optimization of microwave filters using co-kriging’, *International Journal of Numerical Modelling*, 26(April 2011), pp. 493–505. doi: 10.1002/jnm.
- Chiang, T. and Liou, J. J. (2013) ‘AN ANALYTICAL SUBTHRESHOLD CURRENT / SWING MODEL FOR JUNCTIONLESS CYLINDRICAL NANOWIRE FETS’, 26(December), pp. 157–173. doi: 10.2298/FUEE1303157C.
- Gao, H. W. and Chiang, T. K. (2013) ‘A novel scaling theory for fully-depleted omega-gate ( $\Omega$ G) MOSFETs’, *Proceedings of International Conference on ASIC*. doi: 10.1109/ASICON.2013.6811953.

- Intekhab Amin, S. and Sarin, R. K. (2013) 'Junctionless transistor: A review', *IET Conference Publications*, 2013(CP646), pp. 432–439. doi: 10.1049/cp.2013.2625.
- Jazaeri, F. *et al.* (2013) 'Analytical model for ultra-thin body junctionless symmetric double gate MOSFETs in subthreshold regime', *Solid-State Electronics*, 82, pp. 103–110. doi: 10.1016/j.sse.2013.02.001.
- Jazaeri, F., Barbut, L. and Sallese, J. M. (2013) 'Modeling and design space of junctionless symmetric DG MOSFETs with long channel', *IEEE Transactions on Electron Devices*, 60(7), pp. 2120–2127. doi: 10.1109/TED.2013.2261073.
- Jeon, Dae Young *et al.* (2013a) 'Effects of channel width variation on electrical characteristics of tri-gate Junctionless transistors', *Solid-State Electronics*, 81, pp. 58–62. doi: 10.1016/j.sse.2013.01.002.
- Jeon, Dae Young *et al.* (2013b) 'Low-temperature electrical characterization of junctionless transistors', *Solid-State Electronics*, 80, pp. 135–141. doi: 10.1016/j.sse.2012.10.018.
- Jeon, D. Y. *et al.* (2013) 'Revisited parameter extraction methodology for electrical characterization of junctionless transistors', *Solid-State Electronics*. Elsevier Ltd, 90, pp. 86–93. doi: 10.1016/j.sse.2013.02.047.
- Jin, X., Liu, X., Kwon, H. I., *et al.* (2013) 'A subthreshold current model for nanoscale short channel junctionless MOSFETs applicable to symmetric and asymmetric double-gate structure', *Solid-State Electronics*, 82, pp. 77–81. doi: 10.1016/j.sse.2013.02.004.
- Jin, X., Liu, X., Wu, M., *et al.* (2013) 'A unified analytical continuous current model applicable to accumulation mode (junctionless) and inversion mode MOSFETs with symmetric and asymmetric double-gate structures', *Solid-State Electronics*. Elsevier Ltd, 79, pp. 206–209. doi: 10.1016/j.sse.2012.08.003.
- Jin, X. S. *et al.* (2013) 'A continuous current model of accumulation mode (Junctionless) cylindrical surrounding-gate nanowire MOSFETs', *Chinese Physics Letters*, 30(3). doi: 10.1088/0256-307X/30/3/038502.
- Lee, Jong Ho *et al.* (2013) 'A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping

- concentration', *Semiconductor Science and Technology*, 28(1). doi: 10.1088/0268-1242/28/1/015002.
- Kim, T. K. *et al.* (2013) 'First demonstration of junctionless accumulation-mode bulk FinFETs with robust junction isolation', *IEEE Electron Device Letters*. IEEE, 34(12), pp. 1479–1481. doi: 10.1109/LED.2013.2283291.
- Lee, Jong Ho *et al.* (2013) 'A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping concentration', *Semiconductor Science and Technology*, 28(1). doi: 10.1088/0268-1242/28/1/015002.
- Li, C. *et al.* (2013) 'Subthreshold behavior models for nanoscale short-channel junctionless cylindrical surrounding-gate mosfets', *IEEE Transactions on Electron Devices*. IEEE, 60(11), pp. 3655–3662. doi: 10.1109/TED.2013.2281395.
- Moon, D. Il *et al.* (2013) 'Investigation of silicon nanowire gate-all-around junctionless transistors built on a bulk substrate', *IEEE Transactions on Electron Devices*, 60(4), pp. 1355–1360. doi: 10.1109/TED.2013.2247763.
- Lee, Jong Ho *et al.* (2013) 'A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping concentration', *Semiconductor Science and Technology*, 28(1). doi: 10.1088/0268-1242/28/1/015002.
- Park, S. J. *et al.* (2013) 'Back biasing effects in tri-gate junctionless transistors', *Solid-State Electronics*. Elsevier Ltd, 87, pp. 74–79. doi: 10.1016/j.sse.2013.06.004.
- Tang, X. *et al.* (2013) 'A new fabrication method for elevated source/drain junctionless transistors', *Journal of Physics D: Applied Physics*, 46(16). doi: 10.1088/0022-3727/46/16/165101.
- Lee, Jong Ho *et al.* (2013) 'A continuous current model of ultra-thin cylindrical surrounding-gate inversion-mode Si nanowire nMOSFETs considering a wide range of body doping concentration', *Semiconductor Science and Technology*, 28(1). doi: 10.1088/0268-1242/28/1/015002.

- Trevisoli, R. *et al.* (2013) 'Analysis of the leakage current in junctionless nanowire transistors', *Applied Physics Letters*, 103(20), pp. 2013–2016. doi: 10.1063/1.4829465.
- Ghosh, D., Parihar, M. S. and Kranti, A. (2013) 'RF performance of ultra low power junctionless MOSFETs', *Asia-Pacific Microwave Conference Proceedings, APMC*. IEEE, pp. 787–789. doi: 10.1109/APMC.2013.6694932.
- Baruah, R. K. and Paily, R. P. (2014) 'A dual-material gate junctionless transistor with high- $\kappa$  spacer for enhanced analog performance', *IEEE Transactions on Electron Devices*, 61(1), pp. 123–128. doi: 10.1109/TED.2013.2292852.
- Choi, J. H. *et al.* (2014) 'Origin of device performance enhancement of junctionless accumulation-mode (JAM) bulk FinFETs with high- $\kappa$  gate spacers', *IEEE Electron Device Letters*, 35(12), pp. 1182–1184. doi: 10.1109/LED.2014.2364093.
- Sarkar, C. K. and Member, S. (2014) 'Effect of Source / Drain Lateral Straggle on Distortion and Intrinsic Performance of Asymmetric Underlap DG-MOSFETs', *IEEE Journal of the Electron Devices Society*. IEEE, 2(6), pp. 135–144. doi: 10.1109/JEDS.2014.2342613.
- Cong, L. *et al.* (2014) 'Quasi-two-dimensional threshold voltage model for junctionless cylindrical surrounding gate metal-oxide-semiconductor field-effect transistor with dual-material gate', *Chinese Physics B*, 23(1). doi: 10.1088/1674-1056/23/1/018501.
- Ghosh, B., Akram, M. W. and Bal, P. (2014) 'Hetero-gate-dielectric double gate junctionless transistor (HGJLT) with reduced band-to-band tunnelling effects in subthreshold regime Hetero-gate-dielectric double gate junctionless transistor (HGJLT) with reduced band-to-band tunnelling effects in s'. doi: 10.1088/1674-4926/35/6/064001.
- Holtij, T. *et al.* (2014) 'Compact model for short-channel junctionless accumulation mode double gate MOSFETs', *IEEE Transactions on Electron Devices*, 61(2), pp. 288–299. doi: 10.1109/TED.2013.2281615.
- Li, C., Zhuang, Y. Q., *et al.* (2014) 'A two-dimensional analytical subthreshold behavior model for junctionless dual-material cylindrical surrounding-gate MOSFETs', *Chinese Physics B*, 23(3). doi: 10.1088/1674-1056/23/3/038502.
- Pratap, Y. *et al.* (2014) 'An analytical subthreshold current modeling of cylindrical gate all

- around (CGAA) MOSFET incorporating the influence of device design engineering', *Microelectronics Journal*. Elsevier, 45(4), pp. 408–415. doi: 10.1016/j.mejo.2014.01.015.
- Li, C., Zhuang, Y., *et al.* (2014) 'Subthreshold behavior models for short-channel junctionless tri-material cylindrical surrounding-gate MOSFET', *Microelectronics Reliability*. Elsevier Ltd, 54(6–7), pp. 1274–1281. doi: 10.1016/j.microrel.2014.02.007.
- Mangla, A. *et al.* (2014) 'Modeling the channel charge and potential in quasi-ballistic nanoscale double-gate MOSFETs', *IEEE Transactions on Electron Devices*, 61(8), pp. 2640–2646. doi: 10.1109/TED.2014.2327255.
- T. Chiang, "A Novel Scaling Theory for Fully Depleted, Multiple-Gate MOSFET, Including Effective Number of Gates (ENGs)," in *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 631-633, Feb. 2014, doi: 10.1109/TED.2013.2294192.
- François Lime, Oana Moldovan, Benjamin Iñiguez. (2014) 'A Compact Explicit Model for Long-Channel Part I : DC Characteristics', 61(9), pp. 3036–3041.
- Yu, Y. S. (2014) 'A unified analytical current model for N-and P-type accumulation-mode (junctionless) surrounding-gate nanowire FETs', *IEEE Transactions on Electron Devices*, 61(8), pp. 3007–3010. doi: 10.1109/TED.2014.2329916.
- Jazaeri, F., Barbut, L. and Sallese, J. M. (2014) 'Modeling asymmetric operation in double-gate junctionless FETs by means of symmetric devices', *IEEE Transactions on Electron Devices*. IEEE, 61(12), pp. 3962–3970. doi: 10.1109/TED.2014.2361358.
- Pratap, Y. *et al.* (2014a) 'An analytical subthreshold current modeling of cylindrical gate all around (CGAA) MOSFET incorporating the influence of device design engineering', *Microelectronics Journal*. Elsevier, 45(4), pp. 408–415. doi: 10.1016/j.mejo.2014.01.015.
- Kumari, V. *et al.* (2015) 'Theoretical investigation of dual material junctionless double gate transistor for analog and digital performance', *IEEE Transactions on Electron Devices*, 62(7), pp. 2098–2105. doi: 10.1109/TED.2015.2433951.
- Pratap, Y. *et al.* (2015) 'Localized Charge-Dependent Threshold Voltage Analysis of Gate-Material-Engineered Junctionless Nanowire Transistor', *IEEE Transactions on Electron*

- Devices*, 62(8), pp. 2598–2605. doi: 10.1109/TED.2015.2441777.
- Chiang, T. K. (2015) ‘A novel quasi-3D interface-trapped-charge-degraded threshold voltage model for omega-gate ( $\Omega\{G\}$ ) MOSFETs’, *IEEE Transactions on Device and Materials Reliability*, 15(1), pp. 35–39. doi: 10.1109/TDMR.2014.2371050.
- Mukherjee, S. *et al.* (2015) ‘Impact of lateral straggle on analog and digital circuit performance using independently driven underlap DG-MOSFET’, 46, pp. 1082–1090.
- Holtij, T., Kloes, A. and Iñíguez, B. (2015) ‘3-D compact model for nanoscale junctionless triple-gate nanowire MOSFETs, including simple treatment of quantization effects’, *Solid-State Electronics*, 112, pp. 85–98. doi: 10.1016/j.sse.2015.02.002.
- Hur, J. *et al.* (2015) ‘A Core Compact Model for Multiple-Gate Junctionless FETs’, *IEEE Transactions on Electron Devices*, 62(7), pp. 2285–2291. doi: 10.1109/TED.2015.2428711.
- Hwang, B. W., Yang, J. W. and Lee, S. H. (2015) ‘Explicit analytical current-voltage model for double-gate junctionless transistors’, *IEEE Transactions on Electron Devices*. IEEE, 62(1), pp. 171–177. doi: 10.1109/TED.2014.2371075.
- Huang, J. *et al.* (2015) ‘A surface potential based quasi-ballistic double gate MOSFET model’, *Proceedings of the 2015 IEEE International Conference on Electron Devices and Solid-State Circuits, EDSSC 2015*, (3), pp. 467–470. doi: 10.1109/EDSSC.2015.7285152.
- Kumar, M. P. V. *et al.* (2015) ‘Impacts of the Shell Doping Profile on the Electrical Characteristics of Junctionless FETs’, *IEEE Transactions on Electron Devices*, 62(11), pp. 3541–3546. doi: 10.1109/TED.2015.2471797.
- Lee, Y. J. *et al.* (2015) ‘A novel junctionless FinFET structure with sub-5nm shell doping profile by molecular monolayer doping and microwave annealing’, *Technical Digest - International Electron Devices Meeting, IEDM, 2015-(February)*, pp. 32.7.1-32.7.4. doi: 10.1109/IEDM.2014.7047158.
- Fan, J. *et al.* (2015) ‘Insight into gate-induced drain leakage in silicon nanowire transistors’, *IEEE Transactions on Electron Devices*, 62(1), pp. 213–219. doi: 10.1109/TED.2014.2371916.
- Gupta, S. K. (2015) ‘Threshold voltage model of junctionless cylindrical surrounding gate

- MOSFETs including fringing field effects', *Superlattices and Microstructures*. Elsevier Ltd, 88, pp. 188–197. doi: 10.1016/j.spmi.2015.09.001.
- Ghosh, D. and Kranti, A. (2015) 'Impact of channel doping and spacer architecture on analog/RF performance of low power junctionless MOSFETs', *Semiconductor Science and Technology*. IOP Publishing, 30(1). doi: 10.1088/0268-1242/30/1/015002.
- Baruah, R. K. and Paily, R. P. (2016) 'A surface-potential based drain current model for short-channel symmetric double-gate junctionless transistor', *Journal of Computational Electronics*. Springer US, 15(1), pp. 45–52. doi: 10.1007/s10825-015-0723-z.
- Sai, G., Chakraborty, S. and Das, R. (2016) 'Impact of Lateral Straggle on the Analog / RF Performance of Asymmetric Gate Stack Double Gate MOSFET', *Superlattices and Microstructures*, 97, pp. 477–488.
- G. Saini, SudhanshuChoudhary "Improving the performance of SRAMs using asymmetric junctionless accumulation mode (JAM) FinFETs," *Microelectronics Journal*, vol. 58, pp. 1-8, 2016, doi: 10.1016/j.mejo.2016.10.004.
- Kumar, M. *et al.* (2016) 'Analytical model of threshold voltage degradation due to localized charges in gate material engineered Schottky barrier cylindrical GAA MOSFETs', *Semiconductor Science and Technology*. IOP Publishing, 31(10). doi: 10.1088/0268-1242/31/10/105013.
- Hur, J. *et al.* (2016) 'Comprehensive Analysis of Gate-Induced Drain Leakage in Vertically Stacked Nanowire FETs: Inversion-Mode Versus Junctionless Mode', *IEEE Electron Device Letters*. IEEE, 37(5), pp. 541–544. doi: 10.1109/LED.2016.2540645.
- Te-Kuang Chiang. (2016) 'A New Threshold Voltage Model for Short-Channel Junctionless Inverted T-Shaped Gate FETs (JLITFET)', 15(3), pp. 442–447. doi: 10.1109/TNANO.2016.2539284.
- Jeong, S. *et al.* (2016) 'Solid-State Electronics Behavior of subthreshold conduction in junctionless transistors', 124, pp. 58–63.
- Sahay, S. *et al.*, (2016) 'Controlling L-BTBT and Volume Depletion in', *IEEE Transactions on Electron Devices*. IEEE, 63(9), pp. 3790–3794.



- Kumar, M. J. and Sahay, S. (2016) 'Controlling BTBT-Induced Parasitic BJT Action in Junctionless FETs Using a Hybrid Channel', *IEEE Transactions on Electron Devices*. IEEE, 63(8), pp. 3350–3353. doi: 10.1109/TED.2016.2577050.
- Kumar, S. *et al.* (2016) 'A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors with a SiO<sub>2</sub>/High-k Stacked Gate-Oxide Structure', *IEEE Transactions on Electron Devices*, 63(8), pp. 3291–3299. doi: 10.1109/TED.2016.2572610.
- Pratap, Y. *et al.* (2016) 'Gate-Material-Engineered Junctionless Nanowire Transistor (JNT) with Vacuum Gate Dielectric for Enhanced Hot-Carrier Reliability', *IEEE Transactions on Device and Materials Reliability*. IEEE, 16(3), pp. 360–369. doi: 10.1109/TDMR.2016.2583262.
- Goel Ekta, Kumar Sanjay, Singh Kunal, Singh Balraj, Kumar Mirgander, Jit Satyabrata (2016). 2-D analytical modeling of threshold voltage for graded-channel dual-material double-gate MOSFETs. *IEEE Trans Electron Devices*, 63 (3):966–73.
- Sahay, S. and Kumar, M. J. (2016a) 'Insight into Lateral Band-to-Band-Tunneling in Nanowire Junctionless FETs', *IEEE Transactions on Electron Devices*, 63(10), pp. 4138–4142. doi: 10.1109/TED.2016.2601239.
- Sahay, S. and Kumar, M. J. (2016b) 'Insight into Lateral Band-to-Band-Tunneling in Nanowire Junctionless FETs', *IEEE Transactions on Electron Devices*. IEEE, 63(10), pp. 4138–4142. doi: 10.1109/TED.2016.2601239.
- Sahay, S. and Kumar, M. J. (2016c) 'Realizing Efficient Volume Depletion in SOI Junctionless FETs', *IEEE Journal of the Electron Devices Society*. IEEE, 4(3), pp. 110–115. doi: 10.1109/JEDS.2016.2532965.
- Hur, J. *et al.* (2016) 'Comprehensive Analysis of Gate-Induced Drain Leakage in Vertically Stacked Nanowire FETs: Inversion-Mode Versus Junctionless Mode', *IEEE Electron Device Letters*. IEEE, 37(5), pp. 541–544. doi: 10.1109/LED.2016.2540645.
- Mitra, S. K., Goswami, R. and Bhowmick, B. (2016) 'A hetero-dielectric stack gate SOI-TFET with back gate and its application as a digital inverter', *Superlattices and Microstructures*. Elsevier Ltd, 92, pp. 37–51. doi: 10.1016/j.spmi.2016.01.040.

- Singh, B., Gola, D., Singh, K., Goel, E., Kumar, S., *et al.* (2016) ‘Analytical Modeling of Channel Potential and Threshold Voltage of Double-Gate Junctionless FETs with a Vertical Gaussian-Like Doping Profile’, *IEEE Transactions on Electron Devices*, 63(6), pp. 2299–2305. doi: 10.1109/TED.2016.2556227.
- Sharma, A. *et al.* (2016) ‘Effect of high-k and vacuum dielectrics as gate stack on a junctionless cylindrical surrounding gate (JL-CSG) MOSFET’, *Solid-State Electronics*. Elsevier Ltd, 123, pp. 26–32. doi: 10.1016/j.sse.2016.05.016.
- Singh, B. *et al.* (2016) ‘Dielectric pocket double gate junctionless FET: a new MOS structure with improved subthreshold characteristics for low power VLSI applications’, *Journal of Computational Electronics*. Springer US, 15(2), pp. 502–507. doi: 10.1007/s10825-016-0808-3.
- Trivedi, N., Kumar, M., Haldar, S., Deswal, S. S., *et al.* (2016) ‘Analytical modeling simulation and characterization of short channel Junctionless Accumulation Mode Surrounding Gate (JLAMSG) MOSFET for improved analog/RF performance’, *Superlattices and Microstructures*, 100, pp. 1263–1275. doi: 10.1016/j.spmi.2016.11.009.
- Trivedi, N., Kumar, M., Haldar, S., Deswal, S S, *et al.* (2016) ‘Superlattices and Microstructures Analytical modeling simulation and characterization of short channel Junctionless Accumulation Mode Surrounding Gate (JLAMSG ) MOSFET for improved analog / RF performance’, *Superlattices and Microstructures*. Elsevier Ltd, 100, pp. 1263–1275. doi: 10.1016/j.spmi.2016.11.009.
- Yesayan, A., Jazaeri, F. and Sallese, J. M. (2016) ‘Charge-Based Modeling of Double-Gate and Nanowire Junctionless FETs Including Interface-Trapped Charges’, *IEEE Transactions on Electron Devices*, 63(3), pp. 1368–1374. doi: 10.1109/TED.2016.2521359.
- Sahay, S. and Kumar, M. J. (2017a) ‘Diameter dependence of leakage current in nanowire junctionless field effect transistors’, *IEEE Transactions on Electron Devices*. IEEE, 64(3), pp. 1330–1335. doi: 10.1109/TED.2016.2645640.
- Sahay, S. and Kumar, M. J. (2017b) ‘Physical Insights into the Nature of Gate-Induced Drain Leakage in Ultrashort Channel Nanowire FETs’, *IEEE Transactions on Electron Devices*. IEEE, 64(6), pp. 2604–2610. doi: 10.1109/TED.2017.2688134.

- Sahay, S. and Kumar, M. J. (2017c) 'Symmetric Operation in an Extended Back Gate JLFET for Scaling to the 5-nm Regime Considering Quantum Confinement Effects', *IEEE Transactions on Electron Devices*. IEEE, 64(1), pp. 21–27. doi: 10.1109/TED.2016.2628763.
- Gupta, M. and Kranti, A. (2017) 'Variation of Threshold Voltage with Temperature in Impact Ionization-Induced Steep Switching Si and Ge Junctionless MOSFETs', *IEEE Transactions on Electron Devices*. IEEE, 64(5), pp. 2061–2066. doi: 10.1109/TED.2017.2679218.
- Oproglidis, T. A. *et al.* (2017) 'Analytical Drain Current Compact Model in the Depletion Operation Region of Short-Channel Triple-Gate Junctionless Transistors', *IEEE Transactions on Electron Devices*, 64(1), pp. 66–72. doi: 10.1109/TED.2016.2632753.
- Sahay, S. *et al.* (2017) 'Nanotube Junctionless FET: Proposal, Design, and Investigation', 64(4), pp. 1851–1856.
- Wang, Y. *et al.* (2017) 'Graded-channel junctionless dual-gate MOSFETs for radiation tolerance', *Japanese Journal of Applied Physics*, 56(12). doi: 10.7567/JJAP.56.124201.
- Chauhan, R. *et al.* (2017) 'A Comparative study of Junctionless dual material double gate Silicon on Insulator (SOI) and Silicon on Nothing (SON) MOSFET', *2017 4th International Conference on Power, Control and Embedded Systems, ICPCES 2017*, 2017-Janua, pp. 1–7. doi: 10.1109/ICPCES.2017.8117648.
- Singh, B. *et al.* (2017) 'Analytical modeling of subthreshold characteristics of ion-implanted symmetric double gate junctionless field effect transistors', *Materials Science in Semiconductor Processing*. Elsevier, 58(August 2016), pp. 82–88. doi: 10.1016/j.mssp.2016.10.051.
- Rewari, S. *et al.* (2017) 'Gate-Induced Drain Leakage Reduction in Cylindrical Dual-Metal Hetero-Dielectric Gate All Around MOSFET', *IEEE Transactions on Electron Devices*. IEEE, 65(1), pp. 3–10. doi: 10.1109/TED.2017.2771814.
- Tayal, S. and Nandi, A. (2017) 'Study of 6T SRAM cell using High- K gate dielectric based junctionless silicon nanotube FET', *Superlattices and Microstructures*, 112.

- S. Guin, M. Sil and A. Mallik, "Comparison of Logic Performance of CMOS Circuits Implemented With Junctionless and Inversion-Mode FinFETs," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 953-959, 2017, doi: 10.1109/TED.2017.2655541.
- Jaiswal, N. and Kranti, A. (2018) 'A Model for Gate-Underlap-Dependent Short-Channel Effects in Junctionless MOSFET', *IEEE Transactions on Electron Devices*. IEEE, 65(3), pp. 881–887. doi: 10.1109/TED.2018.2796602.
- Kumari, V. *et al.* (2018a) 'Empirical model for nonuniformly doped symmetric double-gate junctionless transistor', *IEEE Transactions on Electron Devices*. IEEE, 65(1), pp. 314–321. doi: 10.1109/TED.2017.2776607.
- Kumari, V. *et al.* (2018b) 'Study of Gaussian Doped Double Gate JunctionLess (GD-DG-JL) transistor including source drain depletion length: Model for sub-threshold behavior', *Superlattices and Microstructures*. Elsevier Ltd, 113, pp. 57–70. doi: 10.1016/j.spmi.2017.09.049.
- Tayal, S. and Nandi, A. (2018) 'Performance analysis of junctionless DG-MOSFET-based 6T-SRAM with gate-stack configuration', *Micro & Nano Letters*, 13, pp. 838–841. doi: 10.1049/mnl.2017.0702.
- B. Alorda and G. Torrens, "6T CMOS SRAM Stability in Nanoelectronic Era : From Metrics to Built-in Monitoring" 2018, doi: 10.5772/intechopen.73539
- Sachdeva N, Vashishath M, Bansal PK. (2018) 'Effect of gate work- function on gate induced drain leakage of MOSFETs'. *IJCEM*, 21(1):11–6.
- Kumar, A. and Tiwari, P. K. (2018) 'An Explicit Unified Drain Current Model for Silicon-Nanotube-Based Ultrathin Double Gate-All-Around MOSFETs', *IEEE Transactions on Nanotechnology*. IEEE, 17(6), pp. 1224–1234. doi: 10.1109/TNANO.2018.2870723.
- Shalchian, M., Jazaeri, F. and Sallese, J. M. (2018) 'Charge-Based Model for Ultrathin Junctionless DG FETs, Including Quantum Confinement', *IEEE Transactions on Electron Devices*. IEEE, 65(9), pp. 4009–4014. doi: 10.1109/TED.2018.2854905.
- Tayal, S. and Nandi, A. (2018) 'Performance analysis of junctionless DG-MOSFET-based 6T-SRAM with gate-stack configuration', 13, pp. 838–841. doi: 10.1049/mnl.2017.0702.

- Bae, M. S. and Yun, I. (2019) 'Compact modeling of the subthreshold characteristics of junctionless double-gate FETs including the source/drain extension regions', *Solid-State Electronics*. Elsevier, 156(March), pp. 48–57. doi: 10.1016/j.sse.2019.03.064.
- Patel, J. *et al.* (2019) 'Performance improvement of nano wire TFET by hetero-dielectric and hetero-material : At device and circuit level', *IEEE TED*, 85(June 2018), pp. 72–82.
- Murnal, V. and Vijaya, C. (2019) 'A Quasi-Ballistic Drain current model with Positional Scattering Dependency applicable for Nanoscale DG MOSFETs', *Proceedings of 2019 3rd IEEE International Conference on Electrical, Computer and Communication Technologies, ICECCT 2019*. IEEE, (1), pp. 1–5. doi: 10.1109/ICECCT.2019.8869340.
- Gola, D. *et al.* (2019) 'Static and quasi-static drain current modeling of tri-gate junctionless transistor with substrate bias-induced effects', *IEEE Transactions on Electron Devices*. IEEE, 66(7), pp. 2876–2883. doi: 10.1109/TED.2019.2915294.
- Bousari, N. B., Anvarifard, M. K. and Haji-Nasiri, S. (2019) 'Improving the electrical characteristics of nanoscale triple-gate junctionless FinFET using gate oxide engineering', *AEU - International Journal of Electronics and Communications*. Elsevier GmbH, 108, pp. 226–234. doi: 10.1016/j.aeue.2019.06.017.
- Goel, A. *et al.* (2019) 'Shallow Extension Engineered Dual Material Surrounding Gate (SEEDM-SG) MOSFET for improved gate leakages, analysis of circuit and noise performance', *AEU - International Journal of Electronics and Communications*. Elsevier GmbH, 111, p. 152924. doi: 10.1016/j.aeue.2019.152924.
- Priya, G. L. and Balamurugan, N. B. (2019) 'New dual material double gate junctionless tunnel FET: Subthreshold modeling and simulation', *AEU - International Journal of Electronics and Communications*, 99, pp. 130–138. doi: 10.1016/j.aeue.2018.11.037.
- Gupta, M. and Kranti, A. (2019) 'Bi-Directional Junctionless Transistor for Logic and Memory Applications', *IEEE Transactions on Electron Devices*. IEEE, 66(10), pp. 4446–4452. doi: 10.1109/TED.2019.2934191.
- Jaiswal, N. and Kranti, A. (2019) 'Modeling Short-Channel Effects in Core – Shell'. IEEE, 66(1), pp. 292–299.
- Banerjee, P. and Sarkar, S. K. (2019) 'Analysis of short channel characteristics in graded

- channel dual-material elliptical gate-all-around (GC DM EGAA) MOSFET', *Semiconductor Science and Technology*. IOP Publishing, 34(3). doi: 10.1088/1361-6641/aafc86.
- Duksh, Y. S. *et al.* (2020) 'Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs', *Silicon*. Silicon. doi: 10.1007/s12633-020-00514-1.
- Garg, A., Singh, Y. and Singh, B. (2020) 'Dual-Channel Junctionless FETs for Improved Analog/RF Performance', *Silicon*. Silicon. doi: 10.1007/s12633-020-00545-8.
- Goel, A. *et al.* (2020) 'High-K Spacer Dual-Metal Gate Stack Underlap Junctionless Gate All Around (HK-DMGS-JGAA) MOSFET for high frequency applications', *Microsystem Technologies*. Springer Berlin Heidelberg, 26(5), pp. 1697–1705. doi: 10.1007/s00542-019-04715-6.
- Jeon, D. Y. *et al.* (2020) 'Controlling the Effective Channel Thickness of Junctionless Transistors by Substrate Bias', *IEEE Transactions on Electron Devices*, 67(11), pp. 4736–4740. doi: 10.1109/TED.2020.3020284.
- Panigrahi, S., Sahu, P. K. and Lenka, A. S. (2020) 'Impact of non-uniformly doped double-gate junctionless transistor on the performance of 6T-SRAM bitcell', *Micro and Nano Letters*, 15(2), pp. 72–77. doi: 10.1049/mnl.2019.0375.
- Preethi, S. and Balamurugan, N. B. (2020) 'Analytical Modeling of Surrounding Gate Junctionless MOSFET Using Finite Differentiation Method', *Silicon*. Silicon. doi: 10.1007/s12633-020-00653-5.
- Sun, Y. *et al.* (2020) 'Analysis of gate-induced drain leakage in gate-all-around nanowire transistors', *Journal of Computational Electronics*. Springer US, 19(4), pp. 1463–1470. doi: 10.1007/s10825-020-01568-5.
- Tripathy, M. R. *et al.* (2020) 'Device and Circuit-Level Assessment of GaSb / Si Heterojunction Vertical Tunnel-FET for Low-Power Applications', *IEEE TED*, pp. 1–8.
- Genius, 3-D Device Simulator, Version 1.9.0, Reference Manual, Cogenda Pvt. Ltd., Singapore.
- Cadence Virtuoso Spectre Circuit Simulator, Cadence Des. Syst., San Jose, CA, USA.

## **References**

---

- IR1: <https://www.extremetech.com/extreme/203490-moores-law-is-dead-long-live-moores-law>
- IR2: <http://pubs.rsc.org/en/content/articlehtml/2015/NR/C4NR01600A>
- IR3: [http://www.slideshare.net/varun\\_bansal90/power-7535521](http://www.slideshare.net/varun_bansal90/power-7535521)
- IR4: [https://www.researchgate.net/figure/MOSFET-cross-sectional-visualization-of-the-hot-carrier-effect-led-by-carrier\\_fig2\\_220408057](https://www.researchgate.net/figure/MOSFET-cross-sectional-visualization-of-the-hot-carrier-effect-led-by-carrier_fig2_220408057)

---

---

## AUTHOR'S RELEVANT PUBLICATIONS

---

---

### Journals:

1. **Kamalaksha Baral**, Prince Kumar Singh, Sanjay Kumar, Sweta Chander, and Satyabrata Jit, "Ultrathin Body Nanowire Hetero-dielectric Stacked Asymmetric Halo Doped Junctionless Accumulation Mode MOSFET for Enhanced Electrical Characteristics and Negative Bias Stability," *Superlattices and Microstructures*, vol. 138, Dec.2019.
2. **Kamalaksha Baral**, Prince Kumar Singh, Sanjay Kumar, Ashish Singh, Manas Tripathy, Sweta Chander, and Satyabrata Jit, "2-D analytical modeling of drain and gate-leakage current of cylindrical gate asymmetric halo doped dual material-junction less accumulation mode MOSFET," *International Journal of Electronics and Communications*, vol. 116, Jan.2020.
3. **Kamalaksha Baral**, Prince Kumar Singh, Sanjay Kumar, Ashish Singh, Manas Tripathy, Sweta Chander, and Satyabrata Jit, "A 2-D compact DC model for engineered nanowire JAM-MOSFETs valid for all operating regimes," *Semiconductor Science and Technology*, vol. 35(8), May 2020.
4. **Kamalaksha Baral**, Prince Kumar Singh, Gautam Kumar, Ashish Kumar Singh, Manas Ranjan Tripathy, Sanjay Kumar and Satyabrata Jit, "Impact of Ion Implantation on Stacked Oxide Cylindrical Gate Junctionless Accumulation Mode MOSFET: An Electrical and Circuit Level Analysis," *Materials Science in Semiconductor Processing* (Communicated)
5. **Kamalaksha Baral**, Prince Kumar Singh, Sanjay Kumar, Ashish Kumar Singh, and Satyabrata Jit, "A Unified 2-D Quasi-ballistic Model for Nanowire Junctionless Accumulation and Inversion Mode MOSFET," *Superlattices and Microstructures* (Communicated)

### International Conference:

1. **Kamalaksha Baral**, Prince Kumar Singh, Sanjay Kumar, Sweta Chander, and Satyabrata Jit, "Performance Analysis and Optimization of Nanotube Junctionless Accumulation MOSFETs with Lateral HfO<sub>2</sub>/SiO<sub>2</sub> Gate-oxide Structure," Nanotechnology for Instrumentation & measurement Workshop, (NANOfIM-2017), GBTU , Noida , India, Nov.16-17, 2017.



2. **Kamalaksha Baral**, Prince Kumar Singh, Sweta Chander, Kunal Singh, and Satyabrata Jit, "Performance Analysis of Nanotube Junctionless Accumulation Mode MOSFETs with Ion Implanted Doping Profile," 3rd International Conference for Convergence in Technology (I2CT-2018), Pune, India, Apr.6-7, 2018.
3. **Kamalaksha Baral**, Prince Kumar Singh, Sanjay Kumar, Sweta Chander, Manas Ranjan Tripathy, and Satyabrata Jit, "Dual Material-Stacked Hetero-Dielectric-Junctionless Accumulation Mode Nanotube MOSFET for enhanced Hot Carrier and Trapped Charges Reliability," 3rd Electron Devices Technology and Manufacturing (EDTM-2019), Singapore, Mar.13-15, 2019