Effect of Gaussian Doping on Vertically Stacked Oxide CG- JAM MOSFET: An Electrical and Circuit Level Analysis

6.1 Introduction

We have analyzed the effects of various device design engineering of the JAM MOSFETs with a lateral graded channel engineering. We have also discussed in Chapter-1 that a vertically graded channel engineering by using a vertical Gaussian doping profile in the channel can also be used for improving the device performance (Kumari, Kumar, Saxena and Gupta, 2018a). It may be mentioned that the Gaussian doping profile provides a better flexibility for changing the doping concentrations in the channel by varying the peak doping, its position and straggle parameter. Even the uniform doping profile can be obtained from the Gaussian doping profile by using the large value of the straggle parameter (Kumari *et al.*, 2017). The Ion-implantation used for doping in a semiconductor normally results in a Gaussian doping profile. Ion-implantation followed by annealing may result in a Gaussian type of doping profile along the radius of the channel in the CG-JAM MOSFETs (Singh *et al.*, 2016). Some researchers have reported the electrical and circuit-level analysis of the Gaussian doping in the source/drain region of the MOS transistors (Sarkar and Member, 2014; Mukherjee *et al.*, 2015; Sai, Chakraborty and Das, 2016). Some analytical models have also been developed the Gaussian doped double-gate MOSFETs (Singh *et al.*, 2016; Kumari, Kumar, Saxena and Gupta, 2018b; Kumari *et al.*, 2018). However, to the best of our knowledge, no significant study has been reported the electrical and circuit-level performances of the Gaussian doped CG-JAM MOSFETs.

In this present chapter, an attempt is made to investigate the TCAD based performance analysis of vertically stacked CG JAM MOSFETs with a vertical Gaussian doping profile. The

effects of the profile parameters on the device and circuit level performances of the device have been investigated in details. DC performance parameters (such as the drain current, threshold voltage, $I_{on}/I_{off,}$ g_m, g_d and intrinsic gain) and RF performance parameters (such as the gate-drain capacitance (C_{gd}), gate-source capacitance (C_{gs}), total gate capacitance (C_{gg}), cutoff frequency (f_T), gain-bandwidth product (GBW product), transit time-τ and transconductance frequency product (TFP)) have been studied. Then, a complimentary CG-JAM p-MOSFET has been constructed by varying the work function of the gate material to implement a CMOS inverter. The static and transient parameters (i.e. noise margin, static current, inverter gain, rise time, fall time, propagation delay, overshoot short-circuit current and power dissipation) of the inverter have been studied. Finally, the static and dynamic characteristic parameters such as the read noise margin-RNM, write noise margin-WNM, N-curve analysis, read access time-RAT and write access time-WAT of a 6T SRAM cell designed by using the proposed Gaussian doped CG JAM MOSFETs have been studied.

Section 5.2 presents the details of device structure and simulation procedure. Some important results and related discussions related to device and circuit level performance of stacked Gaussian doped CG-JAM MOSFET have been presented in Section 5.3. Finally, Section 5.4 summarizes the major observations of the present chapter.

6.2 Device structure and simulation procedure

In this section we would discuss about the specification of the device structure and simulation procedure to obtain the results.

6.2.1 Device structure

Ion implantation and subsequent annealing create a Gaussian type doping profile along the radius r inside the channel region. Fig 6.1 demonstrates the 2-D schematic of Gaussian doped channel CG-JAM MOSFET. As we can observe from fig 6.1 that the peak doping is near the

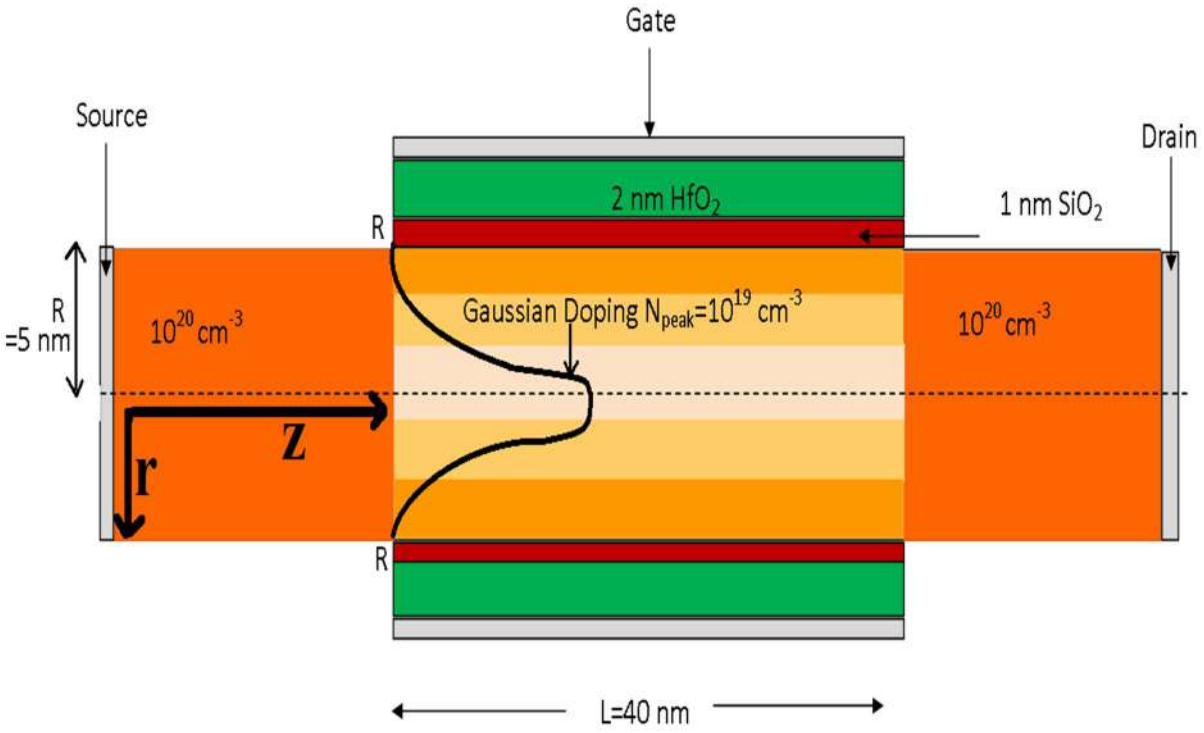


Fig. 6.1: 2-D cross-section diagram of Gaussian doped channel in stacked oxide CG-JAM MOSFET.

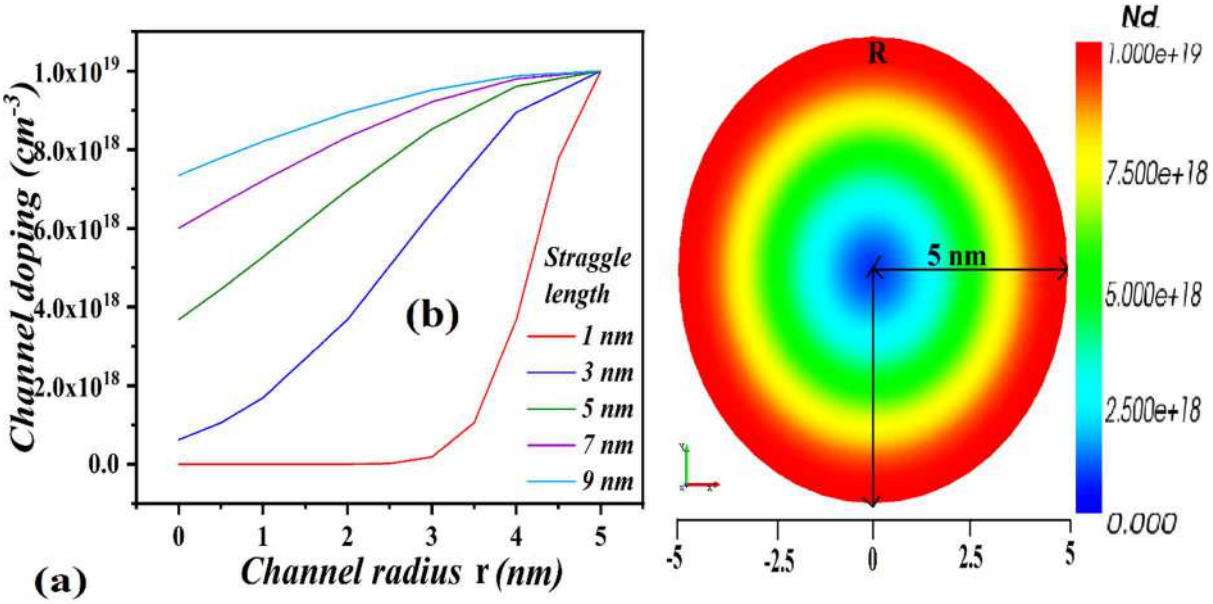


Fig. 6.2: (a) Variation of channel doping against the radius of the channel for different straggle length (b) 2-D view of doping variations along channel radius for straggle length of 3 nm.

surface and decrease as we move towards the center. The Gaussian doping profile could be represented as (6.1) (Kumari *et al.*, 2018).

$$f(r) = N_{peak}\, exp\left[-\frac{(r-R)^2}{2\sigma^2}\right] \tag{6.1}$$

where r is the radius of the channel, R is the position of peak doping, N_{peak} is the peak doping density and σ is the straggle/characteristic length. Here straggle length of 1 nm, 3 nm, 5 nm, 7 nm and 9 nm have been considered. Fig 6.2(a) depicts channel doping concentration along the radius of the channel for different straggle lengths. It should be noted that the channel is vertically Gaussian doped along the radius with the peak doping at the surface. The doping is steeper at the surface and nearly depleted at the center of the device. We could also observe that as the straggle length increase the doping changes from steeper to flatter and tend to spread across the width of the device. As the straggle length increases the doping gets spread and at a straggle length above 10 nm it almost behaves as a uniformly doped device. Fig 6.2(b) shows the 2-D cross-section of the simulated structure along the radius of the channel for straggle length of 3 nm. The CG-JAM structure has a channel length of 40 nm and the source and drain

TABLE 6.1: Device specifications

Device Type	N_{peak} *(cm^{-3})*	*Source /Drain doping (cm^{-3})*	*SiO_2/HfO_2 (nm)*	*Gate material workfunction (eV)*
CG-JAM p-MOSFET	**10^{19}**	**10^{20}**	**1 nm/2 nm**	**4.68**
CG-JAM n-MOSFET	**10^{19}**	**10^{20}**	**1nm/ 2 nm**	**4.9**

extension length of 20 nm. It has a peak doping of 10^{19} cm^{-3}. We have compared here devices with same peak doping but different effective doping so that the mobility of the devices remains almost constant. The details of the device specification are given in table 6.1.

6.2.2 Simulation procedure

The proposed Ion implanted CG-JAM MOSFET has been simulated using a commercial 3-D TCAD tool from COGENDA (COGENDA, 2016). The *BGN* model has been taken to account for bandgap narrowing, doping dependent *lucent* mobility model and *fermi* statistics have been taken for the highly doped channel. *BBT* model has been taken to account for the band to band tunneling near the drain side at a high drain field. *Hot Carrier* model has been enabled to account for hot carrier effects inside the device. Further energy balance solver has been used to account for high field phenomena inside the device. *Cylinder.inverse* command

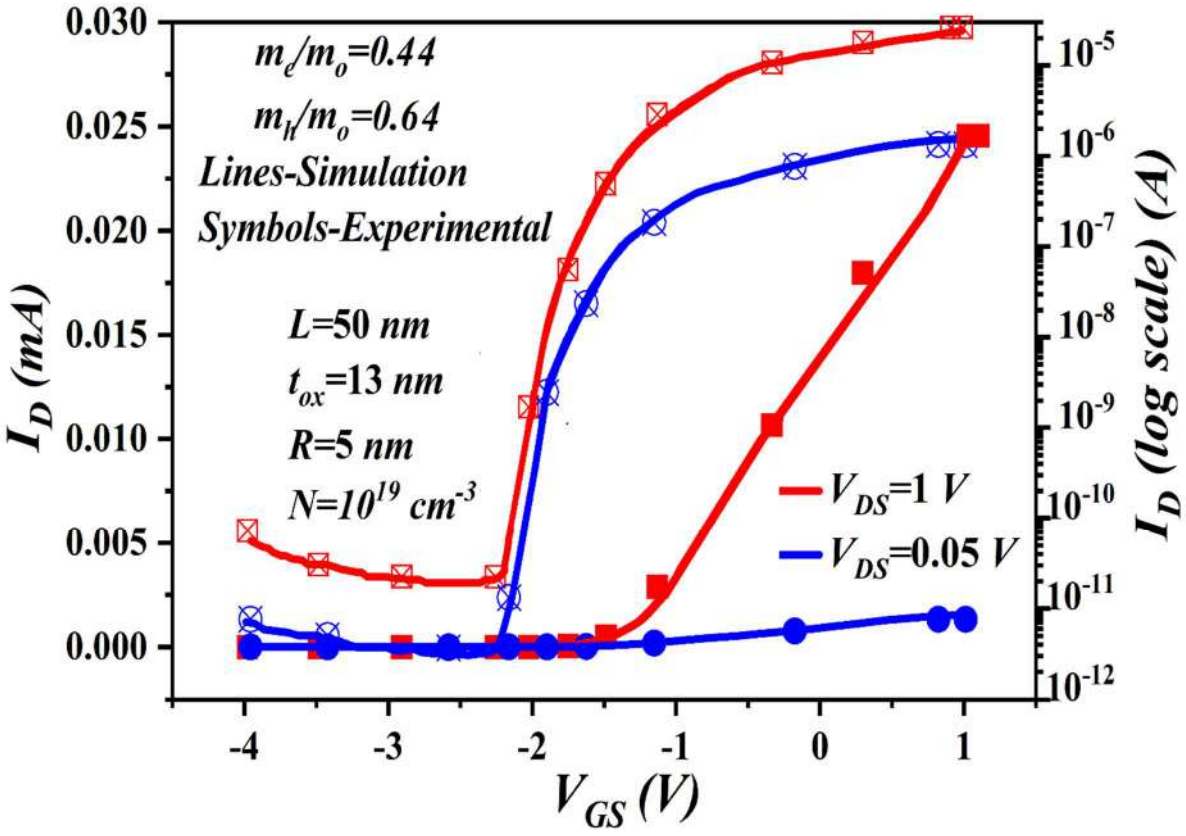


Fig 6.3: Calibration of simulation models with experimental results in (Choi *et al.*, 2011).

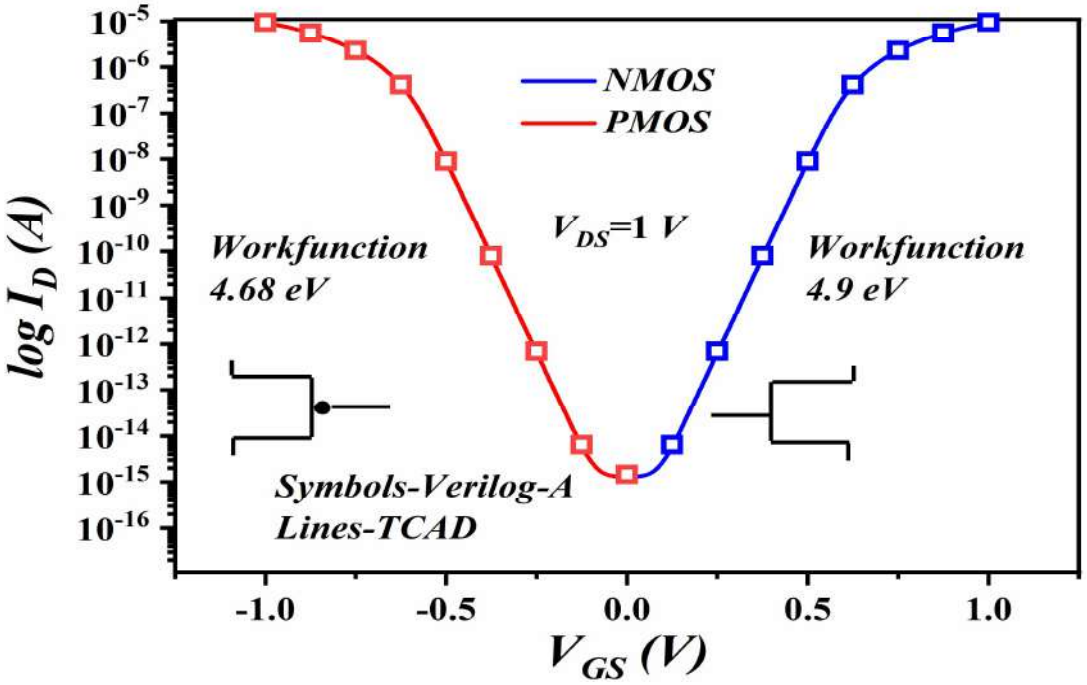


Fig. 6.4: Calibration Verilog-A model with TCAD simulation of complimentary drain current characteristics for stacked oxide CG-JAM p-MOSFET and n-MOSFET to implement COMS inverter at straggle length=1nm and V_{DS}=1 V.

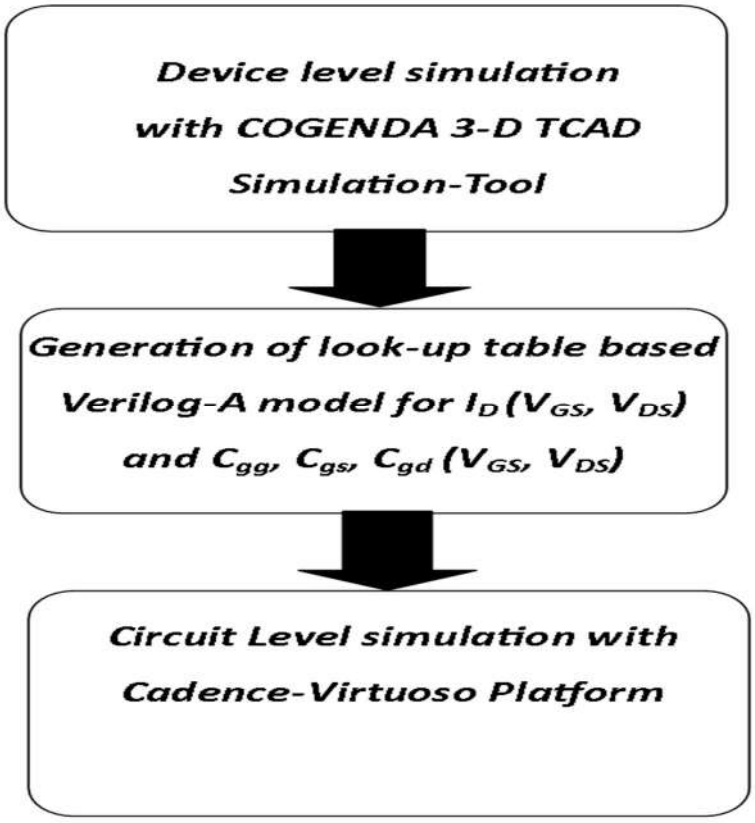


Fig. 6.5: The workflow of the circuit level simulation procedure.

is used for vertical gaussian doping inside the channel. For the simulation of AC parameters like capacitances, a frequency of 1 MHz has been applied as default frequency. Fig 6.3 shows the calibrations of simulation models and their parameters with that of experimental results in (Choi *et al.*, 2011). Carrier masses and mobility have been adjusted to match the experimental result.

Complimentary CG-JAM p-MOSFET has been implemented by varying the gate material workfunction (4.68 eV) for all straggle lengths. ID-VGS has been matched to construct a complementary ion-implanted CG-JAM p-MOSFET. Further calibration with the Verilog-A model has also been done as shown in fig 6.4. A look-up table-based Verilog-A model has been generated with ID (V_{GS}, V_{DS}) and C_{gg}, C_{gs}, C_{gd} (V_{GS}, V_{DS}) information from TCAD simulator. Thereafter circuit-level simulation for CMOS inverter and 6T SRAM have been performed using the generated Verilog-A based look-up table model in the Cadence-Virtuoso platform (CADENCE, 2016). The detailed workflow of the simulation procedure is shown in fig 6.5.

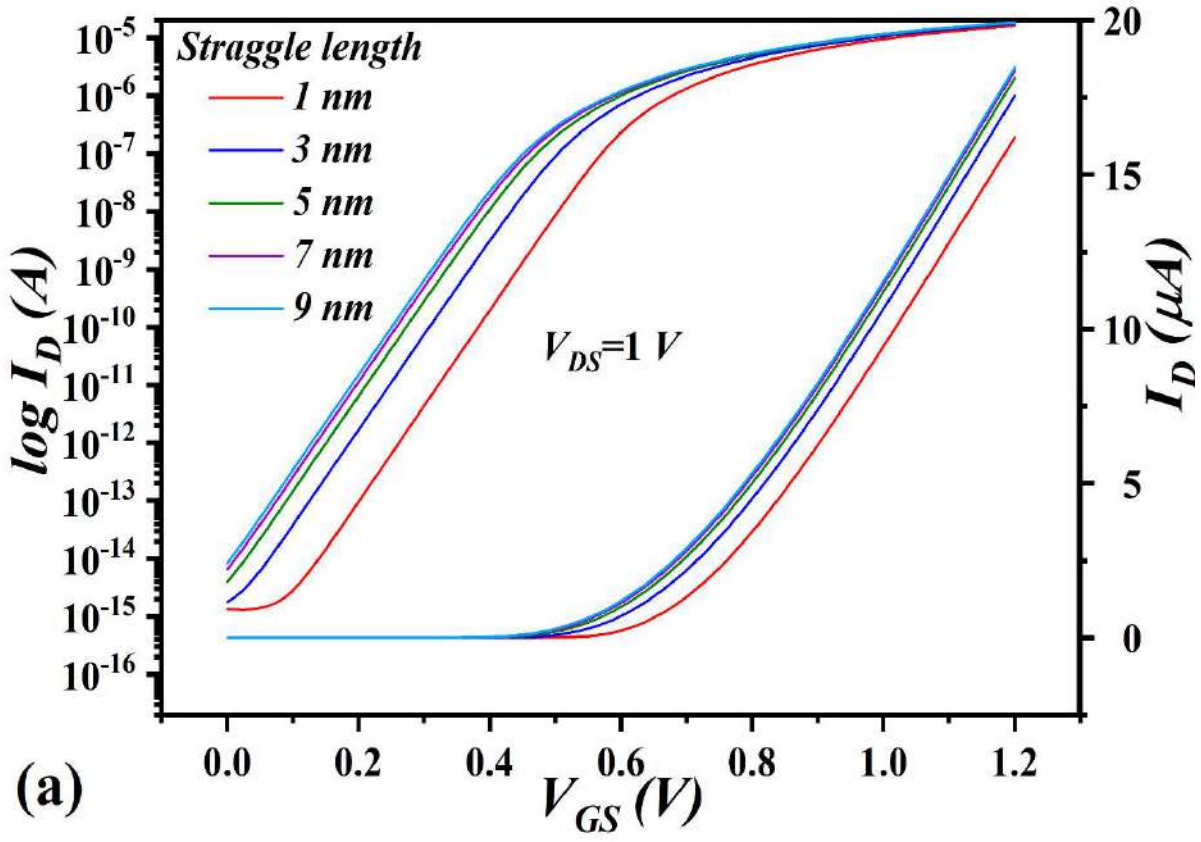
6.3 Results and discussion

In this section, we have analyzed in detail the electrical characteristic (DC and RF) and circuit-level performance (CMOS inverter and 6T SRAM) of ion-implanted CG-JAM MOSFET. Various parameter performances have been analyzed as a function of straggle length.

6.3.1 DC analysis

Fig 6.6 shows I_D-V_{GS} and I_D-V_{DS} characteristics for ion-implanted CG-JAM MOSFET. It could be observed that both I_{ON} and I_{OFF} decrease with a decrease in straggle length. The decrease in the total number of dopants reduces the total volume of carriers. Therefore, the Ion decreases with a decrease in straggle length. Off-state leakage current flows through the center in JAM MOSFET. At lower straggle length the center of the device is effectively depleted of carriers which suppresses the subthreshold leakage current. Fig 6.7(a) shows the variation of g_m and g_d

with V_{GS}. It could be observed that although peak gm decreases with straggle length due to low Ion but the peak g_d increases. It should be noted from the inset of fig. 6.7(a) that g_d decreases substantially at high V_{GS} at lower straggle length. This increases the intrinsic gain (g_m/g_d) and current conversion efficiency, which could be observed in fig 6.7(b). The threshold voltage and I_{ON}/I_{OFF} ratio are important parameters for DC analysis. I_{ON} and I_{OFF} are taken at V_{GS}=1 V and 0 V respectively. The threshold voltage is measured by the constant current method. From table 6.2 it could be observed that both threshold voltage and I_{ON}/I_{OFF} ratio increases with a decrease in straggle length. It is found that for 1 nm straggle length device, I_{ON}/I_{OFF} ratio and threshold voltage increase by 610% and 28% as compared to the device with 9 nm straggle length. The increase in threshold voltage may be attributed to the depletion of carriers at the center of the channel at lower straggle length. As the conduction in channel starts from the center of the device in JAM MOSFET, therefore a higher V_{GS} is needed to turn on the device



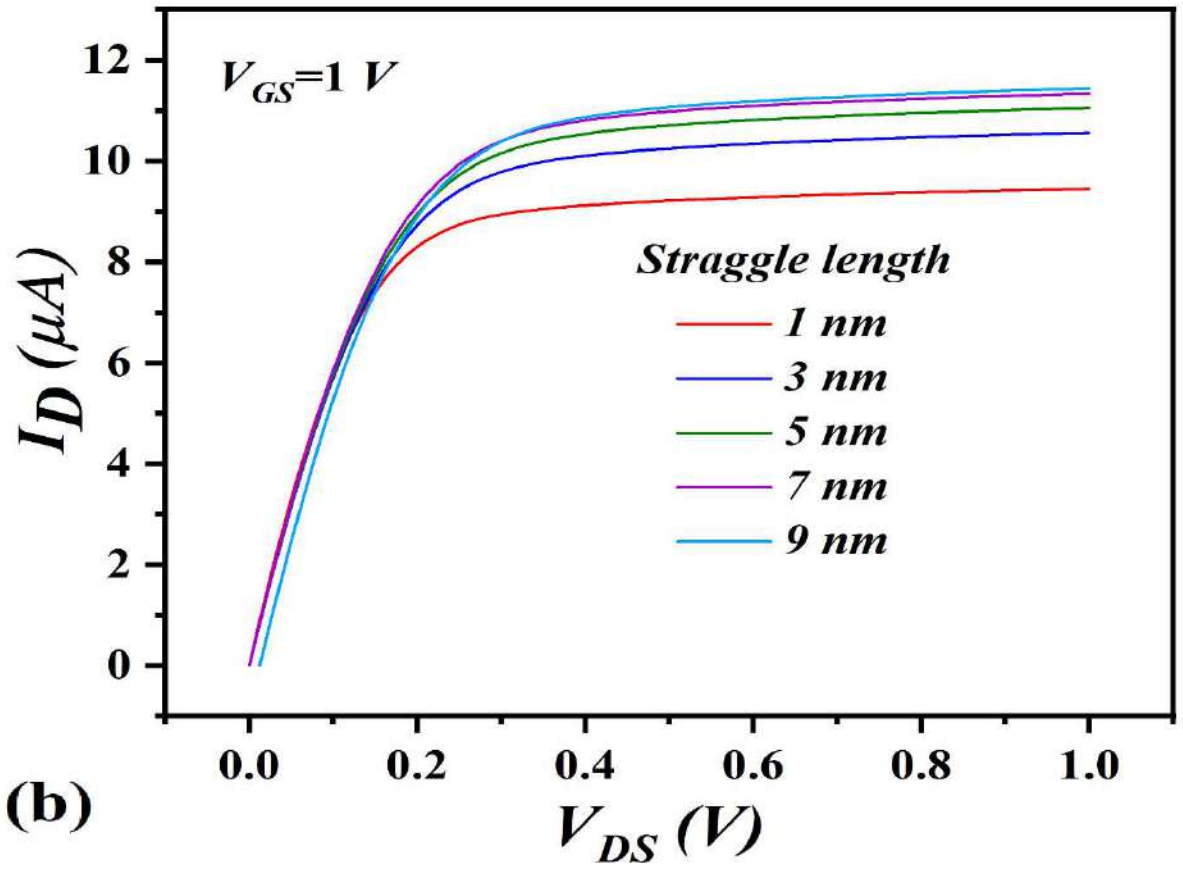
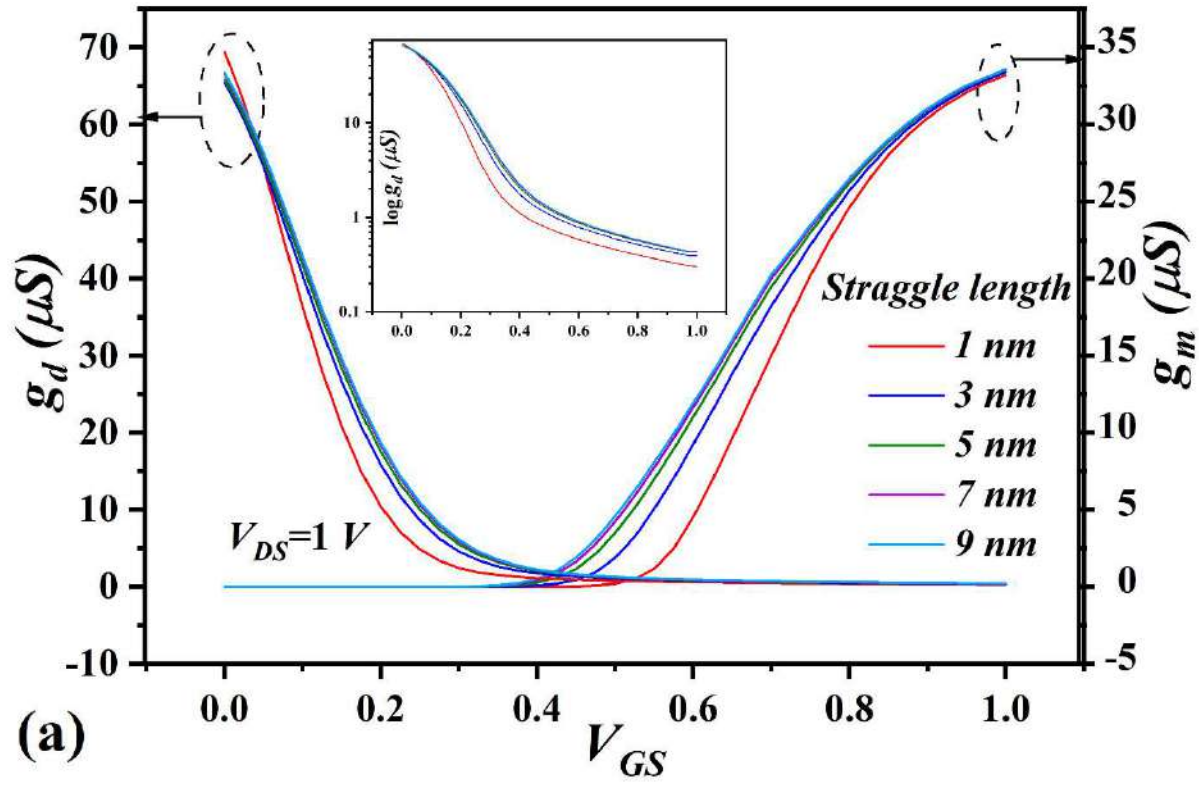


Fig. 6.6: (a) ID-VGS at VDS=1 V; (b) ID-VDS at VGS=1 V at different straggle lengths.



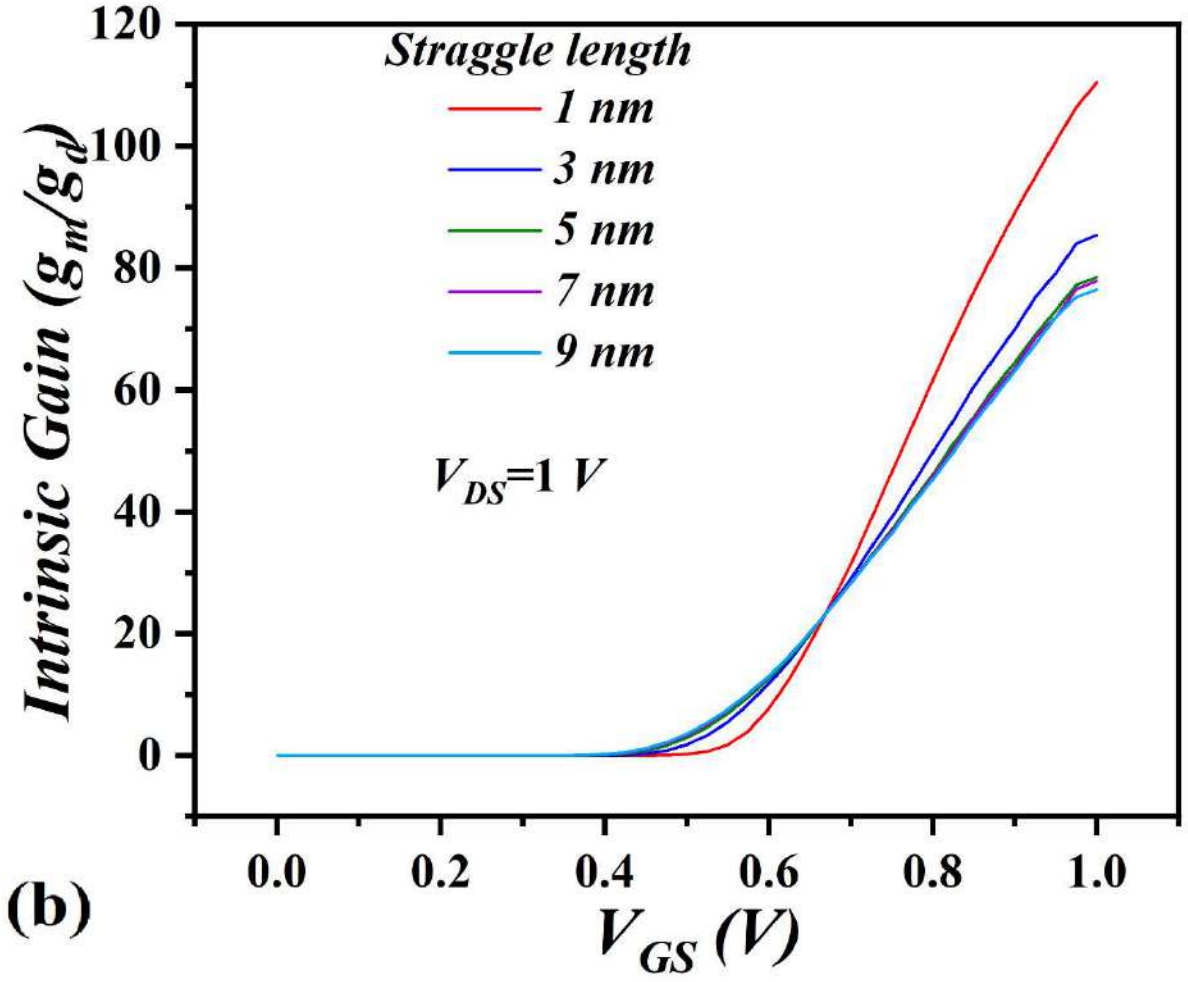


Fig. 6.7: (a) Variation of Transconductance (g_m) and drain conductance (g_d) with V_{GS}, log(g_d) with V_{GS} (inset); (b) variation of intrinsic gain with V_{GS} at different straggle lengths.

TABLE 6.2: Specification of threshold voltage and I_{on}/I_{off} for various straggle lengths of Gaussian doped CG-JAM MOSFET.

Straggle length	1 nm	3 nm	5 nm	7 nm	9 nm
Threshold Voltage	0.563	0.4955	0.463	0.449	0.442
I_{on}/I_{off}	7.05×10^9	5.97×10^9	2.8×10^9	1.77×10^9	1.39×10^9

(Singh, Gola, Singh, Goel, Kumar, *et al.*, 2016). An increase in threshold voltage makes lower straggle length device more immune to drain induced barrier lowering (DIBL). Further higher I_{ON}/I_{OFF} increases the noise margin of the device.

6.3.2 RF analysis

RF or frequency analysis is important from an analogue or circuit level point of view. Fig 6.8(a) shows variations of different capacitances with straggle length. C_{gs} (gate-source capacitance) decreases whereas C_{gd} (gate-drain capacitance) increases with a decrease in straggle length. It could further be observed that total capacitance C_{gg} also decreases with a decrease in straggle length since C_{gs} dominates of the parasitic miller capacitance C_{gd}. It is to be observed that C_{gg} increases with V_{GS} which can be attributed to the lowering of barrier potential and increase of charge from source to drain with an increase in V_{GS}. Since at lower straggle length the device has a smaller number of carriers around the center therefore the charge associated with it is also less. Which is the reason for decreased C_{gg} at lower straggle length. Therefore a device with lower straggle length has a faster response due to the lower value of C_{gg} (Mysore, 2012). Unity short circuit current gain frequency is an important RF parameter and is given by (6.2) (Sai, Chakraborty and Das, 2016). Since C_{gg} decreases more rapidly than gm in a device with lower straggle length. Therefore, it could be observed from fig 6.8(b) that peak f_T increases with a decrease in straggle length.

$$f_T = \frac{g_m}{2\pi(C_{gd}+C_{gs})} \tag{6.2}$$

GBW product defines the constant gain region of operation of a device and is given by (6.3) for a DC gain of 10 [7]. *TFP* (transconductance frequency product) is a figure of merit (FOM) and signifies a trade-off between power dissipation and bandwidth which is represented as (6.4).

$$GBW = \frac{g_m}{2\pi 10 C_{gd}} \tag{6.3}$$

$$TFP = \left[\frac{g_m}{I_D}\right] \times f_T \tag{6.4}$$

It could be observed from fig 6.9 that both GBW product and TFP increase with a decrease in straggle length. For lower straggle length device g_m decreases equivalently as I_D but due to an

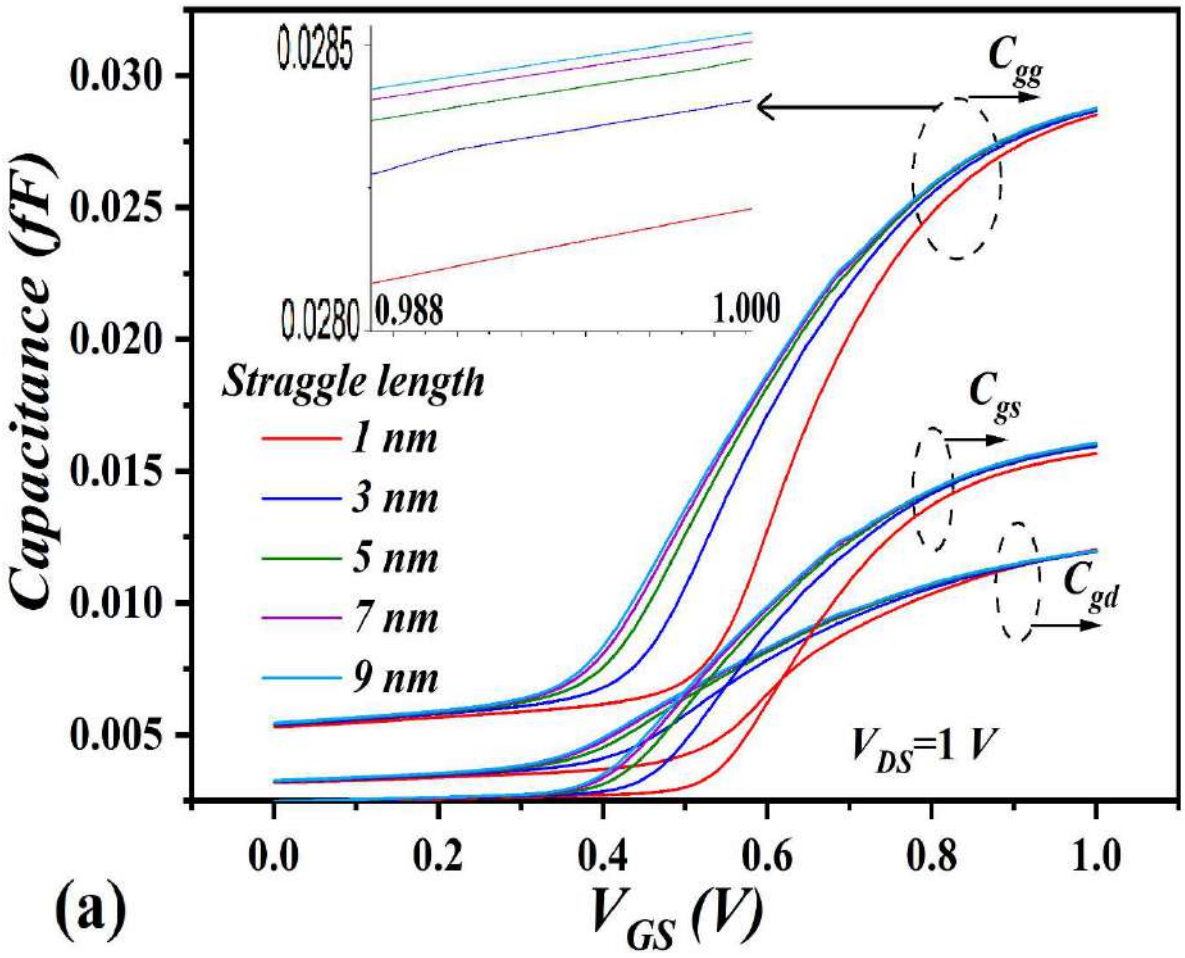
increase in f_T the total TFP is also increased. Transit time is defined as the time taken by the carrier to travel from source to drain and is given as (6.5). The transit time should be as low as possible for faster operation of the device. The frequency of oscillation at which power gain drops to unity is defined as f_{max} and given as (6.6) (Patel *et al.*, 2019).

$$\tau = \frac{1}{2\pi f_T} \tag{6.5}$$

Fig 6.10(a) shows that τ (transit time) is higher for straggle length of 1 nm at the subthreshold region but is lower above

the threshold region of operation.

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{gd} R_{gd}}} \tag{6.6}$$



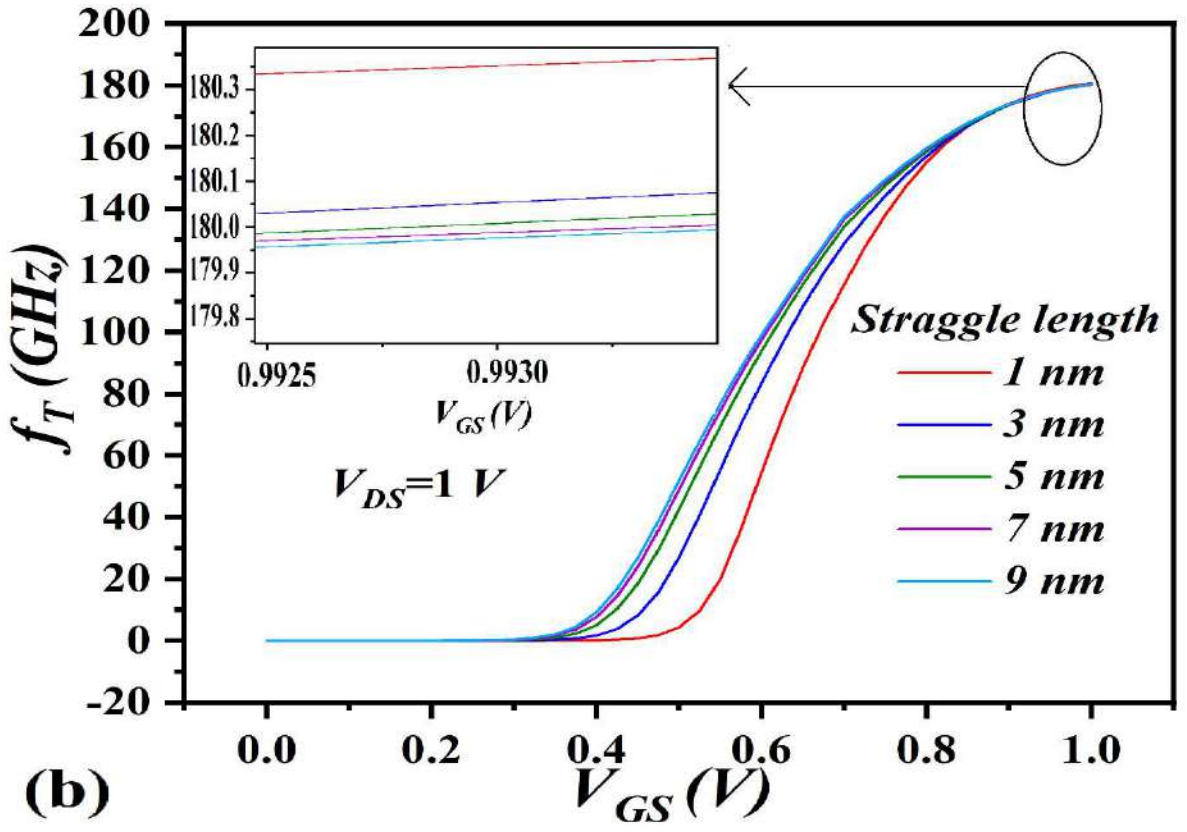
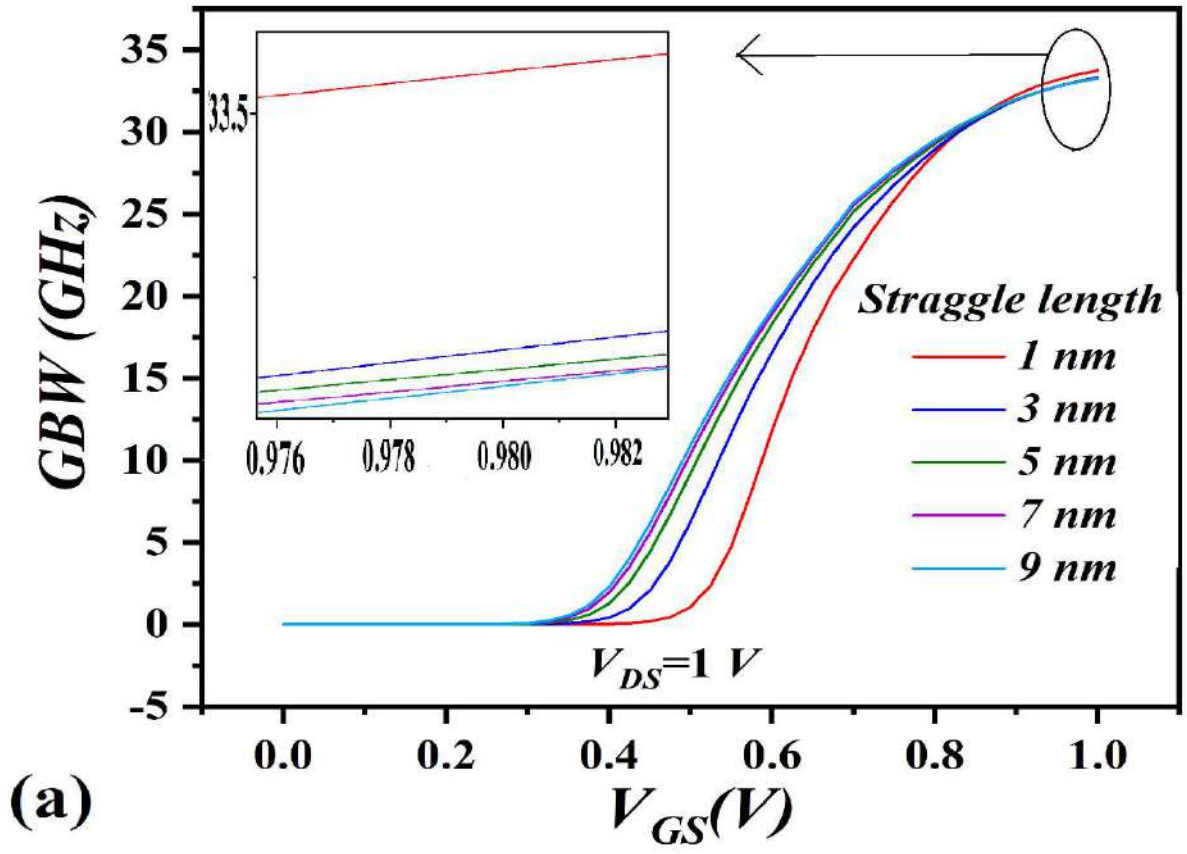


Fig. 6.8: (a) Variation of capacitances C_{gg}, C_{gs} and C_{gd} with V_{GS}; (b) Variation of f_T with V_{GS} for different straggle length.



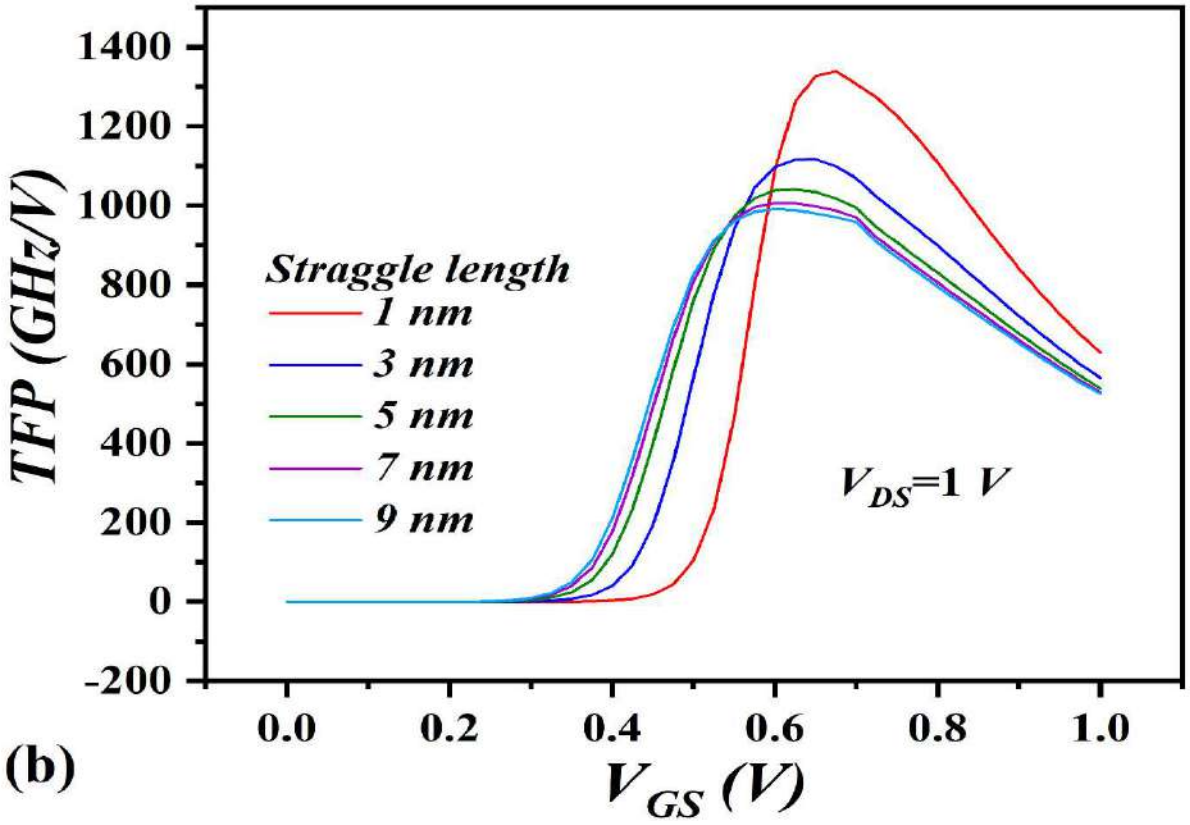
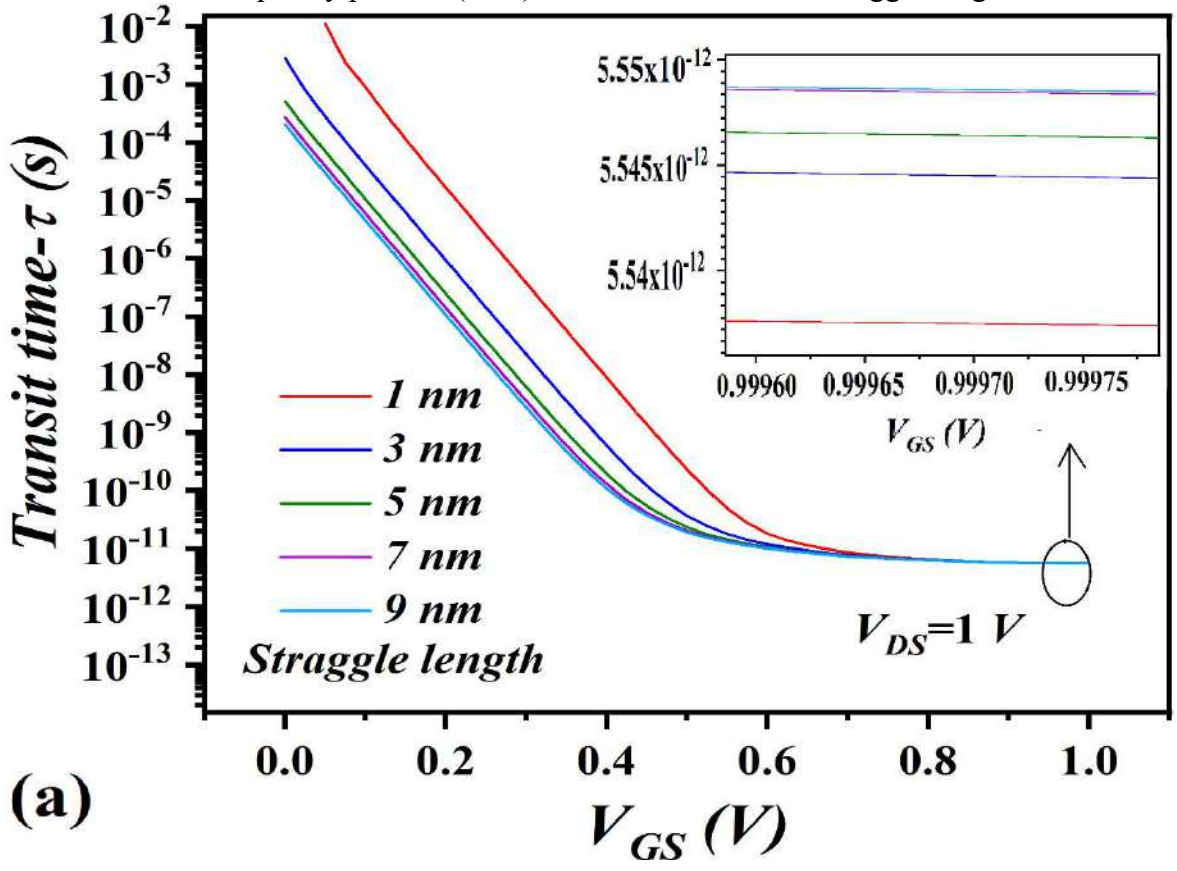


Fig 6.9: (a) Variation of gain bandwidth (*GBW*) product with V_{GS}; (b) variation of transconductance frequency product (*TFP*) with V_{GS} for different straggle length.



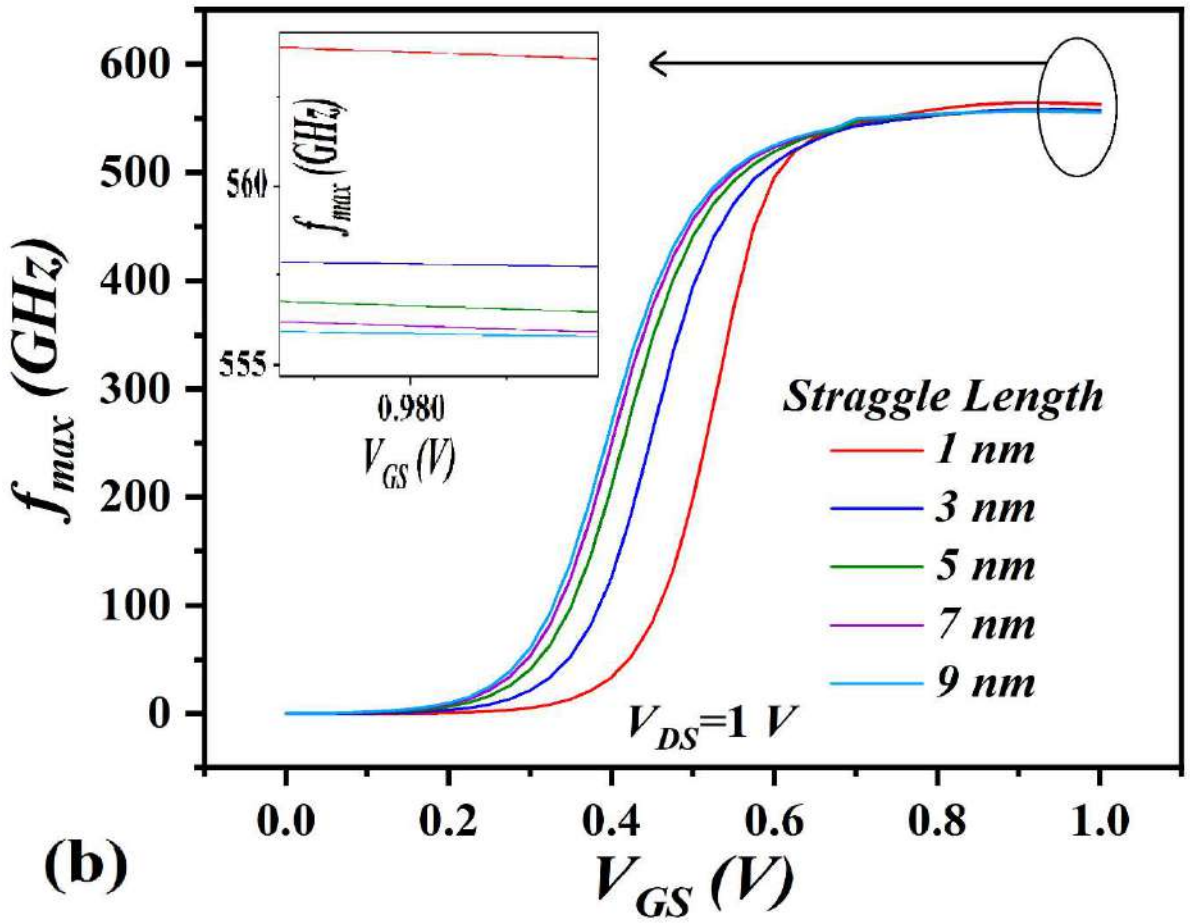


Fig 6.10: (a) Variation of transit time (τ) product with V_{GS}; (b) variation of f_{max} with V_{GS} for different straggle length.

Since transit time is inversely dependant on f_T and f_T increases with decrease in straggle length at higher voltage. This signifies that device with lower straggle length operates faster in on-state. Fig 6.10(b) shows that f_{max} increases with a decrease in straggle length. Therefore, devices show better RF performance for lower straggle length.

6.3.3 Static and transient analysis of CMOS inverter

Fig 6.11 shows the static analysis of CMOS inverter built with ion-implanted CG-JAM MOSFET. Fig 6.11(a) shows the butterfly curve which analyses the noise margin of the devices. The voltages V_{IL} and V_{IH} are voltages where the gain of the inverter $\partial V_{in}/\partial V_{out} = -1$. The minimum and maximum output voltages V_{OH} and V_{OL} can be calculated from the transfer characteristics. $NM_L=V_{IL}-V_{OL}$ and $NM_H=V_{OH}-V_{IH}$ are high and low noise margins (Tripathy *et*

al., 2020). Further, the noise margin could be calculated as diagonal of the largest square inside the butterfly curve divided by $\sqrt{2}$ (Saini, 2016). It could be further observed that both noise margin and inverter gain increase with the decrease in straggle length. The noise margin of the device with 1 nm straggle length (457 mV) increases by 9.6% when compared to the device with 9 nm straggle length (417 mV). The gain of the inverter also increases by 239%. This can be attributed to the fact that I_{on}/I_{off} and threshold voltage both increases with a decrease in straggle length. Therefore, lower straggle length device is more immune to noise. Fig 6.11(b) shows inverter current variations with straggle length. It should be observed that inverter current decreases with straggle length. The inverter current decreases by 97% when 9 nm and 1 nm straggle length devices are compared. Therefore, dynamic power dispassion is reduced for lower straggle length device. Fig 6.12 shows the transient characteristics of CMOS inverter. It could be observed from fig 6.12(a) that overshoot increases with a decrease in straggle length. It could be attributed to the fact that C_{gd} increases with decrease in straggle length and overshoot depends on coupling or miller capacitor which couples input to the output (Alorda *et al.*, 2018; Tripathy *et al.*, 2020). The overshoot increases by 8.3% when 9 nm and 1 nm straggle length devices are compared. Further, it could also be observed that output transition is slow for lower straggle length device which is the cause for higher propagation delay in lower straggle length device. Fig 6.12(b) shows short circuit transient current. It should be noted that short circuit transient current overshoots are oscillating in nature but the average short circuit current is less for lower straggle length device. The detailed analysis of the various transient parameters is given in Table 6.3. It could be observed that both rise time and fall time decrease with a decrease in straggle length. Power dispassion and propagation delay are important FOMs of CMOS inverter. It could be noted that while power dissipation decreases the propagation delay increases with a decrease in straggle length. The increase in propagation delay is due to a reduction of the I_D (propagation delay α V_{DD}/I_D) at lower straggle length.

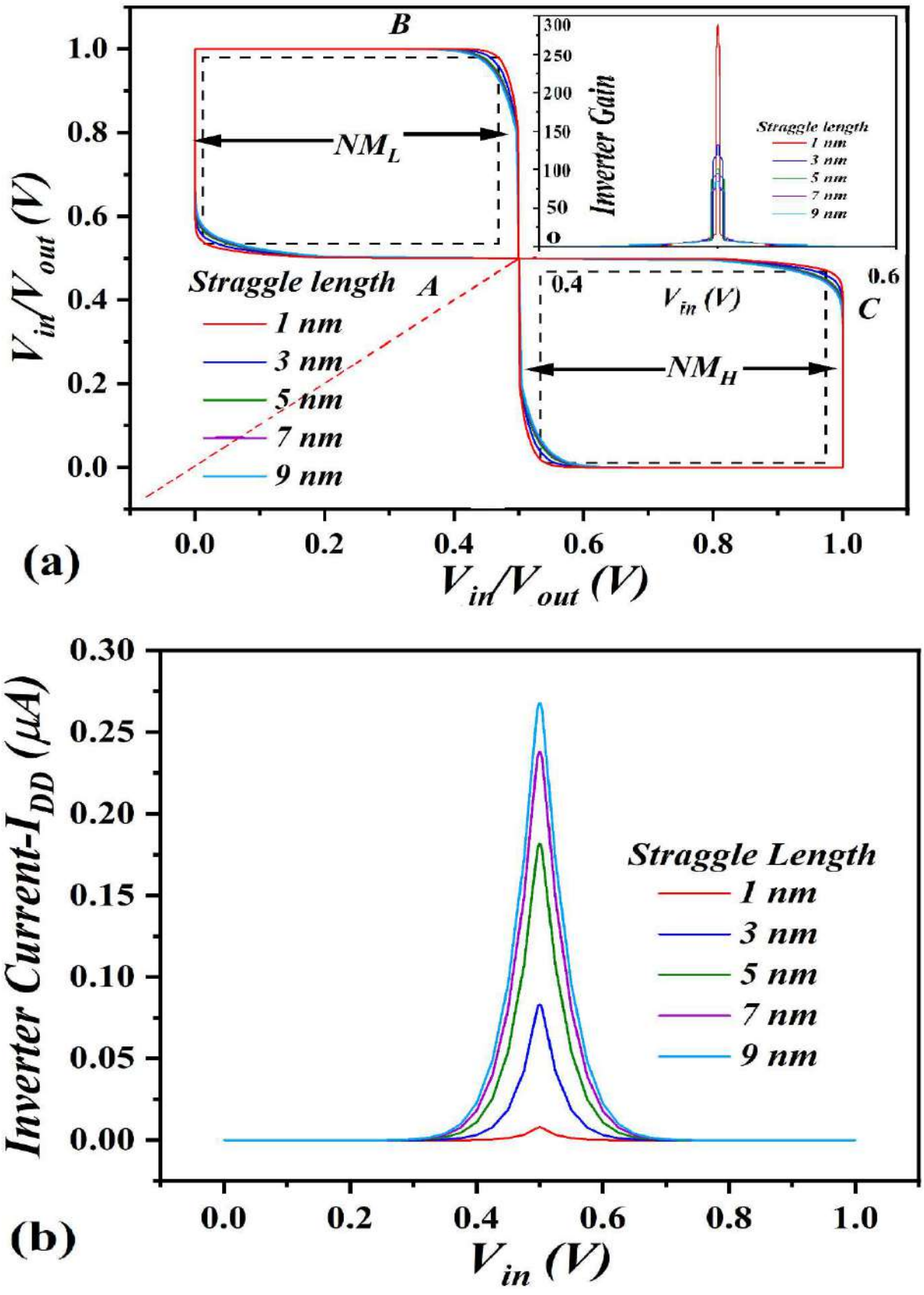


Fig. 6.11: (a) Variation of noise margin and gain of the inverter with straggle length; (b) variation of inverter current with straggle length.

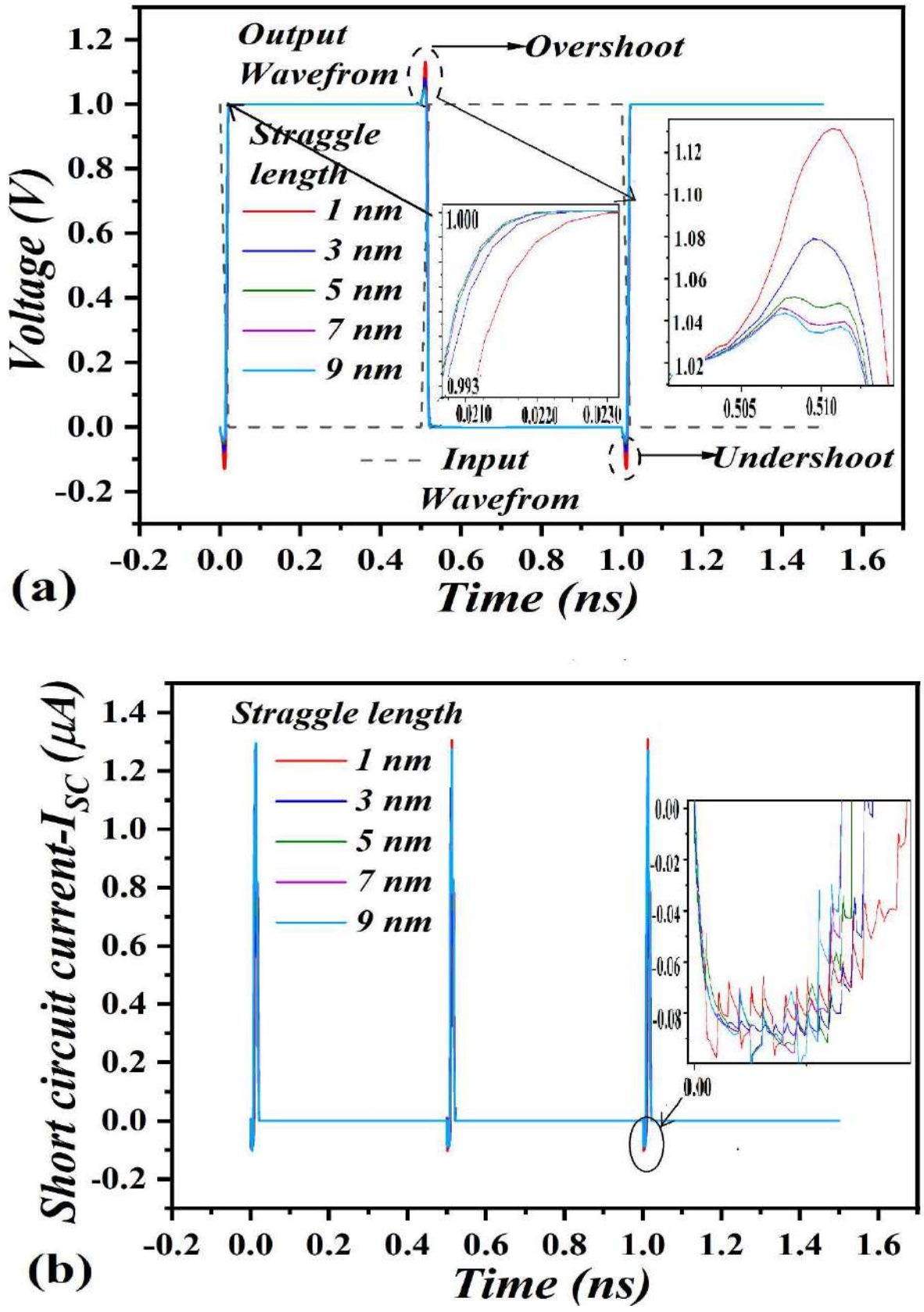


Fig. 6.12: (a) Variations of transient characteristics of the inverter with straggle length; (b) variation in short circuit transient current with straggle length.

Therefore, it could be inferred that although lower straggle length devices are power efficient but are slow to respond for digital circuit applications.

TABLE 6.3: Transient parameters of CMOS Inverter

Straggle length	*Rise time-t_r (ps)*	*Fall time-t_f (ps)*	*Propagation delay-t_{HL} (ps)*	*Propagation delay-t_{LH} (ps)*	*Power dissipation (nW)*
1 nm	**3.93**	**3.98**	**7.506**	**7.52**	**15.39**
3 nm	**4.12**	**4.098**	**6.649**	**6.63**	**17.29**
5 nm	**4.15**	**4.163**	**6.293**	**6.29**	**18.64**
7 nm	**4.24**	**4.246**	**6.154**	**6.14**	**19.30**
9 nm	**4.42**	**4.417**	**6.062**	**6.09**	**19.59**

6.3.4 Static and dynamic analysis of 6T SRAM

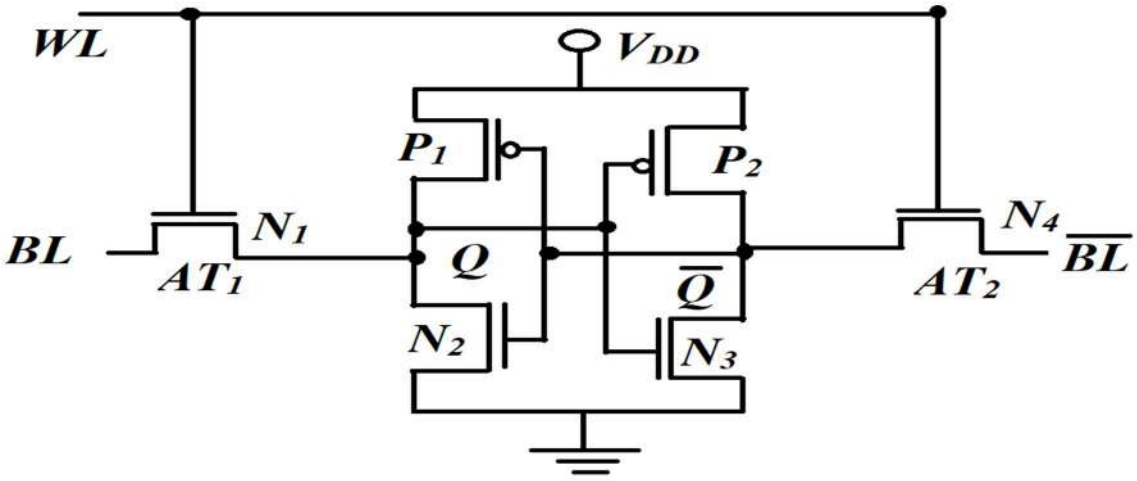


Fig. 6.13: Schematic of a 6T SRAM cell.

For faster access time power-efficient memory should be integrated on the chip (system on chip-SOC or cache memory). 6T SRAMs are volatile refresh independent power-efficient memory which can be integrated on a chip. Fig. 6.13 shows the schematic of an SRAM cell. An SRAM cell consists of two access transistors connected to the bit lines and two inverters

connected back-to-back so that the stored bit stays inside one of the inverter pairs. WL line controls the bit lines. For better circuit performance an SRAM should be immune to noise, have good read stability, write ability and should have a fast response (low access time) (Grossar *et al.*, 2006; Gadhe and Shirode, 2013). In this section we have analyzed RNM, WNM, read stability, write ability and access time of 6T SRAM with ion-implanted CG-JAM MOSFET. RNM is the maximum DC noise voltage that the storage node can tolerate without changing its contents at the storage node (Dhanumjaya and Sudha, 2012; Gadhe and Shirode, 2013). It is gauged by the side of the square which could be fitted inside the butterfly curved formed by two VTC read curves. It is obtained by the VTC curve of the cross-coupled inverter under operating conditions BL, BL' and WL=V_{DD}. Fig. 6.14(a) shows the butterfly diagram for RNM analysis. From fig 14(a) it could be observed that RNM increases with a decrease in straggle length. The RNM for 1 nm straggle length is 196 mV, which is 25% higher as compared to 157 mV for 9 nm straggle length device. Hence, lower straggle length increases the RNM of the device. RNM is also a measure of read stability of the device. WNM may be defined as the minimum bit line voltage required to flip the state of the cell. It is obtained by the VTC curve of the cross-coupled inverter at asymmetric bit conditions by keeping BL and WL at V_{DD} and $\overline{BL}$ at 0. It may be gauged by side of square that fits into the asymmetric VTC curve. Fig 14(b) shows WNM butterfly analysis. From fig. 6.14(b) it could be noted that the WNM also increases with a decrease in straggle length. WNM of 1nm straggle length device is found to be 400 mV, which is 6.9% higher than 374 mV of 9 nm straggle length device. WNM may be defined as the maximum noise voltage at bit lines during a successful write. It is also a measure of write ability of the device (Gadhe and Shirode, 2013; Mukherjee *et al.*, 2015). It should also be noted that a write operation fails when DC noise voltage exceeds WNM. Therefore, a lower straggle length device can tolerate more noise voltage during a successful write operation. Fig 6.15 shows N-curve analysis and measurement setup for the same. N-curve analysis is

important for accurate estimation of read stability and write ability of an SRAM cell (Grossar *et al.*, 2006; Kranti *et al.*, 2010). Static voltage noise margin (SVNM) is a measure of maximum DC voltage that a cell can tolerate before modifying its contents. Static current noise margin (SINM) is defined as the maximum current that a cell can handle before flipping its contents. Both SVNM and SINM are a measure of the read stability of the device. SVMN is the span of the first lobe of N-curve where SINM is the peak of it (Alorda and Torrens, no date). On careful observation, it may be noted that both SVNM and SINM increase with a decrease in straggle length. Therefore lower straggle length devices have better read stability than higher straggle length devices (Samson and Srinivas, 2008; Dhanumjaya and Sudha, 2012). From the second inverted lobe of the N-curve, we could observe write trip voltage (WTV) and write trip current (WTI). WTV is the span of the second lobe whereas WTI is the negative peak of it. WTV may be defined as DC voltage drop required to modify the content of the cell. WTI is the extent of DC current injected into the memory cell to change the bits (Alorda and Torrens, no date). Both WTV and WTI describe write ability of the device. Lower values of these parameters signify better write ability of the device (Samson and Srinivas, 2008). It could clearly be observed from fig 16(a) that both WTV and WTI decrease with a decrease in straggle length. On careful observation, it is found that SVNM, SINM, WTI, and WTV for 1 nm straggle length are 588 mV, 10.16 μA, 1.91 μA, and 282 mV whereas for 9 nm straggle length device are 356 mV, 9.78 μA, 3.96 μA and 490 mV respectively. Therefore, it could be inferred that lower straggle length device presents with better write ability than its higher straggle length counterpart.

Technological advancement is creating the need for faster SRAM cells. Therefore, to cope with the advancement of technology the RAT and WAT of the SRAMs should be as low as possible. RAT is the difference in time between the points where bit line voltage decreases by 50 mV from V_{DD} after the activation of WL (Samson and Srinivas, 2008; Prakash, 2018). Fig 16(a) shows the assessment of RAT for various straggle lengths whereas fig. 6.16(b) shows the

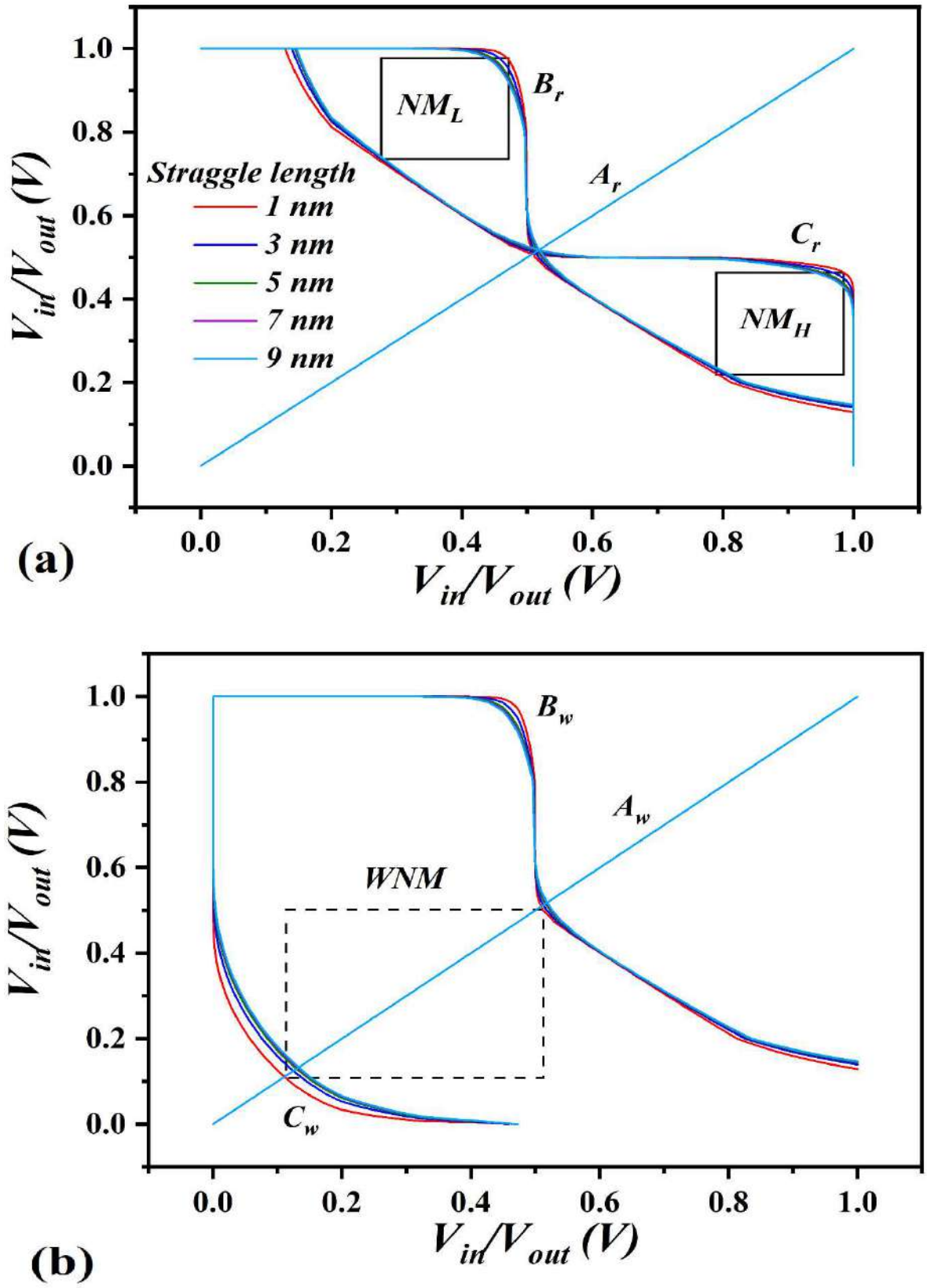
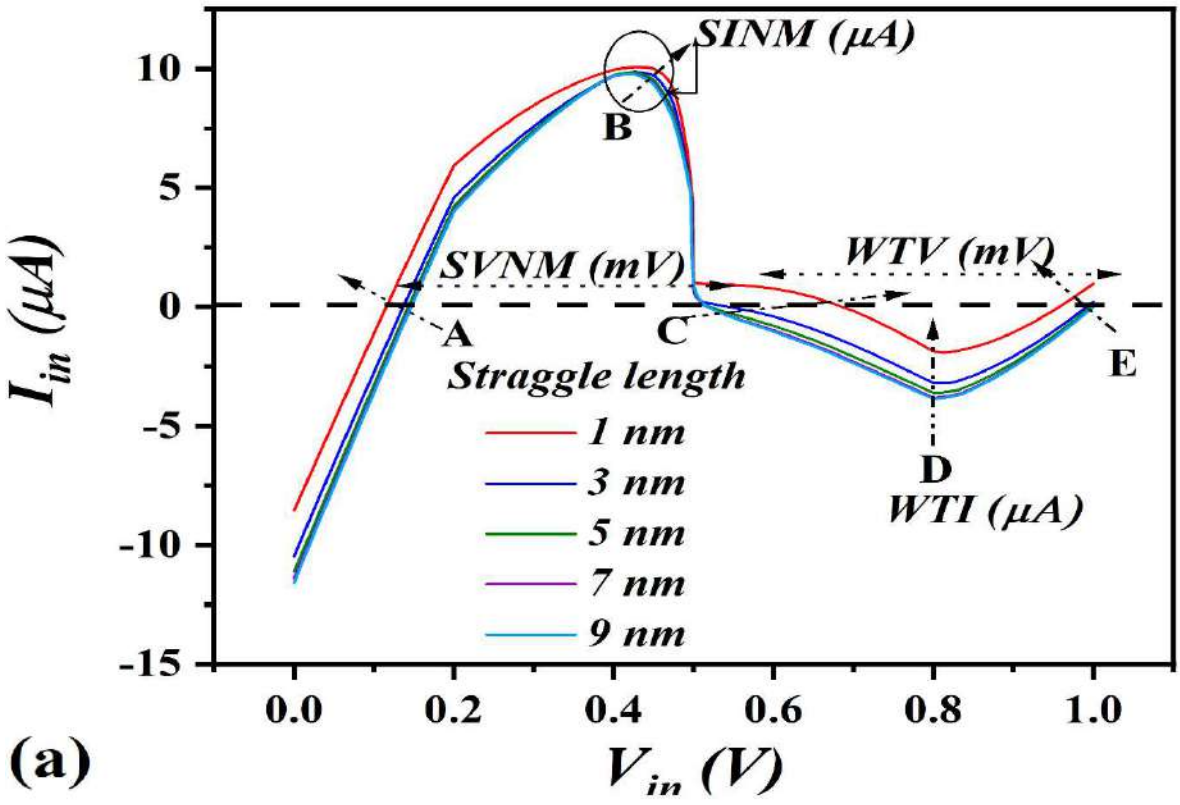


Fig. 6.14: (a) Variation of read noise margin (RNM) of SRAM with straggle length; (b) variation of write noise margin (WNM) with straggle length.



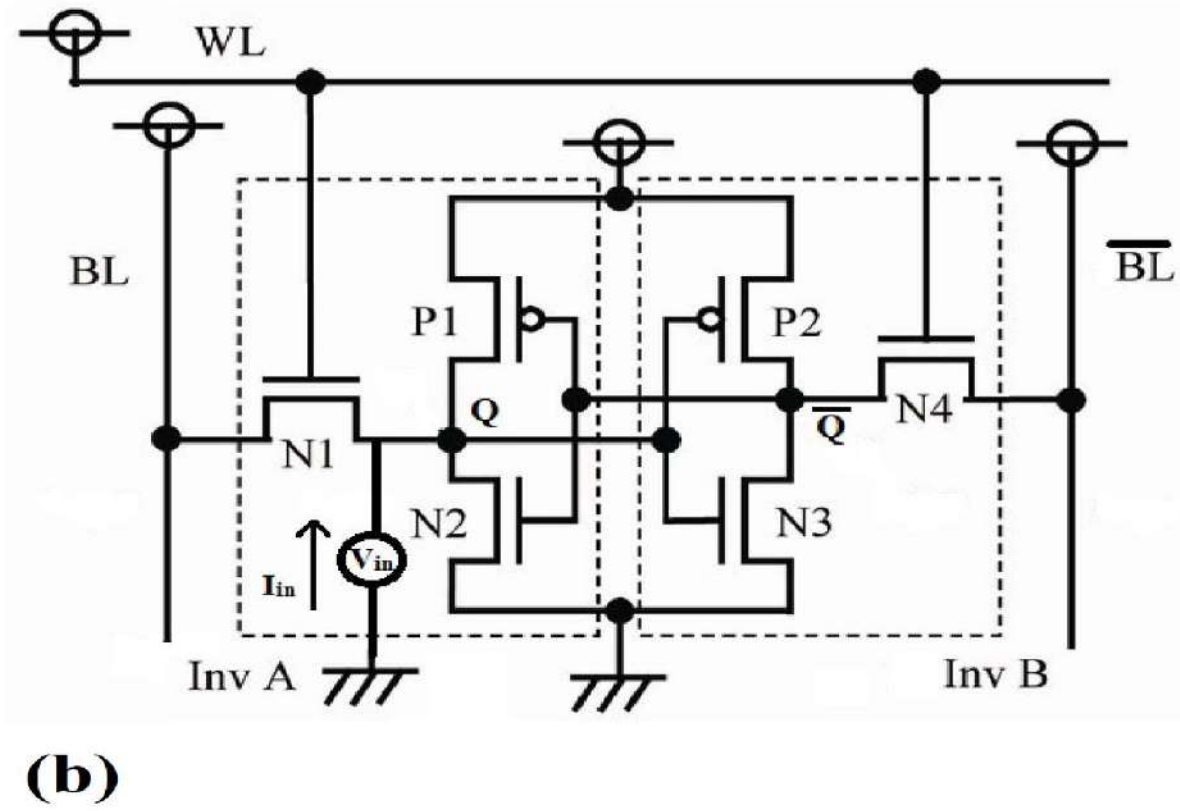


Fig. 6.15: (a) Variation in N-curve of SRAM with straggle length; (b) setup for N-curve measurement.

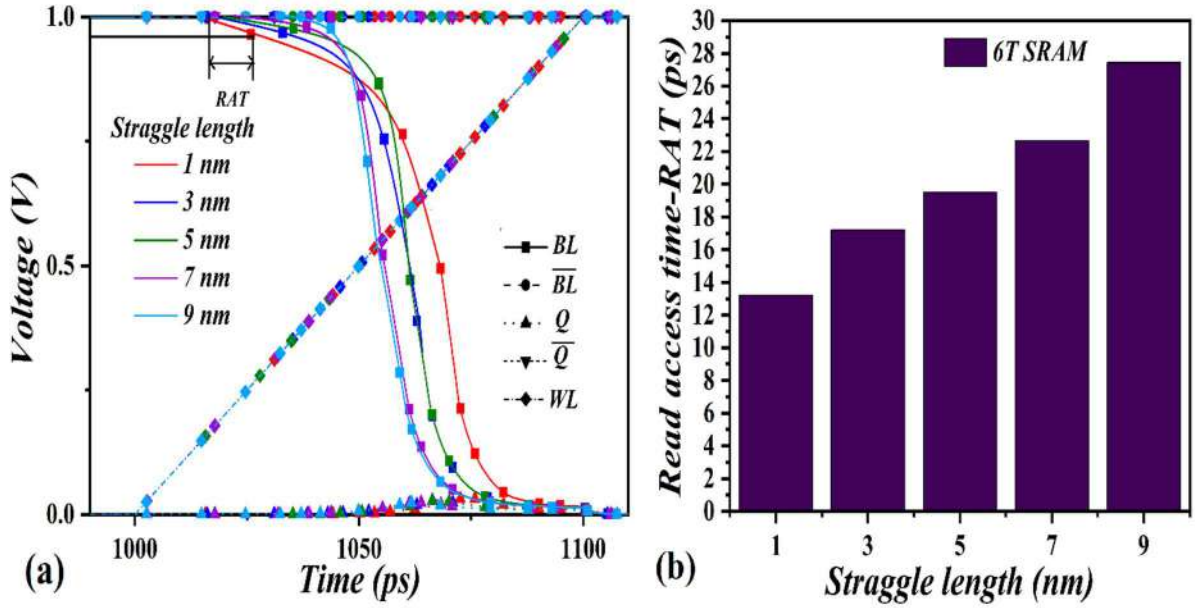


Fig. 6.16: (a) Assessment of RAT for different straggle lengths; (b) variation of RAT with straggle length.

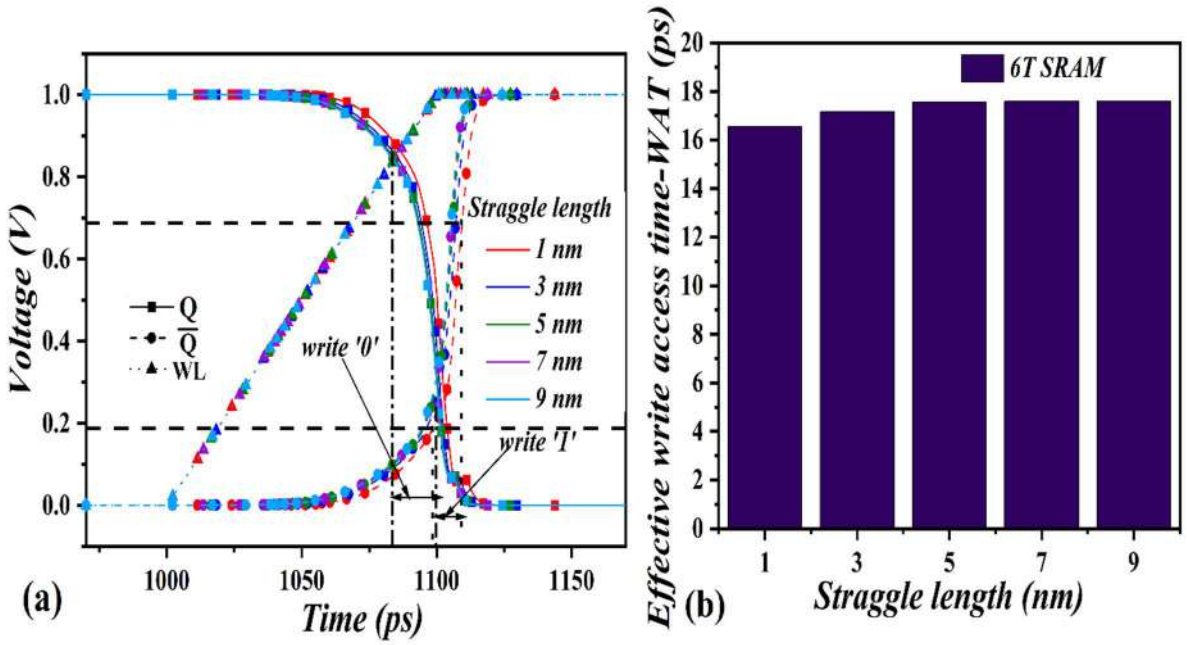


Fig. 6.17: (a) Assessment of WAT for different straggle lengths; (b) variation of effective WAT with straggle length.

variation of RAT with straggle length. It should be noted that RAT decreases with a decrease in straggle length. RAT increases by 24.34% when 1 nm and 9 nm straggle length devices are compared. WAT may be defined as the time required to flip the logic of the stored bit and is

estimated as the time duration between the WL activation time to the time when the opposite node ($\bar{Q}$) charges up to 90% of V_{DD} or discharges to 10% of V_{DD} depending on data written at Q and whichever is the worse (Samson and Srinivas, 2008; Prakash, 2018).

Fig. 6.17(a) shows the assessment methodology of WAT for various straggle lengths. From fig. 6.17(b) it could be observed that WAT also decreases with a decrease in straggle length. WAT of 1 nm device decreases by 6.1% when compared to the device with 9 nm straggle length. Therefore, it may be concluded that both RAT and WAT decrease with a decrease in straggle length. It should be noted that both RAT and WAT depend on C_{gg} and C_{gs} of the access transistors and therefore is lower for lower straggle length devices (Samson and Srinivas, 2008; Prakash, 2018). Therefore, lower straggle length devices are faster to read and write.

6.4 Conclusion

A detailed device and circuit-level analysis of ion-implanted CG-JAM MOSFET has been performed in this chapter. Ion implantation causes a Gaussian type of doping profile inside the channel along the radius r. various parameters have been compared against different straggle lengths (1 nm, 3 nm, 5 nm, 7 nm, and 9 nm) of the Gaussian doping profile. As the straggle length increases the Gaussian doping approaches uniform doping profile. The device-level analysis contains DC and RF analysis. It was found that although the device with the lowest straggle length has least on-current, it presents with the highest I_{ON}/I_{OFF}, g_d and threshold voltage. The lowest straggle length device excels in all RF parameters. Further, a CMOS inverter has been implemented with a complimentary ion-implanted CG-JAM p-MOSFET. Circuit level analysis consists of DC and transient level analysis of CMOS inverter. From the above analysis, it was indicated that the lowest straggle length device has the least power dissipation and highest noise margin but also suffers from high propagation delay. Furthermore, a 6T SRAM cell has been implemented and analyzed for read stability, write ability and access time. From the above investigation, it was found the device with the lowest

straggle length not only has the highest read stability and write ability but also have the least access time. Therefore, it could be concluded that as the straggle length decreases the device becomes fit for circuit applications with a trade-off between propagation delay.