2-D Analytical Modeling and Simulation of Gate and Drain Leakage Currents in CG GC-DM-JAM MOSFET

2.1 Introduction

It is already discussed that the cylindrical gate-all-around (GAA) or nanowire structures are reported to have better gate controllability, smaller short-channel effects (SCEs) and negligible corner effects over other multi-gate structures in MOSFETs (Song *et al.*, 2009). It is also discussed that JAM MOSFETs have higher drive current over the conventional junctionless (JL) MOSFETs (Choi *et al.*, 2014). However, they are reported to suffer from higher leakage currents, and higher hot carrier effects (HCEs) due to high lateral electric field near channel/drain interface than the JL MOSFETs (Poorter and Zoestbergen, 1984; Sahay and Kumar, 2016). Literatures suggest that dual material (DM) gate engineering can reduce the HCEs and BTBT currents (Baruah and Paily, 2014) while graded-channel engineering can reduce the effects of SCEs and HCEs in JL/JAM MOSFETs (Cong *et al.*, 2014; Li *et al.*, 2014; Pratap *et al.*, 2014a, 2015, 2016; Kumari *et al.*, 2015; Chauhan *et al.*, 2017; Bousari, Anvarifard and Haji-Nasiri, 2019; Goel *et al.*, 2019; Priya and Balamurugan, 2019). The literature also shows that that a graded channel in multi-gate structure also reduces the SCEs and HCEs in the MOS transistors (Chen *et al.*, 2013) *(*Goel *et al.,* 2016). In view of the above observations, the present chapter is devoted for developing a theoretical framework for the analysis of drain current and gate leakage current characteristics of the cylindrical gate (CG) graded channel (GC) dual-material (DM) JAM MOSFET possibly for the first time in the literature. Unlike the doping consideration in the IM MOSFET reported by Chen *et al.* (Goel *et al.,* 2016), the channel of our proposed CG-GC-DM JAM MOSFET consists of a lower doping level near the

source side than that of the drain-side region. Since GIDL and gate leakage are important parameters for the MOS transistors, they have been also modelled in addition to the modeling of the drain current for the first time in the JAM MOSFET structures.

In this chapter, we report a 2-D analytical model for various electrical parameters such as central potential, lateral electric field, threshold voltage, roll-off, DIBL, and subthreshold slope (SS). Leakage current reliability issues has also been addressed by modeling the complete drain current (considering GIDL) and gate leakage current in CG-GC-DM-JAM MOSFETs. The 3-D Poisson's equation in cylindrical coordinates has been solved to obtain the channel potential using the superposition technique. The potential function has then been used for modeling various performance parameters mentioned above. We have also compared our proposed device performance parameters with those of the DM-JAM and GC-JAM for various control and screen gate lengths to show the superiority of the proposed JAM MOSFET. The validity of the models have is established by comparing the theoretical results with the commercial 3-D TCAD (COGENDA^{TM}) device simulation data. The layout of this chapter is given below:

Section 2.2 presents the 2-D analytical modeling of the channel potential, channel electric field, threshold voltage, roll-off, DIBL, SS, total drain current (including GIDL) and gate leakage current of the CG GC-DM JAM MOSFET. Some important model results and related discussions have been presented in Sec. 2.3. Finally, Sec. 2.4 includes the summary and conclusion of the present chapter.

2.2 Analytical modeling

Fig. 2.1 shows the 2-D view of the modeled GC-DM-JAM MOSFET structure. Here L, L_1, and L_2 represent the length of the channel, control, and screen gate lengths ($L=L_1+L_2$) respectively. The radial and applicate (length axis) are denoted by r and z, angular axis θ is not shown due to the 2-D nature of the figure. Φ_{m1}, Φ_{m2} represent control and screen gate

workfunctions. n, n^+ and n^{++} represent moderately, highly and degenerately doped n-type semiconductors respectively.

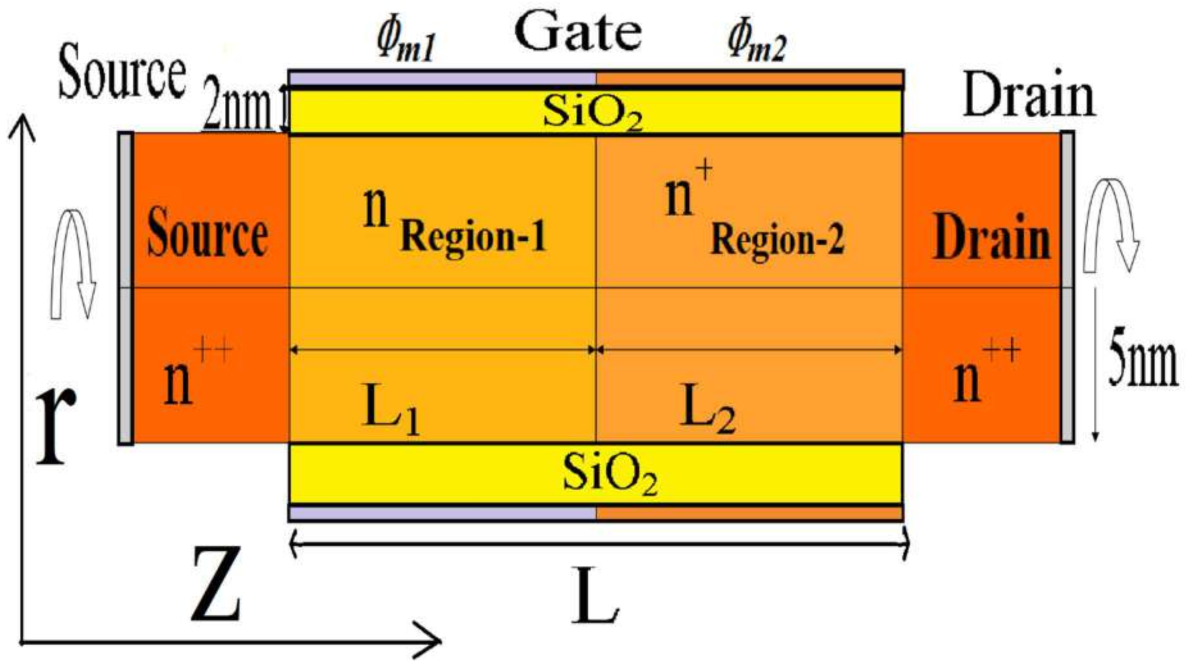


Fig. 2.1: Cross-section view of cylindrical gate GC-DM-JAM MOSFET.

Moreover, gate material with higher work function (tungsten) has been considered in the control gate region (Region 1) and lower work function gate material (copper) over the screen gate region (Region 2). The graded channel can possibly be fabricated using asymmetric halo-doping as used in (Pavanello *et al.*, 2001) Oxide thickness t_{ox} has been taken to be 2 nm. Due to very heavy doping in the source-drain region, depletion region extension in source and drain region is negligible, hence been neglected in the model formulation (Najmzadeh *et al.*, 2012; Gupta, 2015)

2.2.1 Modeling of device potential

Since charge density remains the same throughout the angular coordinate (0-2π) for a given radial distance from the center. Therefore, potential is invariant in θ and has not been considered for the cylindrical Poisson's equation. Poisson's equation in cylindrical coordinates could be written as (Cong *et al.*, 2014):

$$\frac{d^2\psi_j(r,z)}{dz^2}+\frac{1}{r}\frac{d}{dr}r\frac{d\psi_j(r,z)}{dr}=-\frac{qN_{,j}}{\varepsilon_{Si}}\left[1-exp\left[\frac{\psi_j(r,z)-V_{f,j}}{v_t}\right]\right] \quad (2.1)$$

Let the potential distribution function in the channel RegionR_j for$(j=1,\ 2)$ (where R_1 and R_2 represent Regions-1 and 2 respectively as shown in Fig. 1) can be represented as: $\psi_j(r,z)$, where V_T is the thermal voltage of 25.9 mV at room temperature and $V_{f,j}$ is the quasi-fermi level for the region. Appling depletion approximation for junctionless MOSFET in (1), the 2-D potential distribution $\psi_j(r,z)$ in the channel region R_j, $j=1,\ 2$ has been obtained by solving the following Poisson's equations:

$$\frac{d^2\psi_j(r,z)}{dz^2}+\frac{1}{r}\frac{d}{dr}r\frac{d\psi_j(r,z)}{dr}=-\frac{qN_j}{\varepsilon_{Si}},\ j=1,\ 2 \quad (2.2)$$

where, N_1 and N_2 are the doping concentrations of the channel region R_j,$(j=1,\ 2)$ for GC-JAM MOSFET and GC-DM-JAM MOSFET; whereas for DM-JAM MOSFET $N_1=N_2$. Similarly $\phi_{m,j}$ is the gate material workfunction forR_j,$(j=1,\ 2)$ for GC-DM-JAM and DM-JAM MOSFET, whereas for GC-JAM MOSFET$\Phi_{m1}=\Phi_{m2}$. It should be noted that both DM-JAM and GC-DM-JAM MOSFET have $\Phi_{m1}>\Phi_{m2}$. q and ε_{Si} are the electrostatic charge and permittivity of substrate materials (*e.g.,* Si), respectively.

The superposition technique is valid for a linear homogeneous system of equations. Moreover, the potential formulation by this method is limited to the device with a gate length greater or equal to 20 nm. Quasi ballistic modeling of device potential should be considered to model devices with gate length below 20 nm. Appling superposition technique to solve the Poisson's equation of (2) by separating them into 1-D Poison's equation (long channel), $\phi_j(r)$ and 2-D Laplace equation (short channel), $v_j(r,z)$ and can be expressed as (Li *et al.*, 2013; Goel *et al.*, 2019; Priya and Balamurugan, 2019).

$$\psi_j(r,z)=v_j(r,z)+\phi_j(r) \quad (2.3)$$

$$\frac{1}{r}\frac{d}{dr}r\frac{d\phi_j(r)}{dr} = -\frac{qN_j}{\varepsilon_{Si}} \tag{2.4}$$

$$\frac{d^2v_j(r,z)}{dz^2} + \frac{1}{r}\frac{d}{dr}r\frac{dv_j(r,z)}{dr} = 0 \tag{2.5}$$

Due to moderately-high to high doping of the channel, there might be band gap narrowing and change in electron affinity. To incorporate these effects in our present model, we have included the Slotboom and Graaf model under moderately-high to heavily doped conditions (Najmzadeh *et al.*, 2012; Pratap *et al.*, 2015).

$$\Delta E_{g,j} = \beta_E\left(ln(N_j/\beta_N) + \sqrt{ln(N_D/\beta_N)^2 + \beta_C}\right) \tag{2.6}$$

$$E_{g,j}^{eff} = E_g - \Delta E_{g,j} \tag{2.7}$$

$$\chi_j^{eff} = \chi + \Delta E_{g,j}/2 \tag{2.8}$$

where, $\beta_E = 6.92 \times 10^{-3}$eV, $\beta_N = 1.3 \times 10^{17}$cm^{-3}and $\beta_C = 0.5$ are some empirical constants at room temperature; $E_{g,j}^{eff}$ and $\chi_j^{eff}$are the effective energy bandgap and electron affinity after incorporating the above model. E_g and χ are the energy bandgap and electron affinity of the semiconductor material.

For long channel potential,$\phi_j(r)$ and short-channel potential $v_j(r,z)$ can be solved by the following boundary conditions as (Trivedi *et al.*, 2013):

$$\left.\frac{d\psi_j(r,z)}{dr}\right|_{r=0} = 0 \tag{2.9}$$

$$\varepsilon_{Si}\left.\frac{d\psi_j(r,z)}{dr}\right|_{r=R} = C_{ox,j}\left[V_{GS} - V_{fb,j} - \psi_j(r,z)\right] \tag{2.10}$$

$$\varepsilon_{Si}\left.\frac{dv_{(j)}(r,z)}{dr}\right|_{r=R} = C_{ox,j}\left[v_j(r,z)\right] \tag{2.11}$$

$$v_1(r,0) = V_{bi,1} - \phi_1(r) \tag{2.12}$$

$$\nu_2(r, L) = V_{bi,2} - \phi_2(r) - V_{DS} \tag{2.13}$$

$$V_{bi,j} = V_T \, ln\left(N_{S,D}/N_j\right) \tag{2.14}$$

where, V_{GS} and V_{DS} are the gate-to-source voltage and drain-to-source voltage, respectively. $V_{fb,j} = \varphi_{m,j} - \varphi_{s,j}$ is the flat band voltage and $\phi_{m,j}$ is the metal workfunction for regionsR_j,$(j = 1, 2)$;$\varphi_{s,j}$is the semiconductor potential is given by$\varphi_{s,j} = \chi_j^{eff} + E_{g,j}^{eff}/2q - \varphi_{f,j}$ and $\varphi_{f,j} = V_T \, ln\left(N_j/n_i\right)$, (where n_i intrinsic concentration of the substrate material) $\varphi_{f,j}$is the Fermi level for regions R_j;*(j=1,2),*$\varepsilon_{ox}$and$C_{ox} = \varepsilon_{ox}/t_{ox'}$ permittivity and gate-oxide capacitance $t_{ox'} = R \, ln(1 + t_{ox}/R)$ is the effective gate-oxide thickness; V_T and R are the thermal voltage and radius of the device; $V_{bi,j}$ represent the barrier potential at source/channel and drain/channel junction for regions R_j,$(j = 1, 2)$ respectively. Following the methodology adopted by [10], [26], the Eq. (4) and (5) for corresponding long channel potential function,$\phi_j(r)$ and short-channel potential function, $\nu_j(r, z)$ can be solved by above boundary condition and expressed as:

$$\phi_j(r) = \left[\frac{-qN_j}{4\varepsilon_{Si}} r^2 + \frac{qN_jR^2}{4\varepsilon_{Si}} - \frac{qN_j}{2C_{ox}} + V_{GS} - V_{fb,j}\right] \tag{2.15}$$

$$\nu_j(r, z) = \sum_1^\infty J_0\left(\frac{\beta_n \, r}{R}\right)\left[C_{n,j} \, e^{\frac{\beta_n z}{R}} + D_{n,j} \, e^{\frac{-\beta_n z}{R}}\right] \tag{2.16}$$

where β_n are the eigenvalues which must satisfy the following condition:

$$J_0(\beta_n) = -\frac{\varepsilon_{Si}\beta_n}{C_{ox}R} J_1(\beta_n) \tag{2.17}$$

where J_0 and J_1 are the Bessel's function of order 0 and 1, respectively. $C_{n,j}$ and $D_{n,j}$ are constants for regions R_j,$(j = 1, 2)$ which is determined by boundary conditions and continuity equation Eq (18)-(19) and are given by Eq (25), (26):

$$\psi_1(r, L_1) = \psi_2(r, L_1) \tag{2.18}$$

$$\frac{d\psi_1(r,L_1)}{dz} = \frac{d\psi_2(r,L_1)}{dz} \tag{2.19}$$

In Eq. (12)-(13) and (18)-(19) by removing the summation by multiplying with $\int_0^R \frac{\beta_n}{R} r J_0\left(\beta_n \frac{r}{R}\right) d\left(r\frac{\beta_n}{R}\right)$ and integrating, we derive the following equations:

From Eq. (12) and (13) we get

$$C_{n,1} + D_{n,1} = D_{12} \tag{2.20}$$

$$C_{n,2}\, exp\left(\frac{\beta_n L}{R}\right) + D_{n,2}\, exp\left(\frac{-\beta_n L}{R}\right) = D_{11} \tag{2.21}$$

Form Eq. (18)-(19) we get

$$u\left[C_{n,1}\, exp\left(\frac{\beta_n L_1}{R}\right) + D_{n,1}\, exp\left(\frac{-\beta_n L_1}{R}\right)\right] - b_1 V + a_1 w = u\left[C_{n,2}\, exp\left(\frac{\beta_n L_1}{R}\right) + D_{n,2}\, exp\left(\frac{-\beta_n L_1}{R}\right)\right] - b_2 V + a_2 w \tag{2.22}$$

$$u = \frac{\beta_n^2[J_0{}^2(\beta_n) + J_1{}^2(\beta_n)]}{2},\; w = \beta_n J_1(\beta_n),\; b_j = \frac{-qN_j R^2}{4\varepsilon_{Si}} \tag{2.23}$$

$$V = [\beta_n J_1(\beta_n) - 2J_2(\beta_n)],\; a_j = \left[V_{GS} - V_{fbi} + \frac{qN_j R^2}{4\varepsilon_{Si}} + \frac{qN_j R}{2C_{ox}}\right] \tag{2.24}$$

$$\begin{pmatrix} \boldsymbol{C_{n,1}} \\ \boldsymbol{D_{n,1}} \end{pmatrix} = \frac{1}{\Delta}\begin{pmatrix} \mathbf{1} & exp(-\beta_n L/R) \\ \mathbf{-1} & exp(\beta_n L/R) \end{pmatrix} \begin{pmatrix} A_{11} + Q_{11} \\ D_{11} \end{pmatrix} \tag{2.25}$$

$$\begin{pmatrix} \boldsymbol{C_{n,2}} \\ \boldsymbol{D_{n,2}} \end{pmatrix} = -\frac{1}{\Delta}\begin{pmatrix} exp(-\beta_n L/R) & -1 \\ -\,exp(\beta_n L/R) & 1 \end{pmatrix} \begin{pmatrix} A_{12} + Q_{12} \\ D_{12} \end{pmatrix} \tag{2.26}$$

$$Q_{11} = \boldsymbol{cosh}\left(\frac{\beta_n \boldsymbol{L_2}}{\boldsymbol{R}}\right)(\boldsymbol{B_{11}} + \boldsymbol{C_{11}}) \tag{2.27}$$

$$Q_{12} = \boldsymbol{cosh}\left(\frac{\beta_n \boldsymbol{L_1}}{\boldsymbol{R}}\right)(\boldsymbol{B_{12}} + \boldsymbol{C_{12}}) \tag{2.28}$$

$$\Delta = 2\left[sinh\left(\frac{\beta_n L}{R}\right)\right],\; A_{11} = \frac{(V_{bi2} + b_2 V - w a_2 + V_{DS})}{u},\; B_{11} = \frac{V(b_1 - b_2)}{u} \tag{2.29}$$

$$C_{11} = \frac{w(a_2 - a_1)}{u},\quad D_{11} = \frac{V_{bi} + b_1 V - w a_1}{u} \tag{2.30}$$

$$A_{12} = \frac{(V_{bi1}+b_1V-wa_1)}{u}, \quad B_{12} = \frac{V(b_2-b_1)}{u} \tag{2.31}$$

$$C_{12} = \frac{w(a_1-a_2)}{u}, \; D_{12} = \frac{V_{bi2}+V_{DS}+b_2V-wa_2}{u} \tag{2.32}$$

2.2.2 Modeling of the lateral electric field

The electric field could be defined as a gradient of potential and can be expressed as:

$$E_{x,j} = -\frac{d\psi_j(r,z)}{dz} \tag{2.33}$$

$$E_{x,j} = \sum_1^\infty J_0\left(\frac{\beta_n r}{R}\right)\frac{\beta_n}{R}\left[C_{n,j}\,exp(\beta_n z/R) - D_{n,j}\,exp(-\beta_n z/R)\right] \tag{2.34}$$

2.2.3 Modeling of threshold voltage

The threshold voltage (V_{th}) is an important parameter for any MOS device and it can be defined as the gate-to-source voltage at which, minimum central potential equals intrinsic Fermi potential for a junctionless device (Gupta, 2015). Since the region R_1has lower doping than the regionR_2, therefore the lowest minimum potential lies in the region R_1. To calculate threshold voltage, we need to calculate the minimum central potential (*i.e.,* at r = 0). Therefore, for obtaining minimum central potential:

$$\left.\frac{d\psi_j(r,z)}{dz}\right|_{r=0,z=z_{min}} \tag{2.35}$$

$$z_{min} = \frac{R}{2\beta_n} ln\left(\frac{D_{n,j}}{C_{n,j}}\right) \tag{2.36}$$

$$\psi_{min}(r, z_{min}) = V_{GS} + a_{0j}\sqrt{C_{n,j}D_{n,j}} \tag{2.37}$$

where, $a_{0j} = a_j - V_{GS}$

Now equating minimum potential to the Fermi potential (φ_{fi}) and changing V_{GS} to V_{th} (Gupta, 2015).

$$\psi_{min}(r, z_{min})|_{V_{GS}=V_{th}} = \varphi_{f,j} \tag{2.38}$$

$$\left(V_{gs} + 2\sqrt{C_{n,j}D_{n,j}}\right)\Big|_{V_{GS}=V_{th}} = V_{tL} \quad (2.39)$$

where V_{tL} is the long channel threshold voltage represented by,

$$V_{tL} = \varphi_{f,j} - a_{0j} \quad (2.40)$$

Since we have considered region R_1 for minimum central potential, therefore (Pratap *et al.*, 2014a; Goel *et al.,* 2016)

Replacing, $A_{11} \Rightarrow E_{12} - F_{12}V_{th}$ and $D_{11} \Rightarrow E_{11} - F_{11}V_{th}$ (2.41)

where, $C_{1,n} \cdot D_{1,n} = G_1 + G_2V_{th} + G_3{V_{th}}^2$ (2.42)

Now threshold voltage could be expressed as:

$$\partial_1{V_{th}}^2 + \partial_2V_{th} + \partial_3 = 0 \quad (2.43)$$

From (34), we can write as [22], [25]:

$$V_{th} = \frac{-\partial_2 \pm \sqrt{({\partial_2}^2 - 4\partial_1\partial_3)}}{2\partial_1} \quad (2.44)$$

$$E_{11} = \frac{1}{u}[V_{bi1} + b_1V - wa_{01})], E_{12} = \frac{1}{u}[(V_{bi2} + b_2V - wa_{02} + V_{DS})], F = \frac{w}{u} \quad (2.45)$$

$$G_1 = M_{11}M_{21}, G_2 = M_{11}M_{22} + M_{12}M_{21}, G_3 = M_{12}M_{22} \quad (2.46)$$

$$\partial_1 = 4G_3 - 1, \partial_2 = 4G_2 + 2V_{tL}, \partial_3 = 4G_1 - {V_{tL}}^2 \quad (2.47)$$

$$M_{11} = \frac{1}{\Delta}\left[E_{12} + N_1 - E_{11}[N_3 - N_2] \rightleftarrows exp\left(\frac{-\beta_nL_1}{R}\right)\right] \quad (2.48)$$

$$M_{12} = \frac{F}{\Delta}\left[[N_3 - N_2]exp\left(\frac{-\beta_nL_1}{R}\right) - 1\right] \quad (2.49)$$

$$M_{21} = \frac{1}{\Delta}\left[-E_{12} - N_1 + E_{11}[N_3 + N_2]exp\left(\frac{\beta_nL_1}{R}\right)\right], M_{22} = \frac{F}{\Delta}\left[1 - [N_3 + N_2]exp\left(\frac{\beta_nL_1}{R}\right)\right] \quad (2.50)$$

$$N_1 = N_2[B_{11} + C_{11}], N_2 = cosh\left(\frac{\beta_nL_2}{R}\right), \; N_3 = sinh\left(\frac{\beta_nL_2}{R}\right) \quad (2.51)$$

2.2.4 Modeling of threshold voltage roll-off and DIBL

Threshold voltage roll-off can be defined as the difference in threshold voltage between the short channel and long channel device and can be expressed as (Cong *et al.*, 2014):

$$V_{roll-off} = V_{th}|_{short \quad hannel} - V_{tL} \tag{2.52}$$

Threshold voltage decreases with high drain voltage for short channel devices called drain induced barrier lowering (DIBL). The (DIBL) is an important property of short channel devices and an important SCEs parameter, which can be expressed as (Li *et al.*, 2014):

$$DIBL = -\frac{V_{th}|_{V_{DS}=0.05\text{V}} - V_{th}|_{V_{DS}=1\text{V}}}{V_{DS}(0.05\text{V}) - V_{DS}(1\text{V})}(\text{mV/V}) \tag{2.53}$$

2.2.5 Drain current modeling

Drain current of a device is an important parameter for switching purposes. Higher the ratio of I_{ON}/I_{OFF} higher is the noise tolerance and swing of the device. Drain current can be derived from the potential and threshold voltage formulations derived above. A complete drain current model for various regions is expressed as (Pratap *et al.*, 2015, 2016);

$$I_{DS} = \begin{bmatrix} I_{btbt} for - 1V \le V_{GS} \le 0V \\ I_{sub} for 0V < V_{GS} \le V_{th} \\ I_{sat} for V_{th} < V_{GS} \le V_{DS} + V_{th} \\ I_{lin} for V_{DS} + V_{th} < V_{GS} \le V_{DD} = 1V \end{bmatrix} \tag{2.54}$$

I_{btbt} could be defined as the gate induced drain leakage due to band-to-band tunneling in the overlap region near the drain junction. BTBT generation rate could be defined as (Bouhdada *et al.,* 1997; Sachdeva, Vashishath and Bansal, 2018; Goel *et al.*, 2019);

$$BTBT_{gen} = A \times E^2{}_{tot}\, exp\left(\frac{-B}{E_{tot}}\right) \tag{2.55}$$

where, $A = \frac{q^2 m_r{}^{0.5}}{18\pi h^2 E_{g,2}{}^{0.5}}$ and $B = \frac{\pi m_r{}^{0.5} E_{g,2}{}^{0.5}}{2\sqrt{2}qh} = 2.13MV/m$

$$E^2{}_{tot} = E^2{}_{si} + E^2{}_{h} \tag{2.56}$$

$$I_{btbt} = 2\pi R^2 \Delta L \times BTBT_{gen} \tag{2.57}$$

$$E_{si} = \frac{qN_{D,S}}{\varepsilon_{si}}\sqrt{\frac{2\varepsilon_{si}\psi_{si}}{qN_{D,S}}},\ E_h = \frac{V_{DS}-V_{GS}}{\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{ox}\varpi\right)^2} \tag{2.58}$$

$$\psi_{si} = (V_{DS}-V_{GS}) - V_{fb,2} + \frac{qN_{D,S}t^2{}_{ox}\varepsilon_{si}}{\varepsilon^2{}_{ox}} \times \left[\sqrt{\left[\frac{qN_{D,S}t^2{}_{ox}\varepsilon_{si}}{\varepsilon^2{}_{ox}} + (V_{DS}-V_{GS}) - V_{fb,2}\right]^2 - \left((V_{DS}-V_{GS}) - V_{fb,2}\right)^2}\right] \tag{2.59}$$

$$\varpi = \frac{10^{-4}R^{2/3}L^{2/5}}{t^{3/4}{}_{ox}},\ \Delta L = \sqrt{\frac{2\varepsilon_{si}\psi_{si}}{qN_{D,S}}} \tag{2.60}$$

where, ΔL is the length of the overlapped area, m_r=0.37m_0 where m_0 is mass of electron at rest, E_{si} and E_h are vertical and horizontal field respectively and h is the Plank constant (Chen, Wong and Wang, 2001).

I_{sub} could be calculated by the minimum potential method as (Pratap *et al.*, 2016);

$$I_{sub} = 2\pi R^2 \mu_{ef,1f} qV_T n_{i,1} \left(\frac{1-\exp\left(\frac{-V_{DS}}{V_T}\right)}{\int_0^L \frac{1}{\int_0^R \exp\left(\frac{\psi_{min}(r, z_{min})}{V_T}\right)dr} dz} \right) \tag{2.61}$$

As the minimum potential is highest for region-1, only region-1 is taken for the calculation (Najmzadeh *et al.*, 2012; Pratap *et al.*, 2014a)

$$\mu_{eff,j} = \frac{\mu_{max}-\mu_{min}}{1+\left(\frac{N_j}{N_{ref}}\right)^{\tau}},\ \mu_{max}=1330 \text{ and } \mu_{min}=65 \text{ cm}^2/\text{Vs},\ N_{ref}=8.5\times10^{16}/\text{cm}^3,\ \tau = 0.73 \tag{2.62}$$

$$I_{sat} = \frac{2\pi R\mu_{eff,2}C_{ox}}{\left(1+\frac{V_{Dsat}}{E_C L}\right)(L-L_{sat})}\left[\begin{array}{l}\rho(V_{GS}-V_{ths})^{\gamma}V_{Dsat} - \frac{\theta_s V^2{}_{Dsat}}{2} \\ +V_T\theta_s\left(1+exp\left(\frac{V_{DS}-V_{Dsat}}{V_T}\right)\right.\end{array}\right] \tag{2.63}$$

$$\theta_s = 0.1 \Big/ \frac{\partial \psi_{\min}(0, z_{\min})}{\partial V_{GS}} \quad \text{at} \quad V_{GS} = V_{th} \tag{2.64}$$

$$V_{ths} = V_{th}(1-\theta_s), \quad E_C = \frac{2V_{sat}}{\mu_{eff,2}} \tag{2.65}$$

$$V_{Dsat} = \frac{V_{GS}-V_{th}}{1+\frac{(V_{GS}-V_{th})\mu_{eff,2}}{LV_{sat}}} \tag{2.66}$$

$$L_{sat} = \lambda\, ln\left(\frac{V_{DS}-V_{Dsat}}{E_C L + \sqrt{1+\left(\frac{V_{DS}-V_{Dsat}}{E_C L}\right)^2}}\right) \tag{2.67}$$

where, γ is a fitting parameter varying between 0.5 to 1.5 for short channel and 2 for long channel MOSFETs. γ taken here is 1.26 (Pratap *et al.*, 2015). L_{sat} is the characteristics length, whereas $\rho$is a fitting parameter depending on technology varying between 0 and 1, whose value taken here is 0.0046. The analytical expression and calculation of its values can be found in (Im *et al.*, 2002). E_C is critical field and$V_{sat}$is the critical velocity assumed as 1.03×10^7cm/s (Pratap *et al.*, 2015, 2016).λ is also a fitting parameter whose value depends on permittivity and thickness of semiconductor and gate oxide given by $\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}$. Current in the linear region could be calculated as below

$$I_{lin} == \frac{2\pi R\mu_{eff,1}C_{ox}}{(E_C L+V_{DS})(L-L_{sat})}\left[(V_{GS}-V_{ths})^{\gamma/2}V_{DS} - \frac{\theta_s {V_{DS}}^2}{2}\right] \tag{2.68}$$

2.2.6 Subthreshold slope modeling

Subthreshold slope (SS) is an essential parameter and important for switching characteristics of the device. SS could be formulated as below (Li *et al.*, 2013);

$$SS = \frac{dV_{GS}}{d\,log(I_{sub})} \tag{2.69}$$

2.2.7 Gate leakage current modeling

Gate leakage current is an important leakage phenomenon responsible for the power dissipation in any circuit applications therefore, we need to minimize this. Direct tunneling through the thin oxide layer is the major cause of gate leakage and is a strong function of applied gate voltage. The major contribution to this current is from direct tunneling of an electron from the conduction band of the substrate to the gate (ECB-electron conduction band tunneling). Considering the trapezoidal tunneling barrier for thin gate oxide (Darbandy, 2013). Gate current density J_G could be expressed as in (Yeo, King and Hu, 2003). Given:

$$J_{G,j}^{dep/acc} = A_G \times C_{G,j}^{dep/acc}(\varphi_{bi}, t_{ox}, E_{ox}V_{GS})\, exp\left\{\frac{-B_G\left[1-\left(1-\frac{|V_{ox,j}|}{\varphi_{bi}}\right)^{3/2}\right]}{3hqE_{ox,j}}\right\} \quad (2.70)$$

$$A_G = \frac{q^2}{8\pi h\varphi_{bi}\varepsilon_{ox}}, B_G = 8\pi\sqrt{2m_{si}\varphi_{bi}^3} \quad (2.71)$$

$$C_{G,j}^{dep/acc} = exp\left[\frac{20}{\varphi_{bi}}\left(\frac{|V_{ox,j}|-\varphi_{bi}}{\varphi_{bo}}+1\right)^{\alpha_G}\left(\frac{1-|V_{ox,j}|}{\varphi_{bi}}\right)\right]\left(\frac{V_{GS}}{t_{ox}}\right)P_j \quad (2.72)$$

$$P_j = C_{ox}\left\{V_T\, ln\left[\frac{1+exp(-V_{GS}+\Delta V_{GS}-V_{fb,j})}{V_T}\right]\right\} \quad (2.73)$$

where, φ_{bi} and $\varphi_{bo}$are tunneling barrier and band offset whose values for Si-SiO_2 are 3.10 eV, m_{Si}=0.37m_0 and α_G=0.6 is a fitting parameter, $\alpha_G$covers most of the secondary effects accounting for the unknown density of states at electrode interface and the effective masses of the oxide. It should be noted that ECB dominates the direct oxide tunneling process for Si-SiO_2-metal for thin gate oxide (Darbandy, 2013) α_G (ECB) for Si/SiO_2 is 0.6. $\Delta V_{GS}$is also a fitting parameter used to fit the base of modeled and simulated curve and given by $V_{GSmax}(V_{DD})$-

V_{th} given in (Yeo, King and Hu, 2003). $V_{ox,j}$ is the potential buildup in the thin oxide layer and is given as:

$V_{ox,j}^{dep/acc} = V_{GS} - V_{fb,j} - \phi_j^{\frac{dep}{acc}}(R)$ and $E_{ox,j}^{dep/acc} = \frac{V_{ox,j}^{dep/acc}}{t_{ox}}$, is the gate oxide electric field

$\phi_j^{dep}(R)$ could be obtained by Eq. (15) putting r=R, whereas,

$$\phi_j^{acc}(R) = V_{Gf,j} + C_R + V_T - 2V_T LW.\left[\frac{C_R R\sqrt{2\delta_j}\, exp\left(\frac{V_{Gf,j}+C_R-V_{ch,i}}{2V_T}\right)}{4V_T}\right] \quad (2.74)$$

$$V_{Gf,j} = V_{GS} - V_{fb,j}, V_{ch,j} = \varphi_{f,j}, C_R = \frac{4\varepsilon_{si}V_T}{RC_{ox}}, \delta_j = \frac{qN_j}{\varepsilon_{si}V_T} \quad (2.75)$$

Where ϕ_j^{dep} and ϕ_j^{acc} are the surface potential in depletion and accumulation respectively for regions R_1 and R2 and *LW.* is LambertW function (Lin *et al.*, 2007). Gate current, I_G, could be expressed as:

$$I_G = \begin{bmatrix} \pi R^2\left(J_{G,1}^{dep}L_1 + J_{G,2}^{dep}L_2\right), for; V_{GS} \le V_{th,2} \\ \pi R^2\left(J_{G,1}^{dep}L_1 + J_{G,2}^{acc}L_2\right), for; V_{th,2} < V_{GS} < V_{th,1} \\ \pi R^2\left(J_{G,1}^{acc}L_1 + J_{G,2}^{acc}L_2\right), for; V_{GS} \ge V_{th,1} \end{bmatrix} \quad (2.76)$$

Where, $V_{th,j}$ are the threshold voltages for region R_1 and R_2 taken as an individual device with length L_1 and L_2=L-L_1.

2.3 Result and discussion

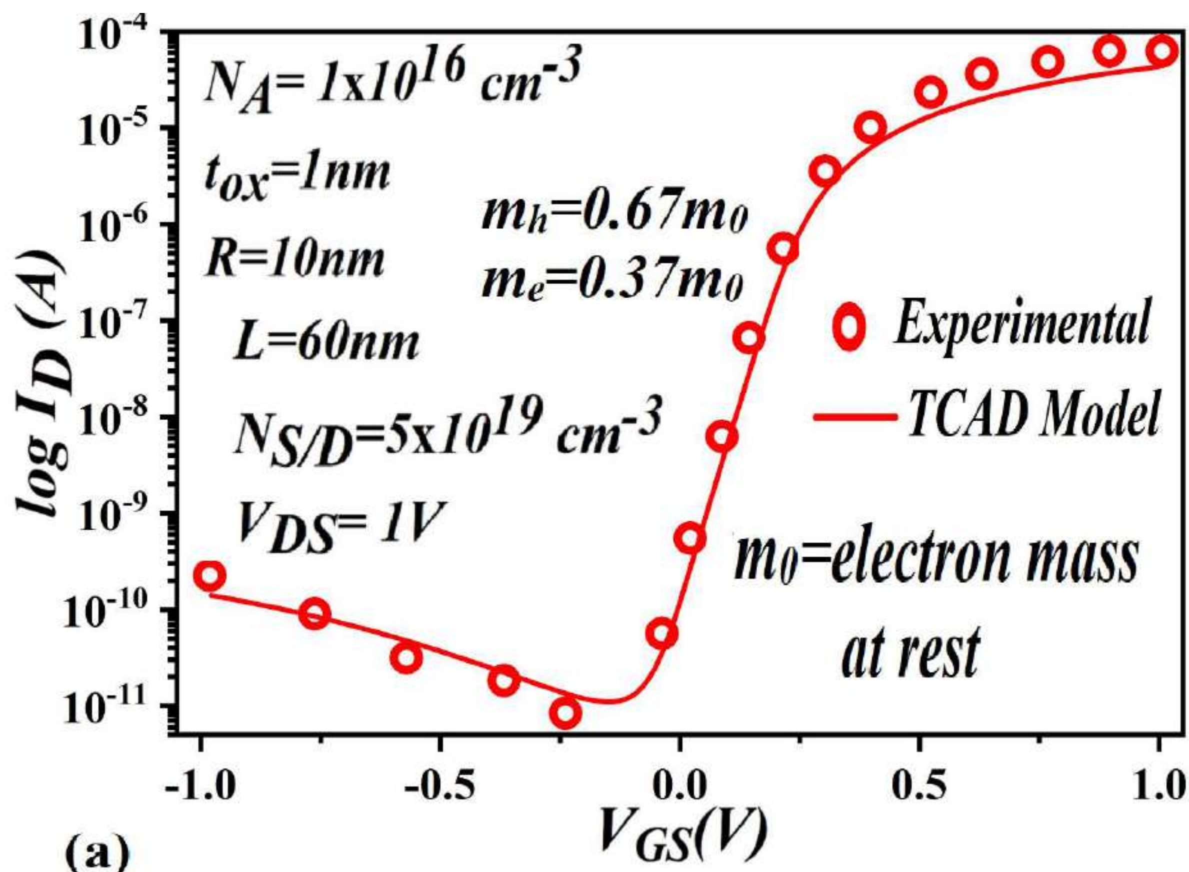
In this section, we have compared our modeled results of proposed GC-DM-JAM and GC-JAM MOSFETs with that of DM-JAM MOSFET for highlighting the merits of our proposed device. For fair comparisons, arithmetic means of doping N_1 and N_2 (graded channel) have been taken for the uniformly doped DM-JAM MOSFET (Trivedi *et al.*, 2013; Li *et al.*, 2014; Pratap *et al.*, 2014a; Goel *et al.,* 2016). Similarly arithmetic mean of gate work functions ϕ_{m1} and ϕ_{m2}

have been taken for GC-JAM MOSFET (Li *et al.*, 2014; Goel *et al.*, 2016). The specifications of the structures are as given in Table 2.1. The analytical results have been validated against 3-D numerical simulation data from TCAD based device simulator from COGENDA™. The *Fermi-Dirac*, *Lucent mobility*, *Bandgap narrowing,* and *HotCarrier*

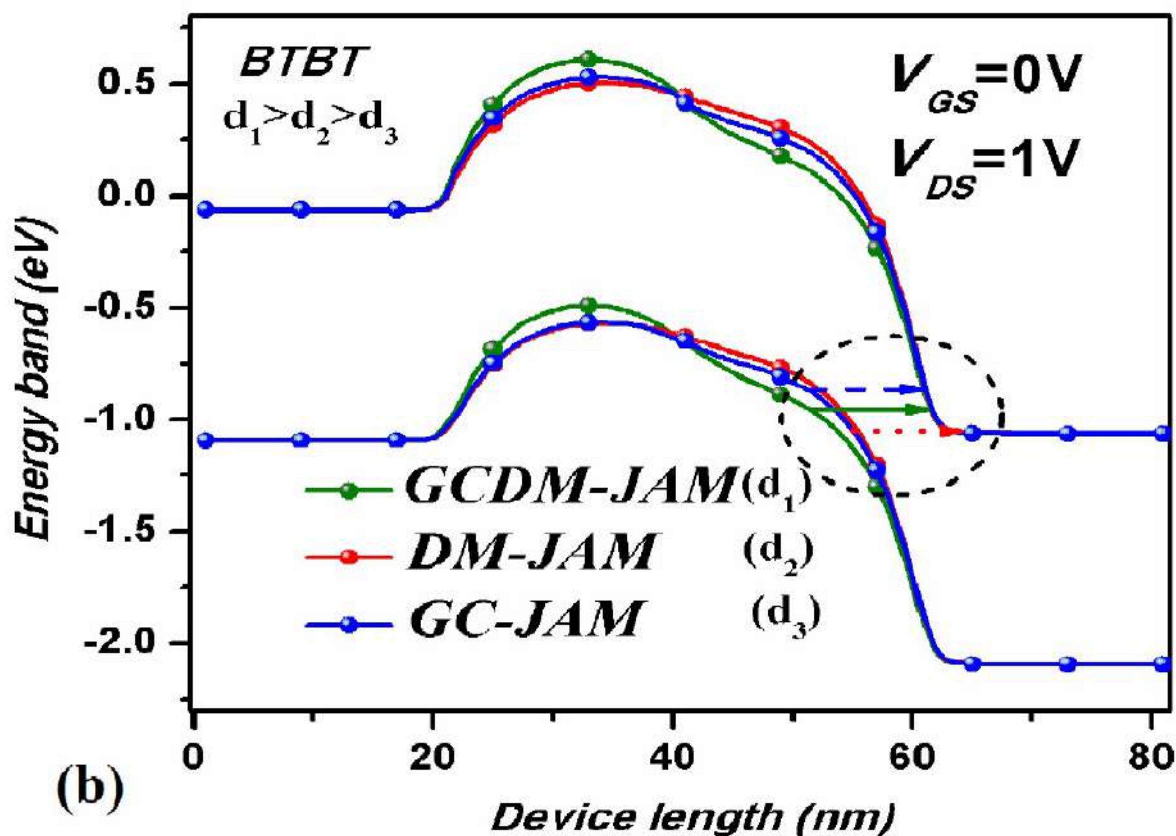
TABLE 2.1: Specifications of different JAM MOSFET structures

MOSFET Type	***Source/Drain Doping (N_S/N_D) (cm^{-3})***	***Channel Doping (cm^{-3}) N_1/N_2***	***Dielectric Gate-oxide***	***Gate Work-function (eV)***
GC-DM-JAM	10^{20}	$10^{18}/10^{19}$	SiO_2	4.9/4.7
GC-JAM	10^{20}	$10^{18}/10^{19}$	SiO_2	4.8
DM-JAM	10^{20}	5×10^{18}	SiO_2	4.9/4.7

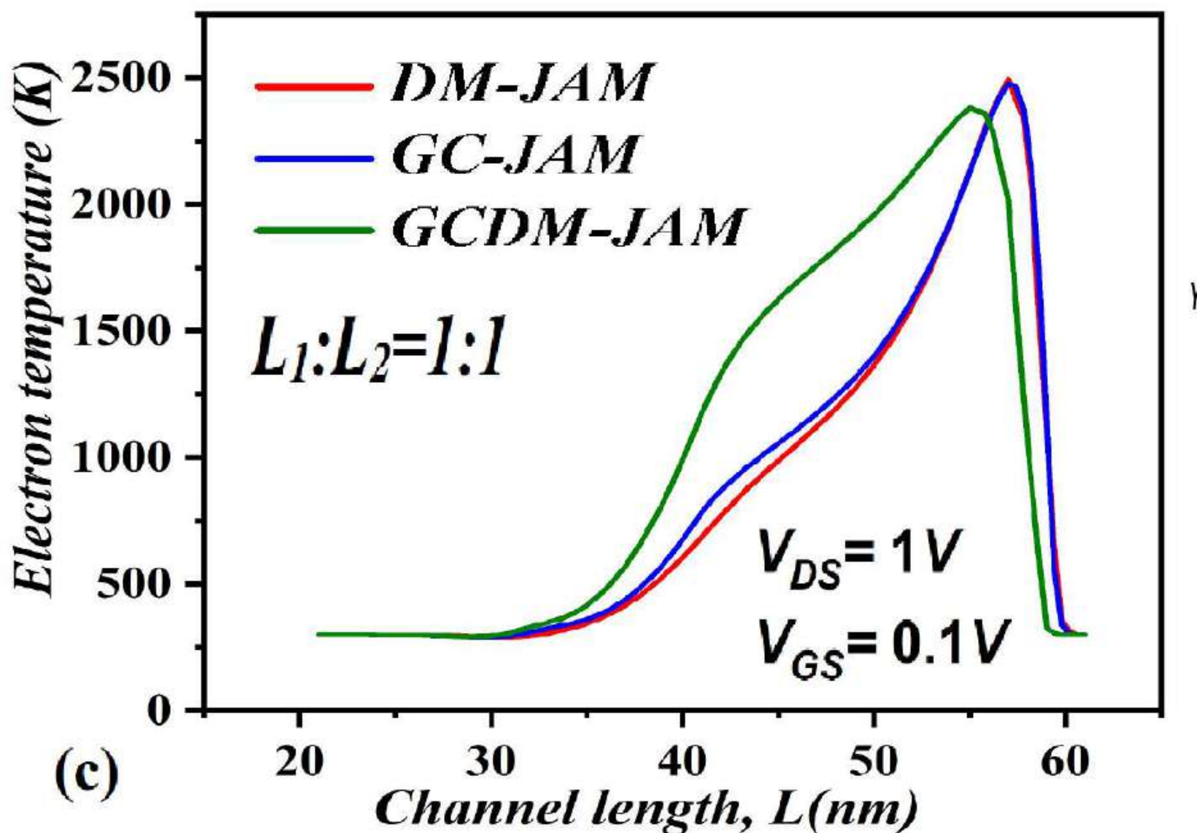
models have been invoked for the 3-D device simulations (VisualTCAD, 2017). Further, *BBT* and *direct tunneling* models have been enabled for GIDL and gate leakage current respectively. The simulated data have been calibrated for electron mass and density of states to match against the experimental data obtained from the I_D-V_{GS} plot as shown in Fig. 2.2(a) (Fan *et al.*, 2015). Fig. 2.2(b) shows the energy band diagram for all three device structures. It could be seen, BTBT width is of the order (GC-DM-JAM>GC-JAM>DM-JAM MOSFET). Therefore, the band-overlapped region near channel/drain junction in GC-DM-JAM MOSFET is minimum due to the longest tunneling width among the three structures. Fig. 2.2(c) shows the variation of carrier temperature against the length of the channel. It could clearly be observed that GC-DM-JAM MOSFET has the lowest carrier temperature near the channel/drain junction. Therefore, having the least impact ionization generated hot carriers. Fig. 2.2(d) shows a simulated 3-D structure of GC-DM-JAM MOSFET.



$N_A = 1x10^{16}\ cm^{-3}$
t_{ox}=1nm
R=10nm
L=60nm
$N_{S/D}=5x10^{19}\ cm^{-3}$
V_{DS}= 1V
$m_h=0.67m_0$
$m_e=0.37m_0$
Experimental
TCAD Model
m_0=electron mass at rest
log I_D (A)
V_{GS}(V)
(a)



BTBT
$d_1>d_2>d_3$
V_{GS}=0V
V_{DS}=1V
GCDM-JAM (d_1)
DM-JAM (d_2)
GC-JAM (d_3)
Energy band (eV)
Device length (nm)
(b)



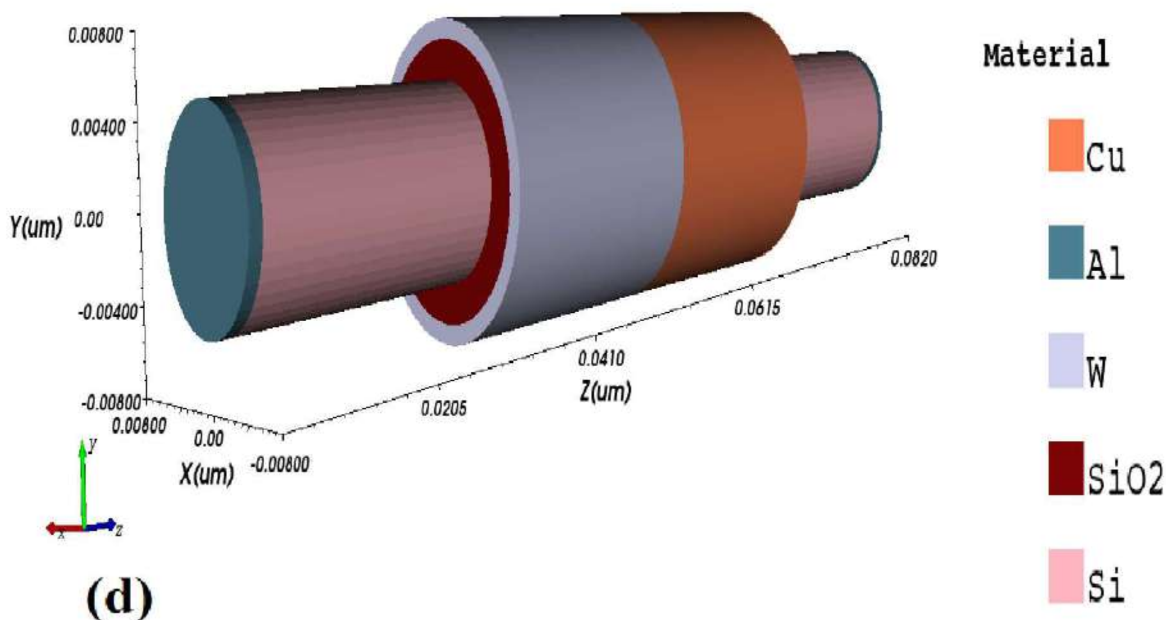
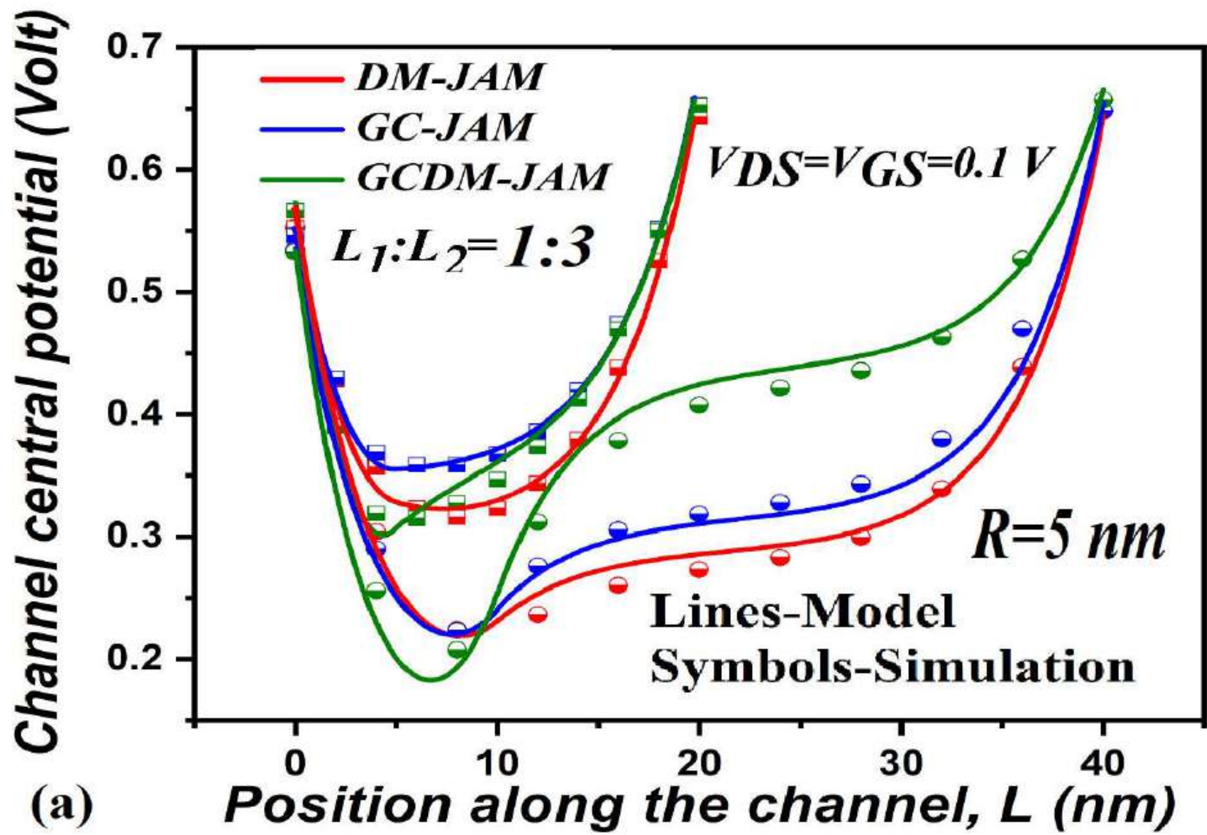


Fig. 2.2: (a) Simulation model calibration against experimental I_d-V_{gs} data of Junctionless-FET from (Fan *et al.*, 2015). (b) Simulated energy band structure for all three devices. (c) Variation of Carrier temperature with a channel length (simulated). (d) A 3-D view of simulated cylindrical gate GC-DM JAM-MOSFET.

In Figures, 2.3-2.7 "L" represents the length of the channel in the z-direction. Fig. 2.3 shows variations of central potential with the length of the channel (L=40 and 20 nm) for all the three different device structures. At radius of R=5nm and V_{GS}= V_{DS} =0.1V for (a) with a ratio of L_1:L_2=1:3 and (b) L_1:L_2=3:1 respectively. It can clearly be observed that GC-DM-JAM has the highest source to channel potential (*i.e.,* highest threshold voltage) among three, thus having the highest immunity to SCE's. As the channel length decreases the barrier potential also decreases for GC-DM-JAM, GC-JAM and DM-JAM, MOSFETs. An analysis of the above figures indicates that the potential barrier increases rapidly with an increase of L_1:L_2, thus reducing the effects of SCEs. It would be interesting to note that with an increase of L_1:L_2 ratio the position of the minimum potential barrier shifts towards the drain side, thereby reducing the reliability towards HCEs. Fig. 2.4 (a) shows variations of central potential with the length of the channel (L=40 and 20nm) for all the three different devices structures at V_{GS}= V_{DS} =$0.1V$ and radius (a) R=5nm, (b) 7nm with a ratio of L_1:L_2=1:1. Furthermore, it could be observed that at a radius of (R=7nm) GC-JAM MOSFET have higher reliability towards SCEs than DM-JAM MOSFET. This can be attributed to the decreased gate-dependent control over SCEs with an increase in radius for the DM-JAM, compared to the doping dependent control over SCEs in GC-JAM MOSFET. Fig. 2.4 (b) shows lateral electric field variations with the length of the channel with a ratio of L_1:L_2=1:1 for a high drain field (V_{GS}=0.1, V_{DS}=$1V$) at R=40 and 20 nm. Fig. 2.5, shows lateral electric field variations with the length of the channel with a ratio of (a) L_1:L_2=1:1, for L=40 and 20 nm (b) L_1:L_2= 1:3 and L_1:L_2= 3:1 for L=40 nm respectively at low drain field (V_{DS}=V_{GS}=0.1V). HCEs are dominant at high drain field and low gate field. It could be observed that the GC-DM-JAM MOSFET has the largest electric field peak and source-side field whereas having the smallest field at the drain side for all ratios of L_1:L_2. From the above observation, it could be inferred that the GC-DM-JAM MOSFET has the best average electric field distribution, higher source acceleration (*i.e.,* speed of the device) and the highest



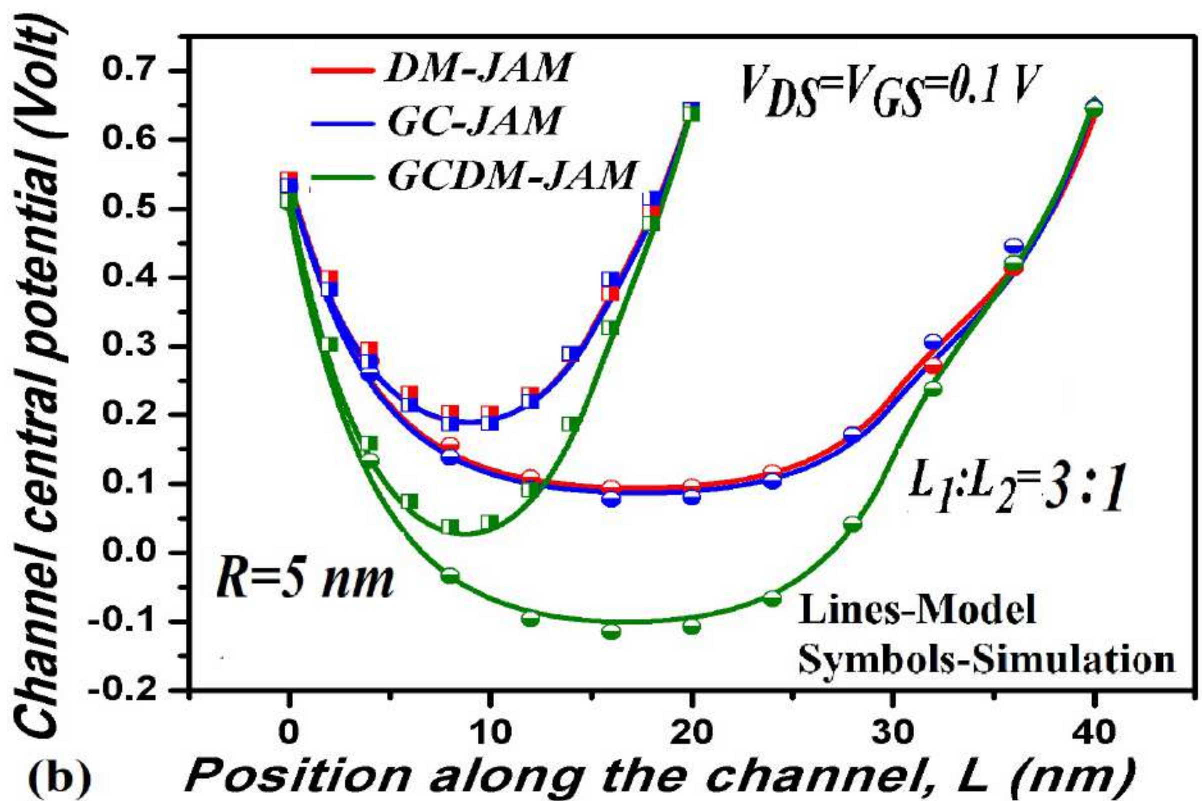
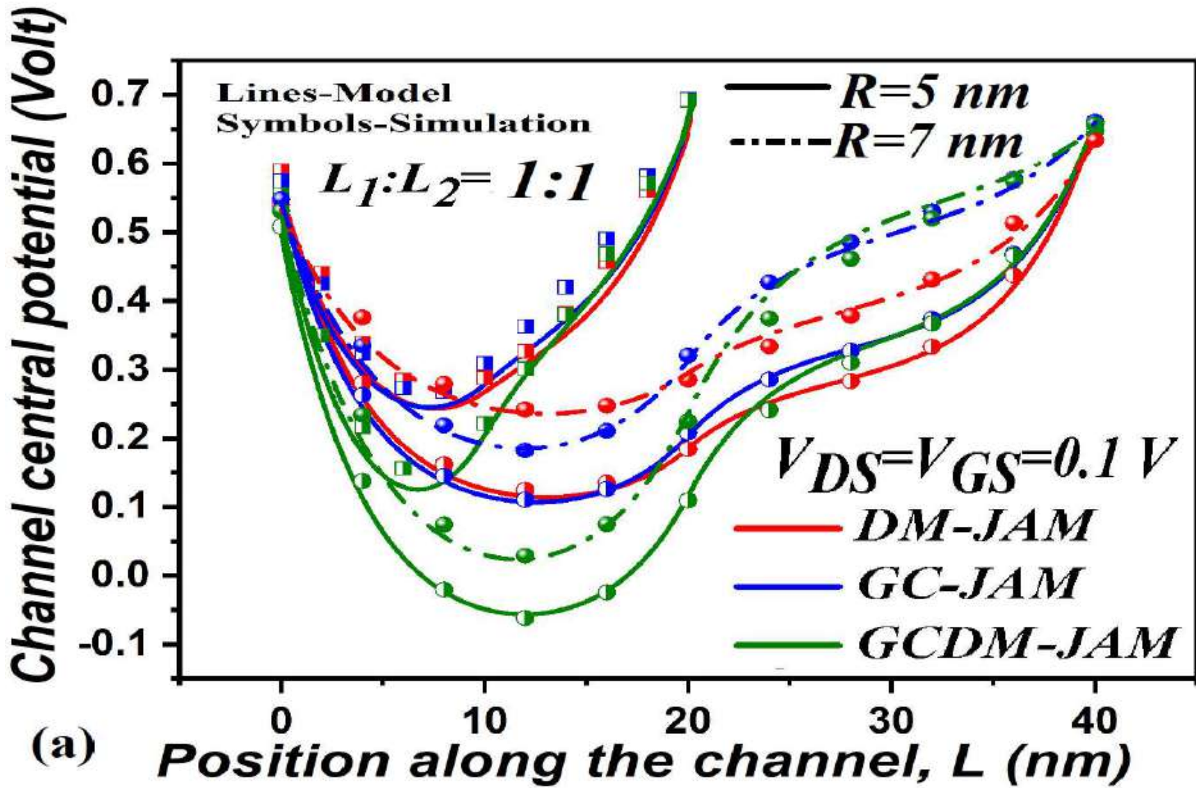


Fig. 2.3: Central channel potential along the channel length at $V_{DS}=V_{GS}$=0.1V, R=5 nm, L=40 nm and 20 nm (a) for L_1:L_2=1:3; (b) L_1:L_2=3:1.

reliability towards HCEs. Further, it could also be observed that with an increase in the ratio of L_1:L_2, the peak electric field shifts towards the drain side. Thereby increasing the effect of the high electric field in the drain side of the channel (Li *et al.*, 2014; Pratap *et al.*, 2014a; Goel *et al.*, 2016). From the detailed analysis of figures 2.3-2.5, it could be observed that SCEs decrease and HCEs increase with an increase in L_1:L_2, therefore we have to choose an optimum value for the same. Thus, for further analysis an optimum value of L_1:L_2=1:1 has been chosen. In Fig. 2.6 and 2.8, "*l*" represents different channel lengths for various technology nodes.

Fig. 2.6 shows the variation of (a) threshold voltage and (b) roll-off against different channel lengths (20-200 nm) for three different device structures at (V_{DS} =0.5 V) with L_1:L_2=1:1. It is to be noted, GC-DM-JAM MOSFET has the highest threshold voltage (*i.e.,* lowest SCEs) and lowest roll-off [21], [22]. Fig. 2.7 (a) shows the variation of drain current (in log scale) against gate voltage for all the compared devices. It is observed that GC-DM-JAM MOSFET has the highest I_{ON}/I_{OFF} ratio and lowest GIDL. GIDL is the leakage current in the off-state of the device. It could be noted that GIDL leakage for DM-JAM is more than GC-JAM MOSFET, although having similar drain current characteristics, due to low HCEs in GC- JAM. Fig 2.7 (b) shows GIDL current against drain voltage, it is observed that GIDL current is lowest for the GC-DM-JAM MOSFET. Fig 2.7 (c) shows gate leakage current (in logarithmic scale) against gate voltage for all the compared devices. Gate leakage is the leakage current at on state of the device. It could be noted that gate leakage is the lowest for GC-DM-JAM MOSFET for all operating regions. Gate leakage current is a strong function of gate field. Therefore, we could observe a sudden increase in gate leakage at high gate field (at V_{GS}>0.6 V) as both regions R_j;*(j=1,2),* are working in the accumulation regime. Fig 2.7 (d) shows the variation of gate current with temperature. It could be inferred that gate leakage for GC-DM-JAM



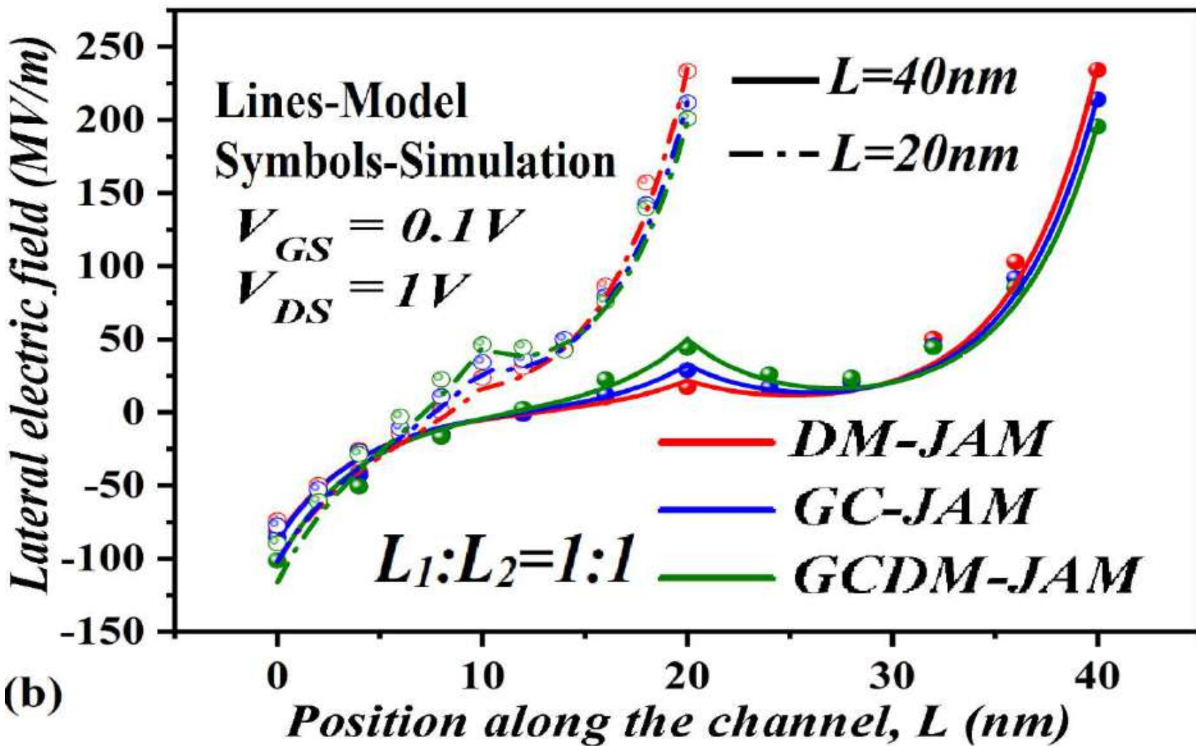


Fig. 2.4: (a). Central channel potential along the channel length at V_{DS}=V_{GS}=0.1V, L_1:L_2=1:1 and at R=5 nm, 7 nm; (b). Lateral electric field along the channel length at V_{DS}=1 V, V_{GS}=0.1V-high field, L_1:L_2=1:1 and R=5 nm.

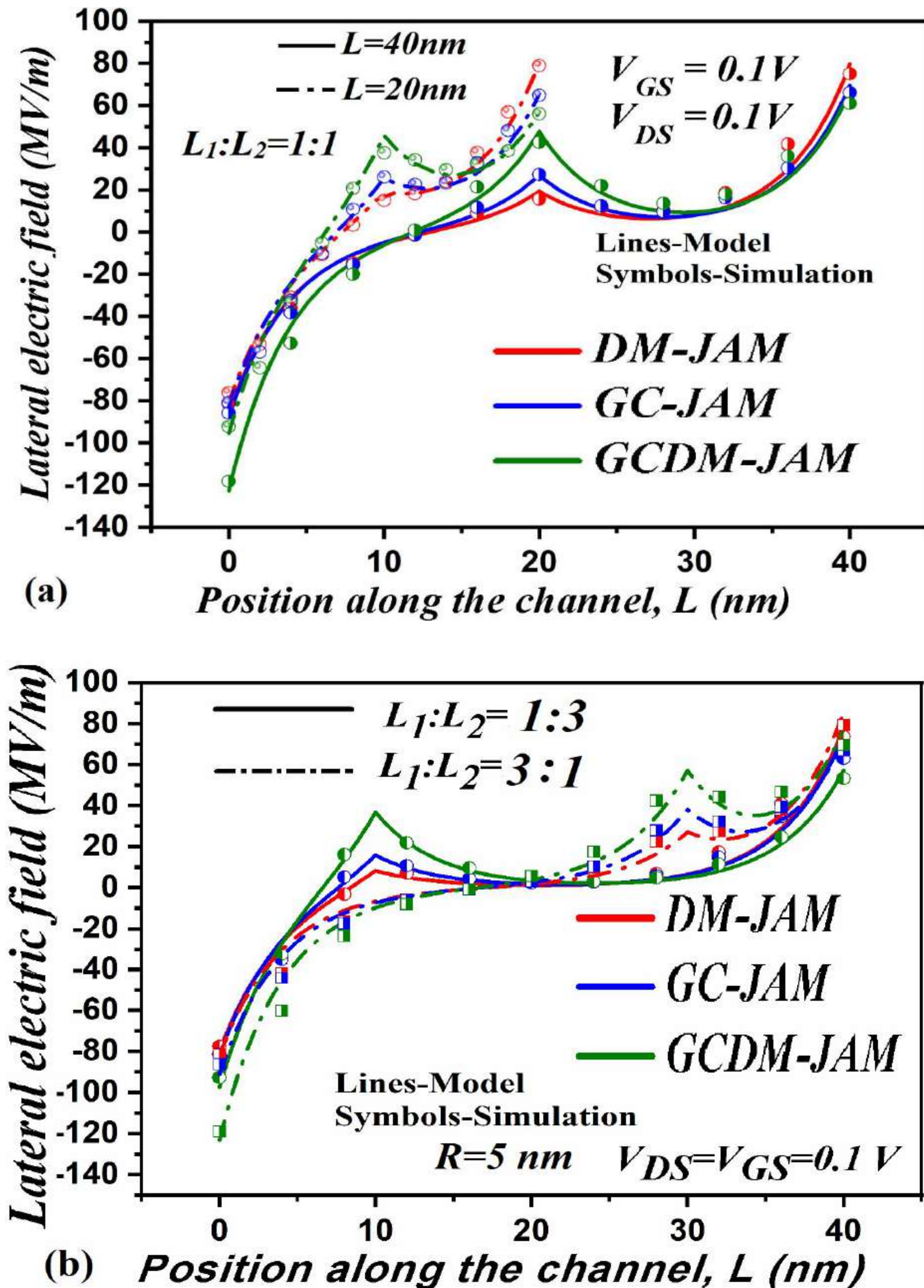
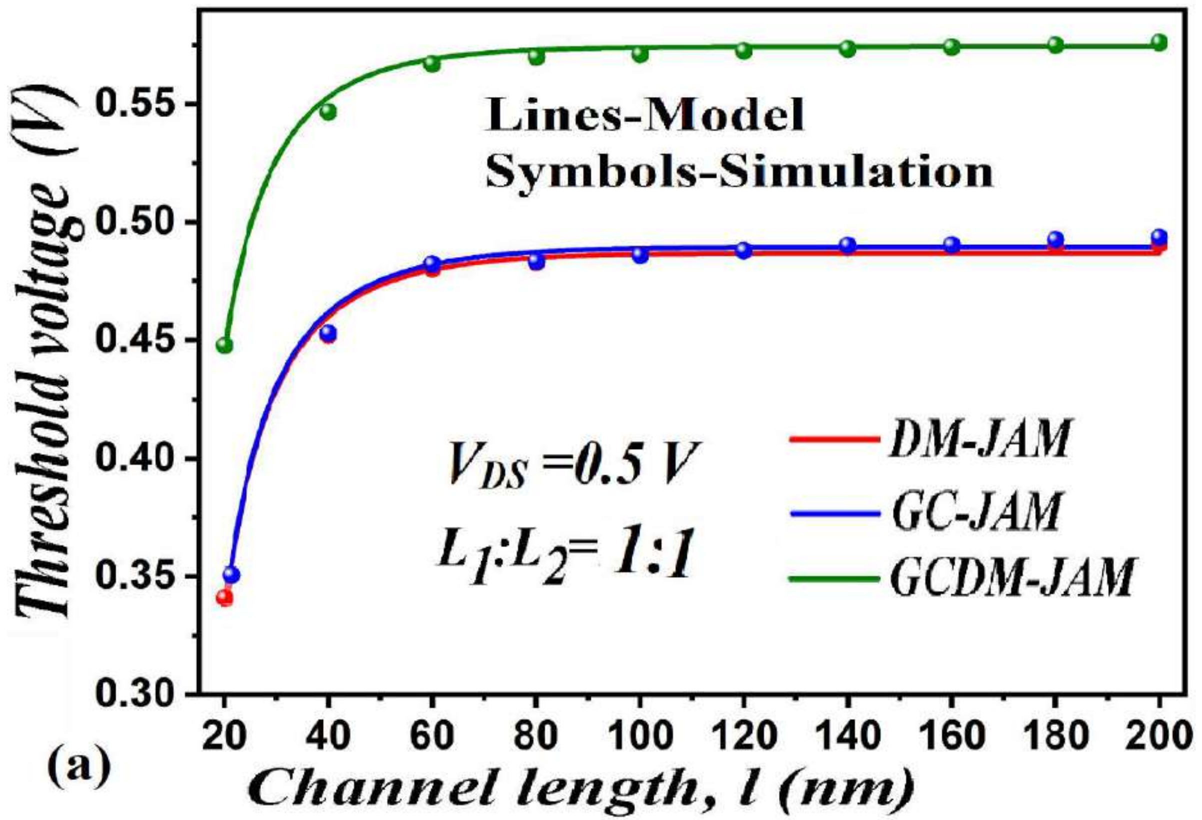


Fig. 2.5: Lateral electric field along the channel at (V_{DS}=V_{GS}=0.1V)-low field at (a). L=40 nm, 20 nm and L_1:L_2=1:1; (b). L=40 nm, L_1:L_2=1:1 and L_1:L_2=3:1.



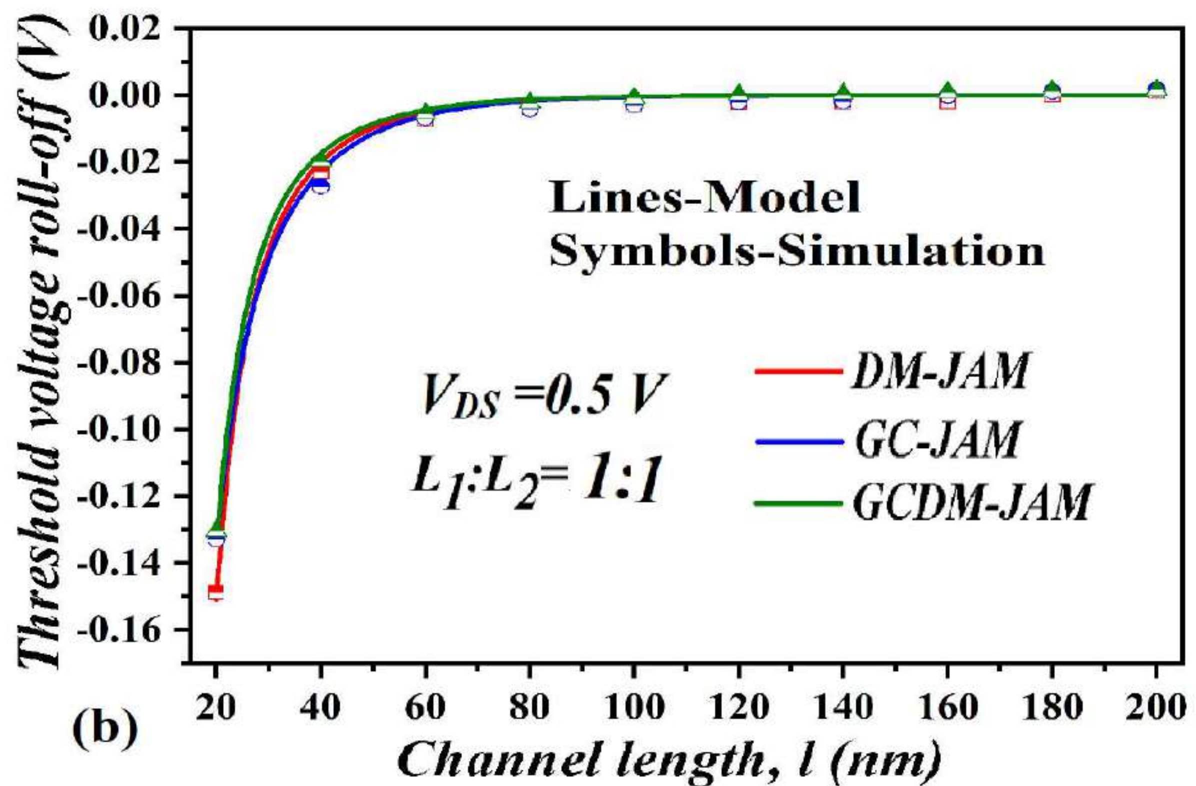
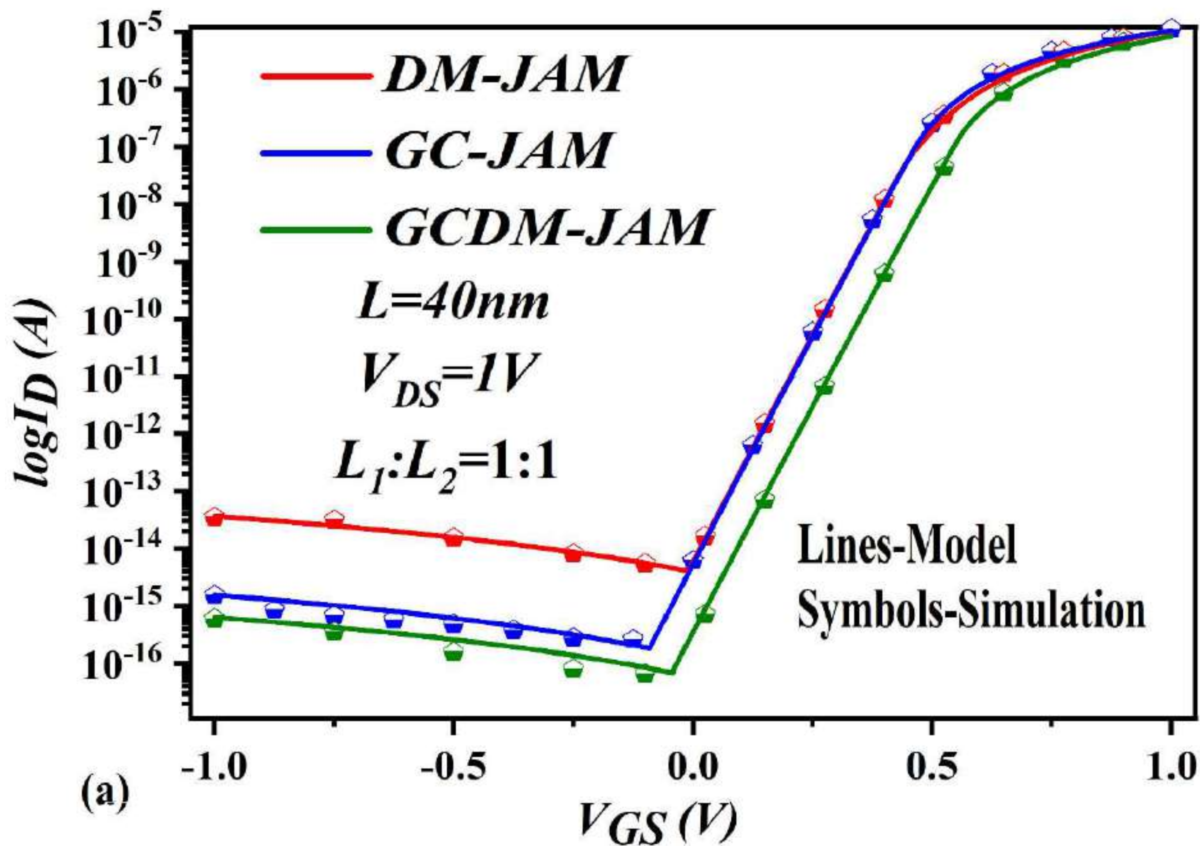
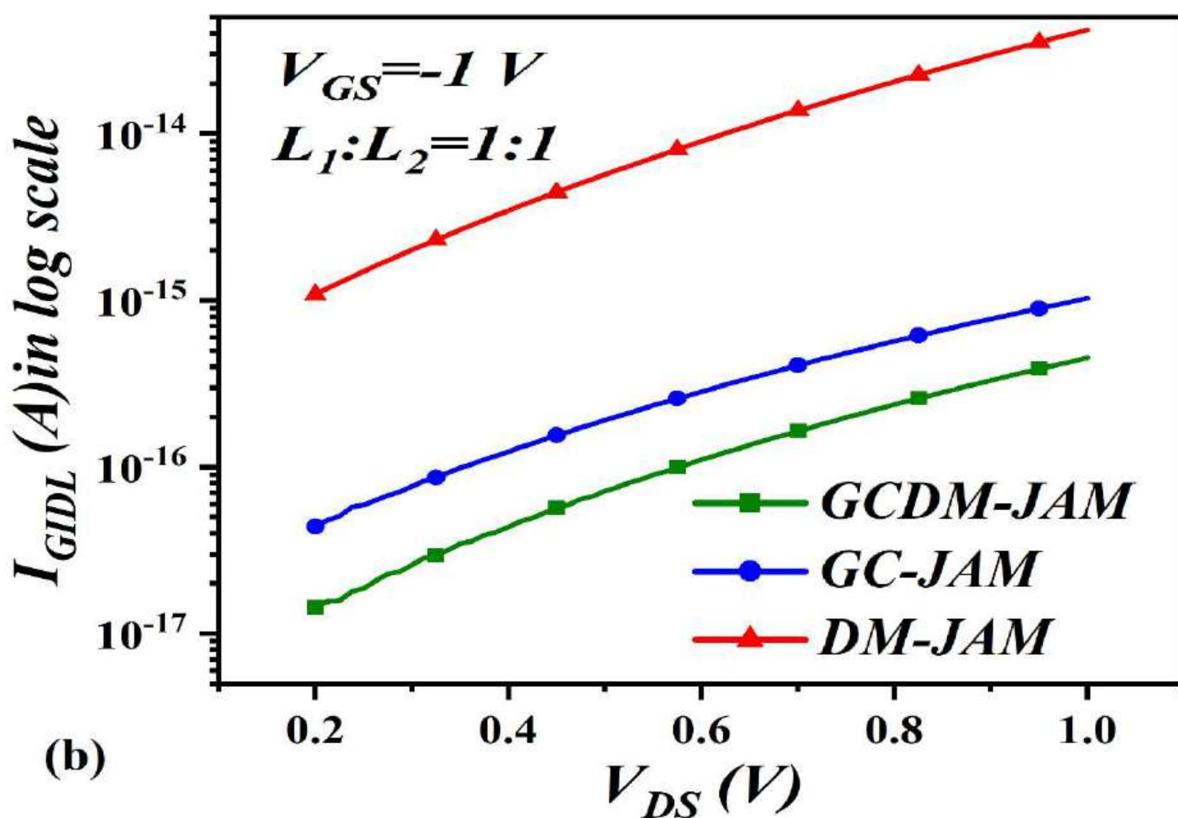
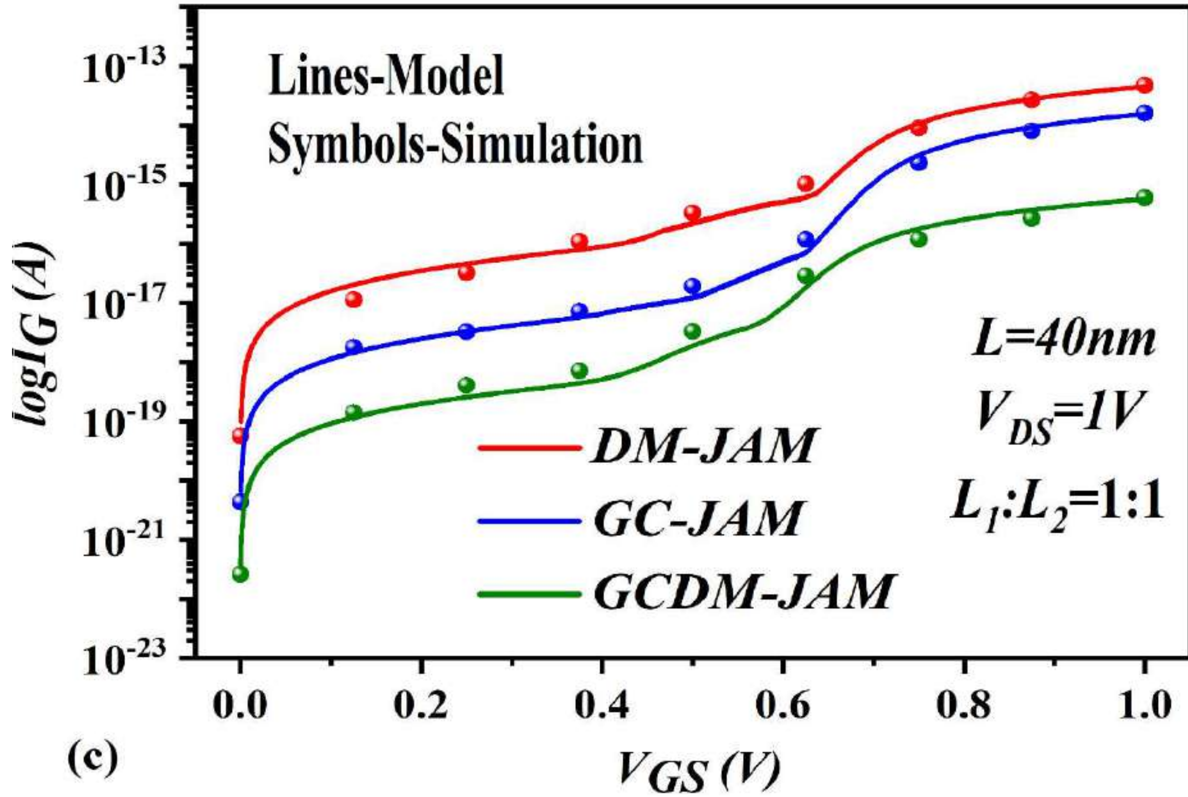


Fig. 2.6: (a) Threshold voltage; (b) roll-off, variations with variation of channel length, at (V_{DS}=0.5V) for L_1:L_2=1:1.


DM-JAM
GC-JAM
GCDM-JAM
L=40nm
V_DS=1V
L_1:L_2=1:1
Lines-Model
Symbols-Simulation
logI_D (A)
V_GS (V)
(a)


V_GS=-1 V
L_1:L_2=1:1
GCDM-JAM
GC-JAM
DM-JAM
I_GIDL (A)in log scale
V_DS (V)
(b)



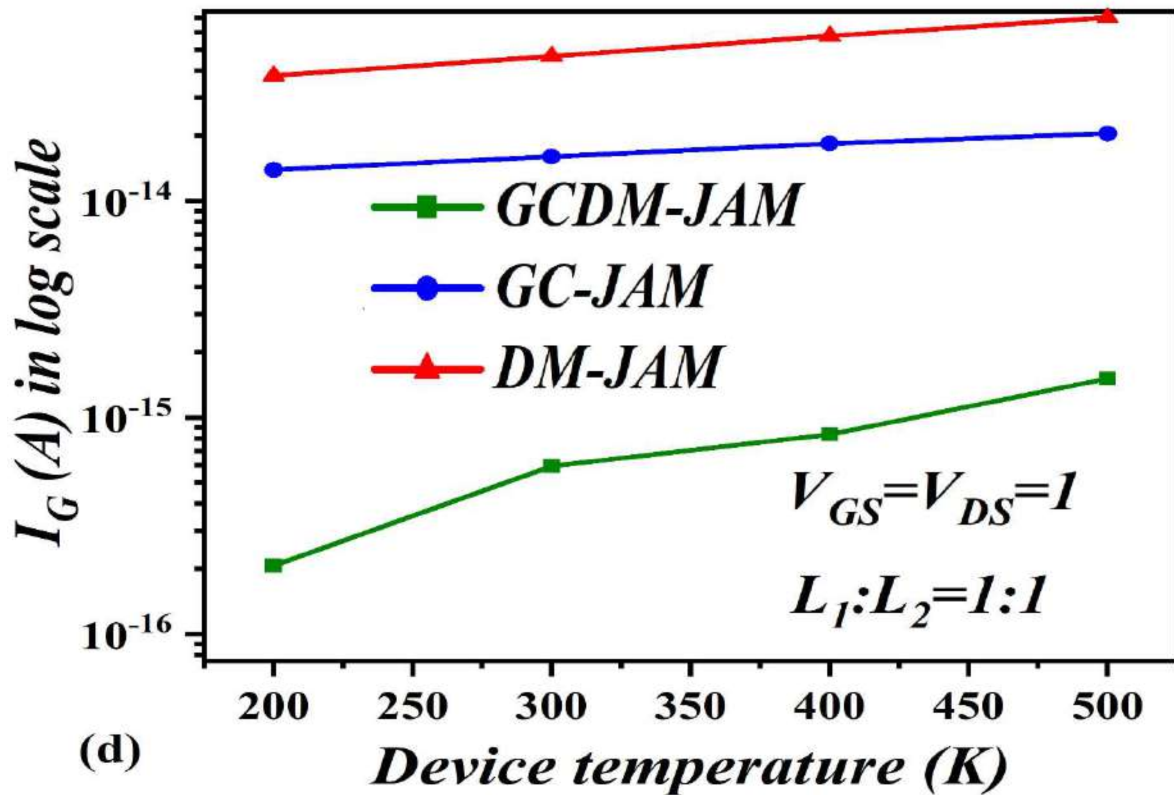


Fig. 2.7: (a) Drain current (in log scale) variations with variation of gate voltage at V_{DS}=1 V; (b) GIDL current variations against drain voltage; (c) gate current variations with gate voltage at V_{DS}=1 V; (d) gate current variation with temperature at V_{DS}=V_{GS}=1 V; with L_1:L_2=1:1.

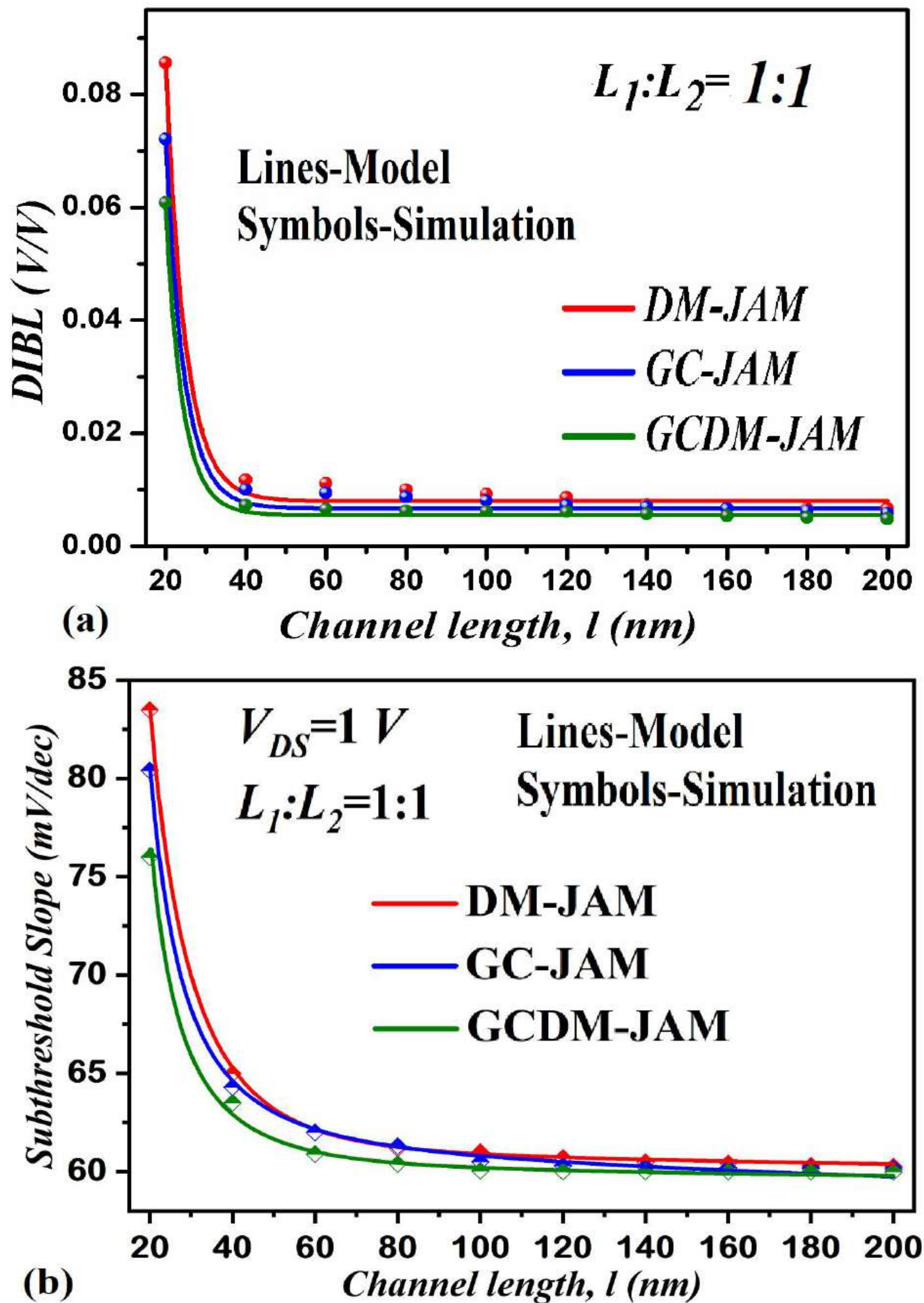


Fig. 2.8: (a) DIBL; (b) Subthreshold slope, with variation in channel length at L_1:L_2=1:1.

MOSFET is least even at a high temperature thus showing its immunity towards increase in temperature. Fig. 2.8 shows (a) DIBL and (b) Subthreshold slope (SS) against different channel lengths (20-200nm) for three different device structures. It is to be observed that both DIBL and SS are least for the GC-DM-JAM MOSFETs. Thus, the proposed device is more immune towards drain voltage variations and has steep switching characteristics.

2.4 Conclusion

A 2-D analytical model of surface potential, lateral electric field, threshold voltage, roll-off, DIBL, the complete drain current (including GIDL), SS and gate leakage current for short-channel GC-DM-JAM, GC-JAM and DM-JAM MOSFET has been presented in this chapter. A comprehensive analysis of the above models has been carried out and compared with each other on the basis of performance metrics. An analysis of device parameters, radius R of the CG-device, channel length, and L_1:L_2 ratio variations have been carried out. It has been observed in the present study that GC-DM-JAM MOSFET gives the highest reliability in terms of SCEs against drain voltage variations, Hot carrier effects (i.e., HCEs), leakage current (GIDL and gate leakage) and against temperature variations. Furthermore, it also increases I_{ON}/I_{OFF} ratio, reduces DIBL, and SS. GC-DM-JAM MOSFET effectively suppresses HCEs and leakage currents thereby increasing its reliability and I_{ON}/I_{OFF} (6.2×10^{10} against 2.15×10^{10} of GC-JAM MOSFET and 8.4×10^{8} of DM-JAM MOSFET). Moreover, at increased radius-R GC-DM-JAM MOSFET gives greater reliability than DM-JAM MOSFETs which is essential from fabrication (higher structure stability) and switching (higher ON-current) point of view. These enhanced electrical features and lower leakage characteristics at both the on and off-state makes the proposed device suitable for analog/digital applications.