Introduction and Organization of the Thesis

1.1 Introduction

One of the most revolutionary inventions in the semiconductor industry was the discovery of bipolar junction transistor (BJT) by William Shockley, John Bardeen, and Walter Brattain in 1947 at the Bell Laboratory. The bulky vacuum tubes were quickly replaced by the BJT to realize complex miniaturized electronic circuits. However, the realization of electronic circuits with hundreds of transistors, resistors, capacitors and diodes by hand soldering was an extremely difficult task. This was overcome by the conceptualization of the Integrated Circuit (IC) technology by Jack Kilby (along with Robert Noyce) in 1958 for which Kilby was awarded the Nobel Prize in Physics on December 10, 2000. The BJT was the key active circuit element in the ICs for building various complex multifunctional electronic circuits in a single chip. A significant boost up in the IC technology was attained by the experimental demonstration of the metal-oxide-semiconductor field-effect transistor (MOSFET) by Kahng and Atalla in 1960 (Kahng and Atalla, 1960). The easier fabrication, lower power dissipation, higher drive current, higher speed, better scalability and inherently higher input impedance of the MOSFET made it soon a more preferred transistor over the BJT for the IC applications (Streetman and Banerjee, 2006)(Sviličić and Kraš, 2006). A p-MOSFET and an n-MOSFET were soon combined in the same wafer to achieve the complimentary-metal-oxide-semiconductor (CMOS) structure. The CMOS based IC technology was then extensively explored to build SRAMs, microprocessors, microcontrollers and various complex digital logic circuits.

The everlasting aspiration of developing complex multifunctional ICs such as microprocessors and microcontrollers led to the integration of billions of CMOS circuits and

components on a single chip thereby increasing their packing density. The relentless increase in the number of transistors per unit area in the ICs forced to reduce the dimensions of MOS transistors aggressively through a systematic scaling process. By observing the initial trend of increasing the number of electronic components in an IC, Gordon E. Moore, the co-founder of the Fairchild Semiconductor and Intel, predicted in 1965 that the total number of components in an IC would be doubled every year over at least one decade (G. E. Moore, 1965). This is commonly known as the Moore's law. Later in 1975, he changed his prediction to doubling of the number of components in the ICs every two years for the next decade (G. E. Moore, 1975). The Moore's law has been the guiding principle behind the colossal growth of the IC industry over more than last six decades. The number of transistors on a single IC has increased from a few to billions in the span of nearly six decades. It can be easily realized from the growth of electronic industry over the last few decades as shown in Fig 1.1 (Internet resource, IR1). With the increase in the number of transistors per unit area of the ICs, the channel length has been decreased drastically over the years from micrometer (μm) to nanometer (nm) scale. Figure 1.2 (Internet resource, IR2) shows the variation in the number of MOS transistors and gate lengths of the MOS transistors during last few decades. It is observed that the initial gate-length of 10 μm in 1970 is predicted to be reduced 5 nm in 2030. This has been possible by the systematic scaling of device parameters which is briefly discussed in the following section.

1.2 MOS Transistor Scaling

The CMOS scaling is basically the process of miniaturization of MOS transistors without compromising their performance parameters. Thus, all the device parameters like the gate-length, oxide thickness, channel thickness, threshold voltage, applied bias voltages, doping concentration etc. are required to be scaled in such a way that the performance degradation with the reduction in the gate-length becomes the minimum. In this direction, two main types of scaling rules were proposed: constant field scaling (Dennard *et al.*, 1974) and constant

voltage scaling (Taur and Ning, 1998). The basic objective of the constant field scaling rules proposed by Dennard *et al.* (Dennard *et al.*, 1974) was to maintain the same electric field

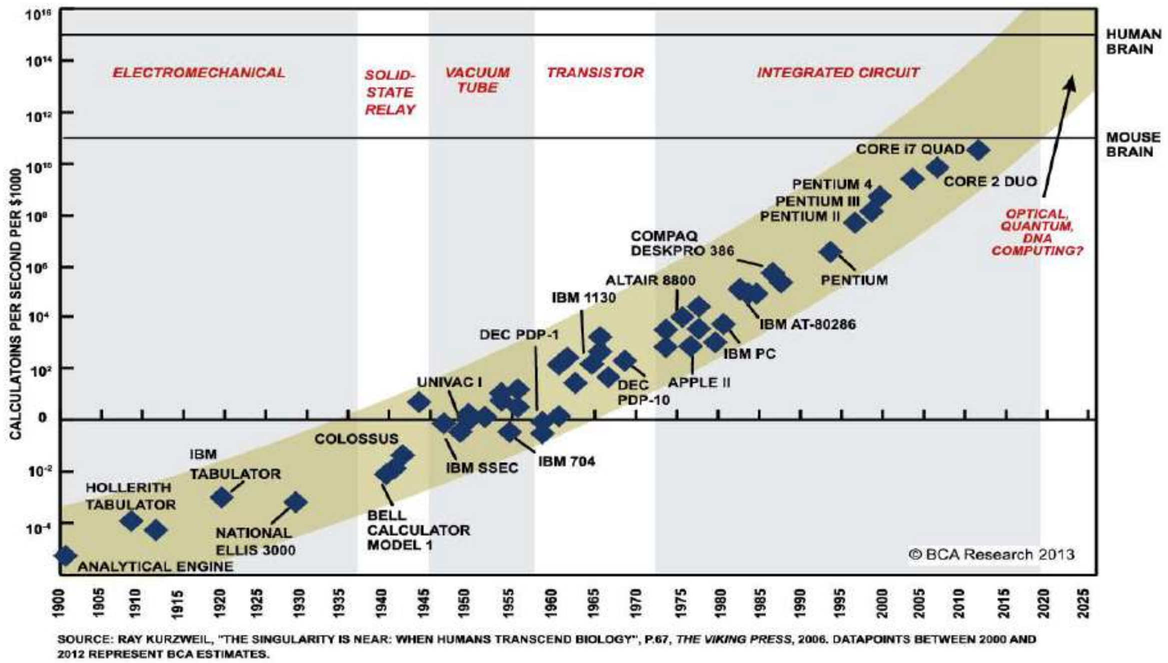

Fig. 1.1: Evolution of the electronic industry as the result of *Moore's law* (Internet resource, IR1).

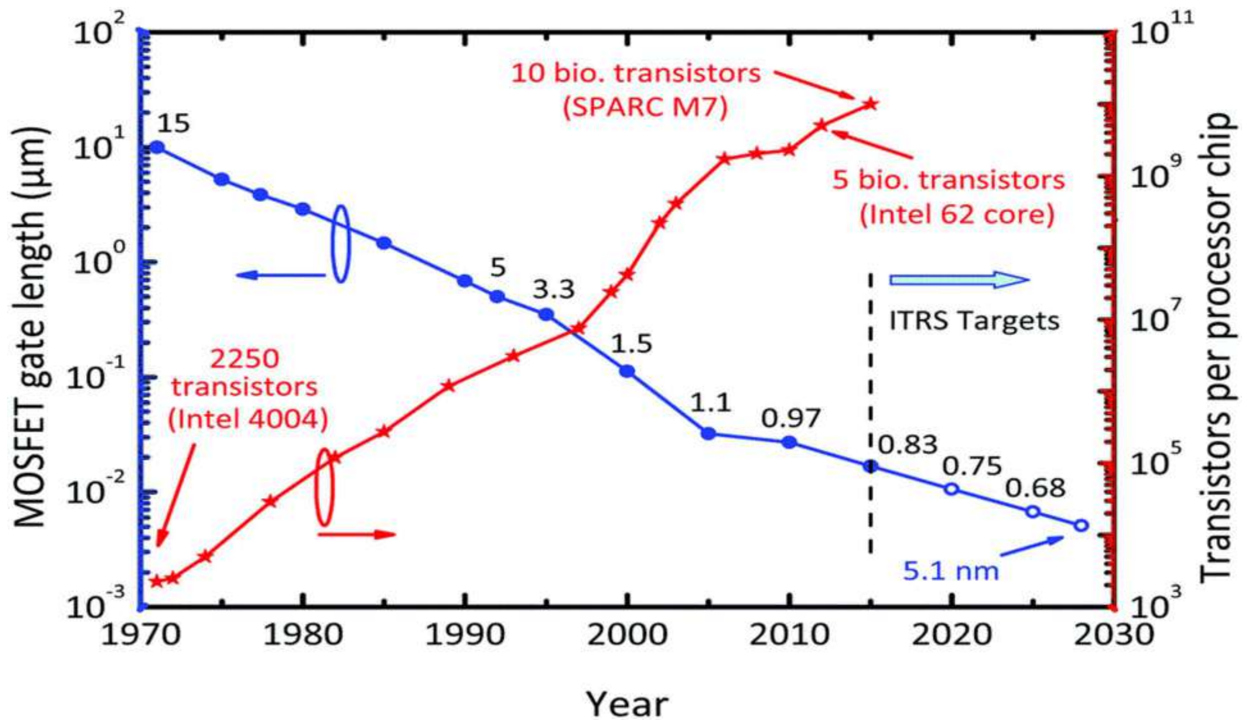

Fig. 1.2: The ITRS roadmap of transistor development (Internet resource, IR2)

everywhere in the miniaturized version of the transistor as that of the unscaled device. According to this scaling rules, if the gate length is scaled down by α factor, then all the dimensional parameters (e.g. oxide thickness, the channel thickness and source (drain)/channel junction depth) and voltage parameters (e.g. gate voltage, drain voltage and threshold voltage) are to be also scaled down by the α factor. The major disadvantage of this rule is that scaling of voltages by α reduces the noise margin of the device and necessitates the need for different supply voltages for differently scaled MOS devices. On the other hand, Taur and Ning proposed the constant voltage scaling in which all the device dimensions and the channel doping concentration were suggested to reduce by α in the scaled device while maintaining the same operating voltages of the unscaled transistors. The constant voltage scaling led to the continuous increase in the electric fields in the channel and other sections of the device in successive scaling generations. The high channel electric fields led to several undesired phenomena such as the velocity saturation of carriers in the channel (Zhou and Long 1998), hot carrier effects (Long *et al.,* 1999; Zhou, 2000), avalanche breakdown (Taur and Ning, 1998), etc.

To overcome the constraints and limitations of the aforementioned two main scaling rules, a quasi-voltage scaling theory was proposed by Arora in 1993 (Arora, 1993). In this method, the bias voltages are scaled by a factor smaller than the scaling factor α used to scale the device dimensions (Arora, 1993). Figure 1.3 shows that the bias voltage (V_{DD}) and threshold voltage V_{th} are reduced by nearly one fifth and half of their corresponding original values during the technology scaling of CMOS from 1.4 µm to 65 nm node (Packan, 2007). Further, the figure also shows the reduction in gate overdrive voltage with different technology generation nodes. This shows that the switching characteristics of the MOSFETs are degraded due to the worsening of I_{ON}/I_{OFF} ratio and gate delay ($C_{GG}V_{DD}/I_{ON}$) ratios, where C_{GG}, I_{ON} and I_{OFF} are gate capacitance, on-current and off-current of the MOS device, respectively. Since the bias

voltage cannot be reduced below a certain limit for practicalities of circuit operations, the drain voltage is fixed approximately at 1 V for 90 nm technology node and beyond (Nilsson, 2006). Thus, while the miniaturization of MOS transistors by scaling is essentially required for accommodating billions of transistors in modern multifunctional complex ICs, the technology scaling results in severe performance degradations of the MOS transistors. The reduction in threshold voltage increases the subthreshold leakage current which, in turn, increases the power dissipation of the CMOS ICs.

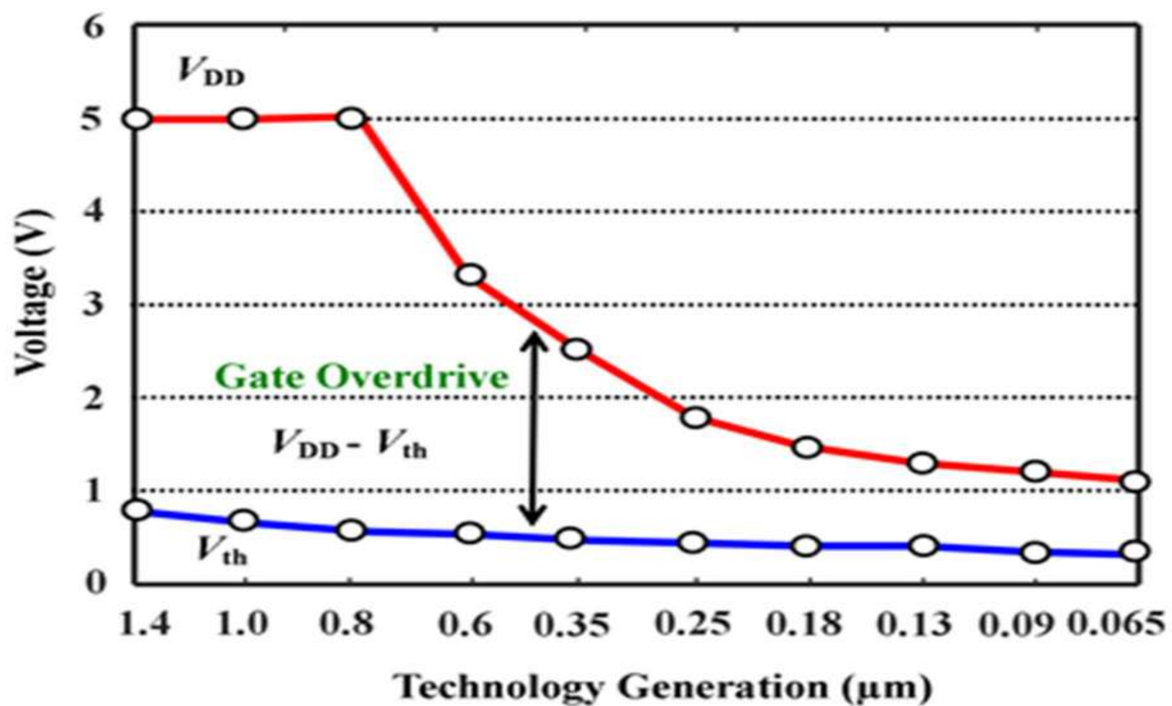

Fig. 1.3: Variation of supply voltage and threshold voltage against technology generation (Packan, 2007).

1.2.1 Power Management in CMOS ICs

The active power (P_{active}) and static power (P_{sub}) losses in the ICs can be described by the following equations (Nilsson, 2006):

$$P_{active} = f_{clk} C_{load} V_{DD}^{2} \quad (1.1)$$

$$P_{sub} = V_{DD} I_{OFF} \tag{1.2}$$

where f_{clk} and C_{load} in eq.(1.1) are the frequency of operation and load capacitance respectively.

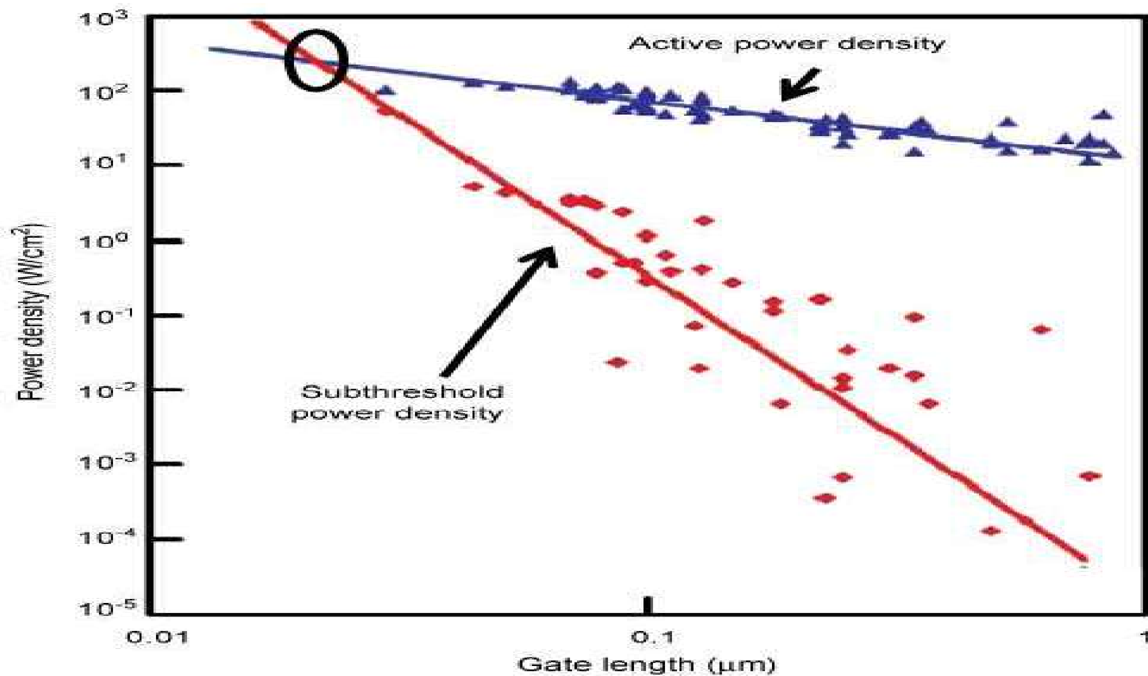

Fig. 1.4: Variation of power density against gate length scaling of MOS device (Meyerson, 2004).

The reduction in the gate-length through technology scaling reduces the transit time delay and hence the frequency of operation of the device. Thus, the active power is increased with technology scaling when drain voltage (V_{DD}) is fixed at nearly 1 V. On the other hand, subthreshold power dissipation is also increased with scaling due to the increase in the subthreshold leakage current in the MOS transistors. Thus both the active and subthreshold power losses are increased with the reduction in the gate-length due to scaling as shown in fig 1.4. The increase in both the OFF-state leakage current and subthreshold swing (SS) with the decrease in threshold voltage due to scaling are demonstrated by the drain current (I_D) versus gate-to-source voltage (V_{GS}) characteristics of three different MOSFET in fig 1.5. Thus, it is

necessary to minimize the threshold voltage degradation in the MOS transistor scaling to minimize the static or subthreshold power loss in the ICs. This is achieved by increasing the channel doping concentration. However, the increased channel doping compensates the reduction in the threshold voltage at the cost of reduced speed of operation of the MOSFETs due to the reduction in the channel carrier mobility by impurity scattering. This clearly defeats the basic purpose of the technology scaling of the MOS transistors (Hu, 2010).

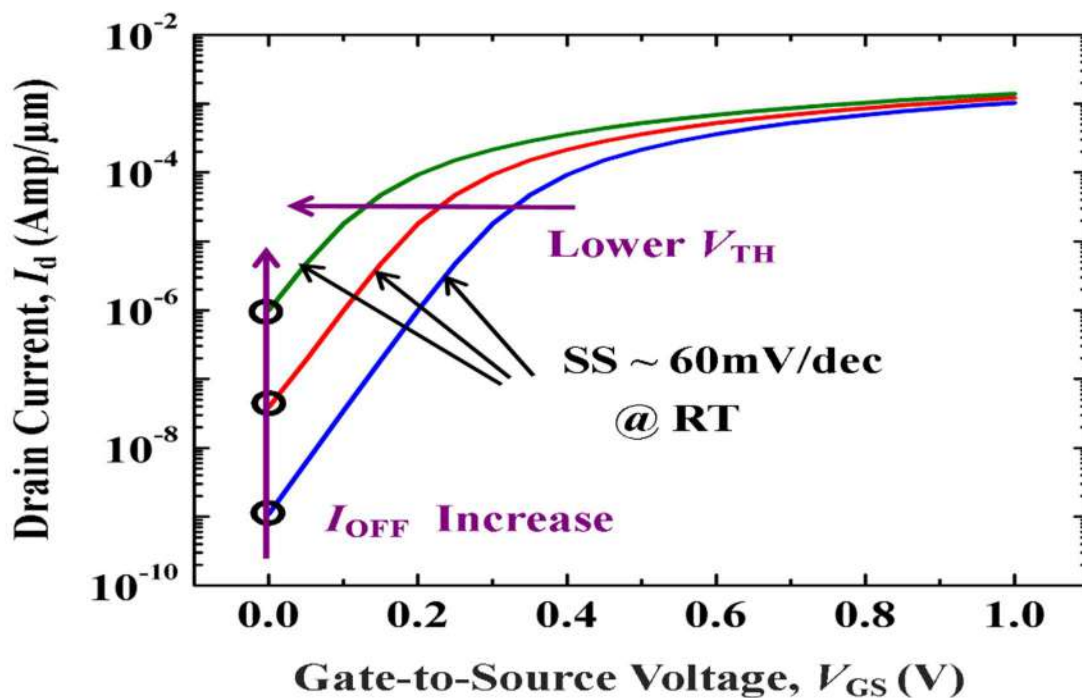

Fig. 1.5: Variation of drain current against gate-to-source voltage of MOS device (Internet resource, IR3).

1.2.2 Short Channel Effects (SCEs) in Classical MOSFETs

An MOSFET is said to be a long-channel device if the channel electric field below the gate is one-dimensional (1-D) and the channel electrostatics are nearly independent of the electric fields in the source/channel and drain/channel depletion regions. In long-channel MOSFETs, the threshold voltage of the device is independent of the channel length and the channel electrostatics are purely controlled by only gate voltage of the MOSFET. However, in the short-

channel MOSFETs, the channel length of the MOSFET is so small that the depletion regions below the gate, at the source/channel junction and at the drain-channel junction are merged together. Thus, the electrostatics of the channel region of the short-channel MOSFETs are not only controlled by the gate voltage but also by the source and drain voltages. Unlike the long-channel MOSFETs, the channel electric field becomes a two-dimensional (2-D) function and the threshold voltage becomes a strong function of the drain voltage and channel length in short-channel MOS transistors. As a consequence, the threshold voltage is reduced by substantial sharing of the channel depletion charges by the depletion regions of the source/channel and drain/channel junctions (Sze and Ng, 2007) of the MOSFET. The reduction in the gate-length in the nanoscale MOSFETs due to scaling thus results in several adverse effects on the performance parameters of the MOSFETs such as the reduction in the threshold voltage, increase in the OFF state leakage current, increase in the subthreshold swing, channel carrier velocity saturation, increase in the power dissipation, hot carrier effects, drain-induced barrier lowering (DIBL), reduction in effective channel length (i.e. channel length modulation), increase in gate-induced leakage current (GIDL), increase in gate-oxide tunneling leakage current, direct source to drain quantum tunneling (ballistic transport), surface scattering, and impact ionization in the short-channel MOSFETs. These effects are commonly known as the short-channel effects (SCEs) in the MOSFET scaling theory. Some of the major SCEs are briefly discussed below:

Drain induced barrier lowering (DIBL): The DIBL is one of the most detrimental SCEs in the subthreshold regime of operation of the MOSFETs. As the drain voltage (V_{DS}) is increased, the drain/channel depletion region is extended toward the source in the channel thereby decreasing the charge sharing by the depletion region under the gate. This effectively reduces the potential barrier at the source/channel junction, which, in turn, reduces the threshold voltage (V_{th}) of the

MOSFETs. The DIBL is given by the difference between threshold voltages at the low and high V_{DS} as shown in fig. 1.6 (Sze and Ng, 2007).

Channel length modulation: When $V_{DS} \geq V_{GS}-V_{th}$, the drain current ($I_D$) becomes relatively constant and the device is said to be operated in the saturation regime. Inversion charge density $Q_I(x)$ is proportional to $V_{GS}-V(x)-V_{th}$ where $V(x)$ is the channel potential. This, when $V(x)$ approaches to $V_{GS}-V_{th}$, the inversion charge $Q_I(x)$ approaches to 0. Therefore, for $V_{DS} > V_{GS}-V_{th}$, the formation of the channel inversion region is restricted to the region $0 \leq x \leq L' <$ channel length (L) below the gate and the MOSFET is said to be in the *pinch-off* condition. If V_{DS} is increased further, the effective channel length L' is reduced. This dependence of L' on the drain voltage is known as the channel length modulation. This effect decreases the channel resistance and increases the drain current in the saturation region. In other words, the slope of the I_D/V_{DS} curve becomes slightly positive and deviates from the ideally zero value in the saturation regime of operation of the device (Kang *et al*., 2002)

Subthreshold slope (SS) degradation: The subthreshold swing (SS) is defined as the gate-to-source voltage needed to change the drain current by one order of magnitude or one decade. Mathematically, SS is defined as

$$SS = \frac{\partial V_{GS}}{\partial(log\ \ _d)} = \underbrace{\left(1 + \frac{C_{Dep}}{C_{ox}}\right)}_{m} \underbrace{(V_T\, ln\, 1\, 0)}_{n} \qquad (1.3)$$

where C_{Dep} and C_{ox} are the depletion and oxide capacitances, respectively. The value of "n" is 60 mV/dec and "m" is always greater than 1. Therefore, the thermodynamic limit of SS for MOSFET is 60 mV/dec, which is called the Boltzmann limit. The SS value is increased with the decrease in channel length (Sze and Ng, 2007).

Gate induced drain leakage (GIDL): When a high drain bias voltage but a low or a negative gate bias voltage is applied to the MOSFETs, the electric field in between the gate-end of the

channel and drain/channel junction is normally very high. Under this condition, there is a high possibility of tunneling of electrons from the valence band of the channel to empty states in the conduction band of the drain region as demonstrated in fig. 1.7(Bouhdada *et al.,*1997; Sun *et al.*, 2020). This band-to-band tunneling (BTBT) thus increases the drain leakage current under the OFF state operation of the MOSFETs which is highly undesirable in the MOSFET operation.

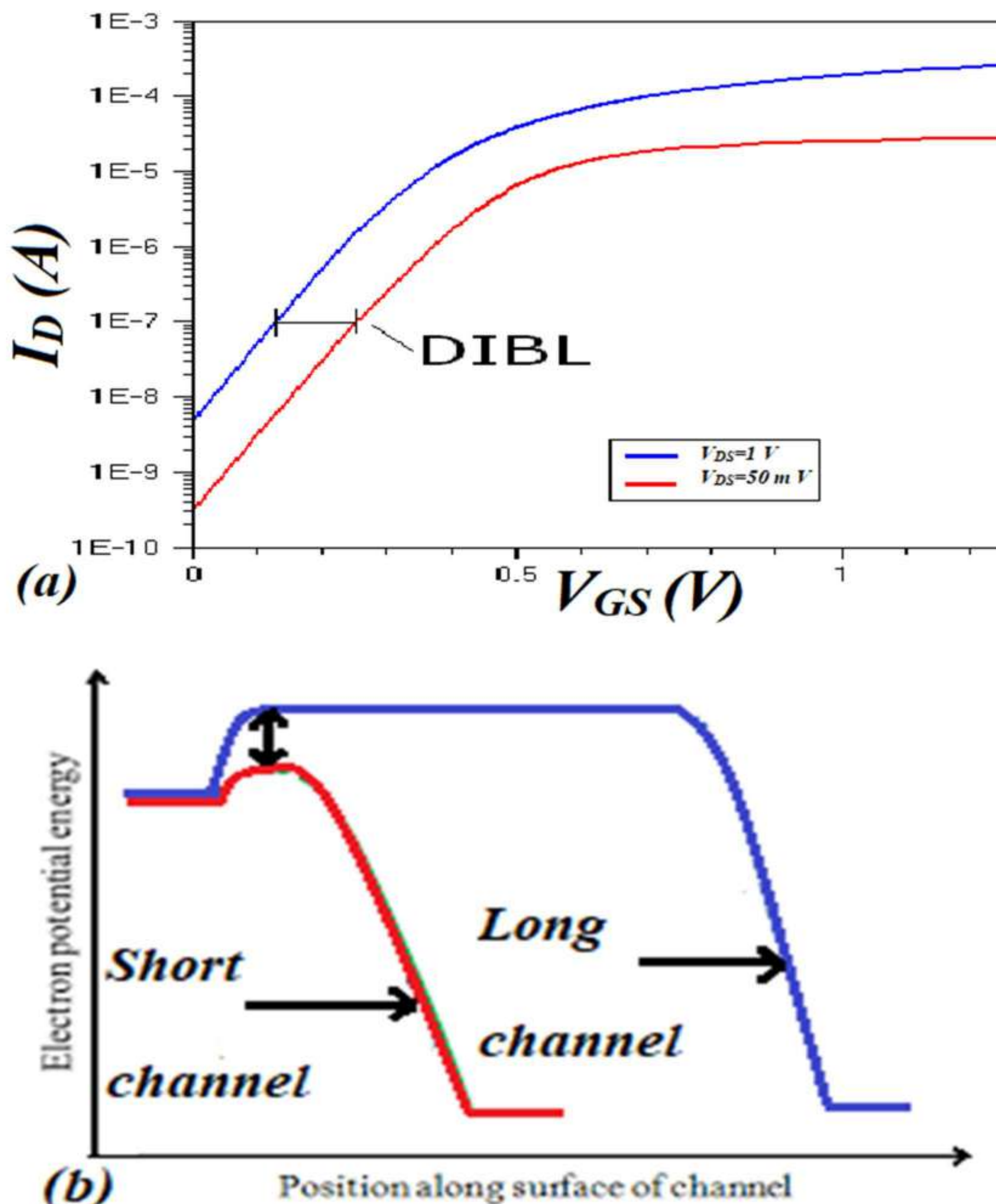

Fig. 1.6: (a) Variation of DIBL with the drain to source voltage (1 *V* and 50 *mV*) (b) energy band diagram representation of DIBL.

Direct gate oxide leakage: Since gate oxide thickness is also reduced with the reduction in the gate length, the oxide electric is increased with the technology scaling generations. This enhances the probability of tunneling of the carriers from the channel into the gate directly through the thin gate oxide layer and contributes to the gate leakage current (Yeo, King and Hu, 2003) as shown in fig. 1.8. This increases the power loss of the MOS transistors.

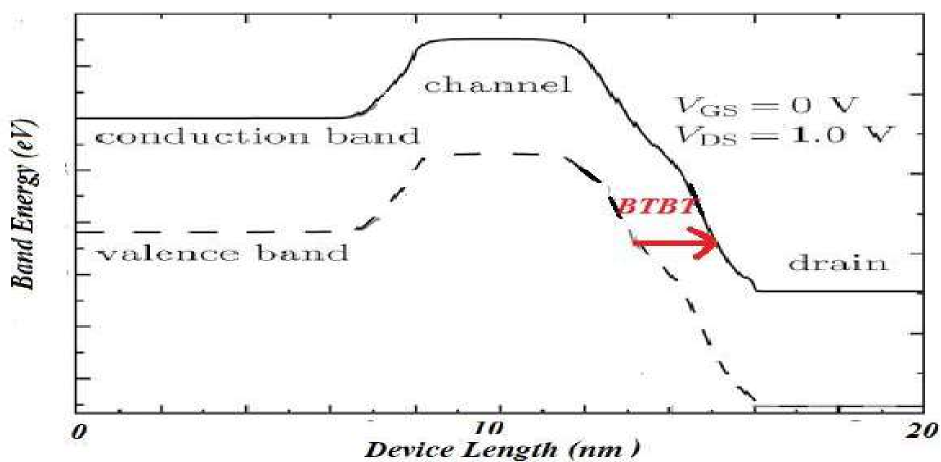

Fig. 1.7: The process of band to band tunneling (BTBT) in MOSFET giving rise GIDL.

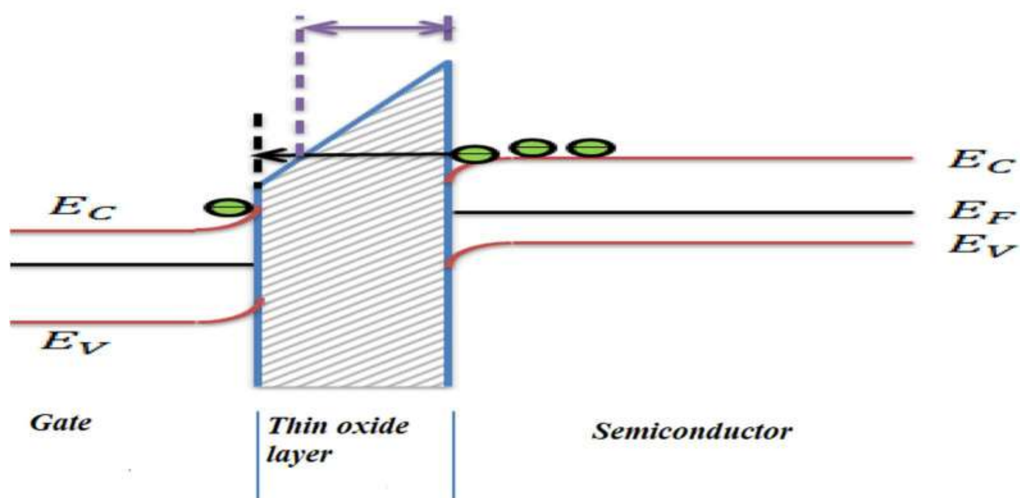

Fig. 1.8: The mechanism of direct gate tunneling as gate oxide leakage.

Direct source to drain quantum tunneling (ballistic transport): The lateral electric field in the channel is increased with the decrease of the channel length. This high electric field in the channel enhances the probability of carrier tunneling directly from the source to drain through the extremely narrow channel existing between them. This ballistic transport phenomenon can't be ignored for modeling the device characteristics of the MOS transistors with channel lengths below 30-40 nm (Wang and Lundstrom, 2002). The ballistic transport at about 10 nm channel length contributes to a leakage current in addition to the thermionic current (Eminente *et al.*, 2005). The mechanism of ballistic transport is demonstrated in fig. 1.9.

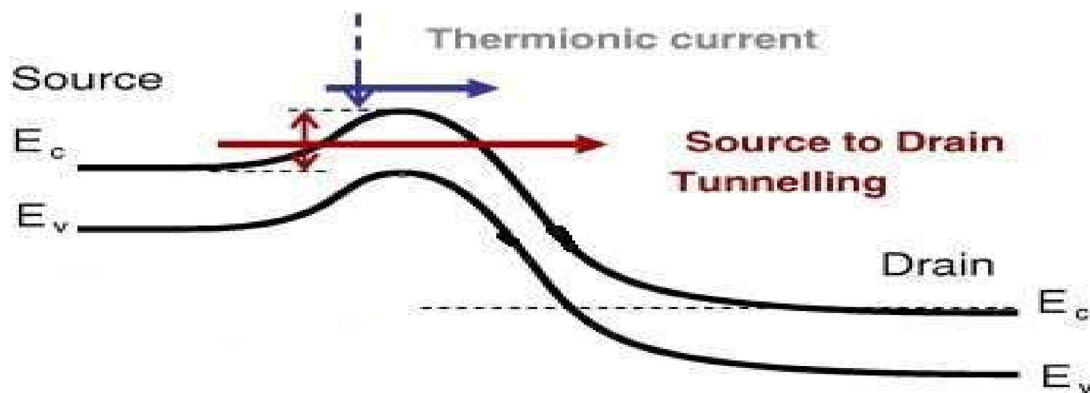

Fig. 1.9: The mechanism of ballistic transport in MOSFET.

Surface scattering: The increase in the oxide electric field due to the decrease in the gate oxide also increases the vertical electric field in the channel drastically at the oxide/channel interface. This high vertical electric field reduces the mobility of the channel carriers due to enhanced surface scattering. The surface scattering thus degrades the transconductance of the device (Schroeder, 1994).

Velocity saturation: The drift velocity (v_d) of the channel carriers is proportional to the channel electric field, i.e. $v_d = \mu E$, where E and μ are the channel electric field and mobility of channel carriers. However, when the electric field exceed a critical value, the velocity reaches to a saturation value of ~10^7 cm/s for silicon. For short-channel MOSFETs, the inherently high

electric field in the channel may make the carriers' velocity saturated, which, in turn, provides only the saturation drain current without any linear region existing in I_D vs. V_{DS} characteristics. Thus the devices may not be suitable for linear circuit applications. This phenomenon is called the velocity saturation in short-channel MOSFETs (Takeuchi and Fukuma, 1994).

Hot carrier effects (HCEs): For low V_{GS} and high V_{DS}, there exists a very high electric field at the drain side of the MOSFET. This high lateral field may accelerate the carriers near the channel-drain junction. As a result, some of the carriers may gain sufficient kinetic energy and may enter into the gate oxide dielectric region or may damage the channel/oxide interface. This phenomenon may modify oxide interface charges and disturb the normal electrical behavior of the device (Arora, 1993). At higher fields, the hot carriers may damage the oxide interface and affect the functionality of the device as shown in fig. 1.10.

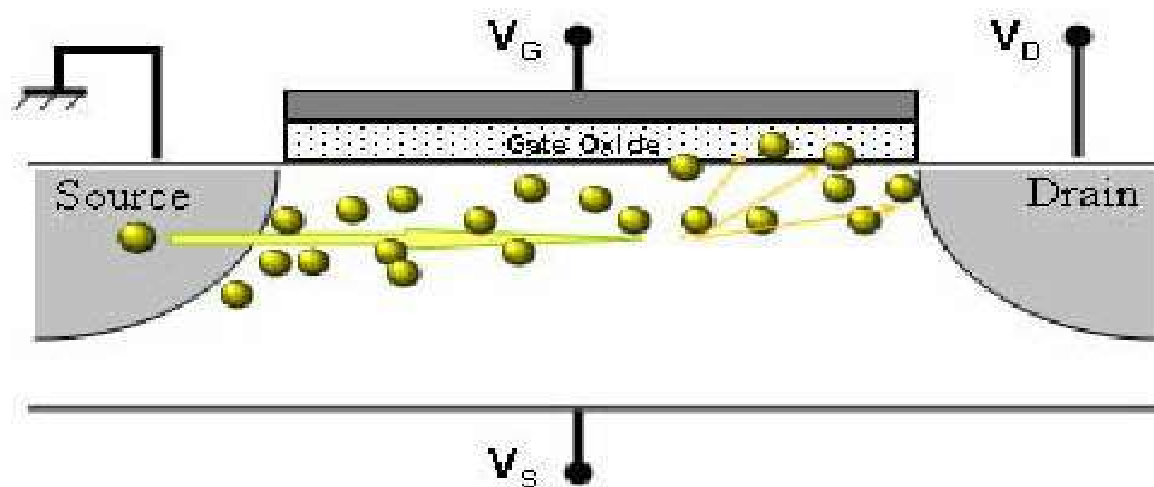

Fig. 1.10: Generation of hot carriers in bulk MOSFET device (Internet resource., IR3).

Impact ionization: The high velocity of the electrons under a very high electric field in the channel of a short-channel MOSFET may generate electron-hole pairs in the depletion region of the channel/drain junction by the process of impact ionization. The generated carriers may move toward the gate, drain and substrate to produce gate leakage current, GIDL and substrate leakage current which are undesirable for the device (Kamata, Tanabashi and Kobayashi,

1976). The electrons travel towards the drain and leftover holes are accumulated in the bulk substrate. This forms the p-type base of an n-p-n parasitic BJT thereby contributing to the undesired substrate leakage current in the MOSFETs (Chaudhry *et al.*, 2004).

1.3 Non-Classical MOSFETs for Sustaining Scaling

The scaling of the classical MOSFETs or conventional bulk MOSFETs has reached to its bottleneck due to excessive SCEs as discussed above in sub-100 nm gate-length devices. The major problem with the bulk MOSFET structure is associated with the use of p-n junctions namely the source/channel and drain/channel junctions. As per the scaling rules, the width of the depletion regions at these two junctions are also required to be reduced with the reduction in the gate-length of the classical MOSFETs. This requires to maintain a steep doping gradient at these junctions which is very difficult to fabricate in a very short channel length MOSFETs. Further, the typical npn or pnp BJT structure of the classical MOSFETs results in severe leakage currents in the device as discussed in the previous section. Thus, the scalability of the MOS transistors can be improved if a non-classical MOS structure is achieved without having any junctions. In this direction, J. P Collinge and his group at the Tyndall National Institute developed a tri-gate MOS structure in 2010 without using any p-n junctions and named it junctionless (JL) MOSFET (J. P. Colinge, Lee, Afzalian, *et al.*, 2010). The original TEM image of the fabricated JL MOSFET is shown in fig. 1.11. The schematic structure of the basic JL MOSFET structure proposed by Colinge et al. (Colinge *et al.*, 2011a) is shown in fig. 1.12. The device uses same type of doping under the source, channel and drain electrodes. Thus, the channel of the JL MOSFET basically acts a resistor which can be varied by the gate voltage. The gate electrode material and the channel thickness are selected such a way that the channel is fully depleted by the work function difference of the gate-metal and channel material under equilibrium condition. Clearly, when the drain voltage is applied, the channel offers a very high resistance and hence a very low drain current for a zero gate voltage. This is called the OFF

state condition of the device. A suitable gate voltage is applied to reduce the depletion region and hence to increase the conductivity of the channel. When the gate-depletion region is the minimum or zero, then the device offers the maximum drain current and the device is said to be in the ON state. The JL MOSFET possesses lower off-current, DIBL and subthreshold degradation due to their high threshold voltage (J. P. Colinge, Lee, Ferain, *et al.*, 2010). Further, the junctionless MOSFET conducts through bulk and therefore is much less susceptible to surface scattering (Colinge *et al.*, 2011a). Our present thesis deals with the modeling and simulation of some engineered JL MOSFET structures. The following section is devoted to introduce the basic working principle of the JL MOSFET.

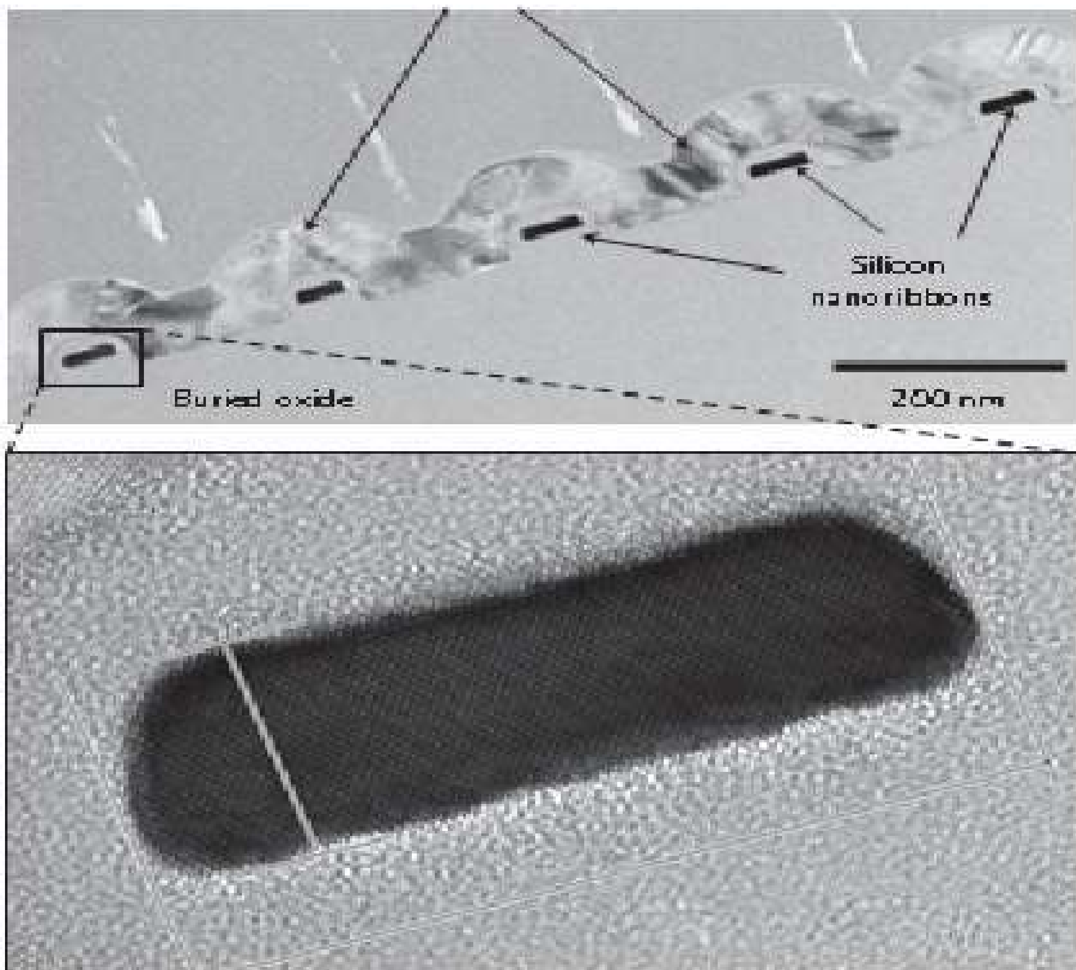

Fig. 1.11: TEM image of five gated nanoribbon and magnified image of a single nanoribbon, (Colinge *et al.*, 2011a)

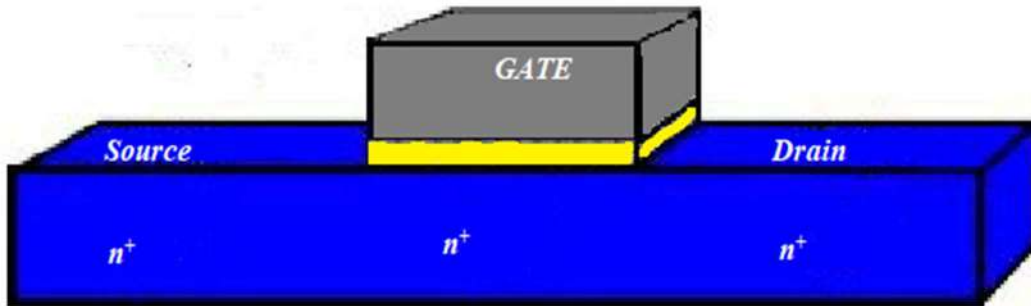

Fig. 1.12: Schematic structure of the basic bulk JL MOSFET structure

1.3.1 Working of the Junctionless MOSFET

The schematic structure considered in fig. 1.12 shows that the conventional JL MOSFET device can be viewed as a gated semiconductor bar with a high doping concentration (~ 10^{19} /cm^3) under all the source, channel and drain electrodes. Unlike the inversion mode of operation in the bulk MOSFET, the JL MOSFET works either in the accumulation or partial depletion mode. The working principle of the junctionless MOSFET is demonstrated in fig. 1.12. Under the OFF-state operation (i.e. $V_{GS}<V_{th}$), channel thickness of the JL MOSFET is considered to be small enough to get completely depleted of carriers by the work function difference between gate material and the channel material. Since there is no mobile carriers in the channel under the OFF state, negligible drain current is observed. However, when the gate voltage becomes greater than the threshold voltage (i.e., $V_{GS}>V_{th}$), the conduction path begins to build up at the center of the device for a nanowire device as proposed in (Colinge *et al.*, 2011a) to result in a significant drain current in the device (fig. 1.13 and fig. 1.14). We call it the ON state operation of the JL MOSFET. It may be noted that the carriers have bulk mobility instead of surface mobility as observed in the classical MOSFET. Thus, the carriers do not suffer from mobility degradation due to surface scattering as observed in the conventional MOSFETs working on

the principle of surface inversion phenomenon. The channel carriers mostly suffer from the lattice scattering and impurity scattering due to heavily doped channel. As a result, the effect of temperature variation on the mobility of channel carriers is reported to be smaller in the JL MOSFET than the conventional MOSFET working on the principle of surface inversion (J. P. Colinge, Lee, Afzalian, *et al.*, 2010; Colinge *et al.*, 2011a). When $V_{GS}=V_{FB}$, where V_{FB} is flat band voltage, the device works under the partial depletion mode. When $V_{GS,}$ is increased further, the device starts to work in the accumulation mode where the channel behaves as a simple resistor as demonstrated in fig. 1.14.

The I_D-V_{GS} characteristics (in logarithmic scale) of the bulk MOSFET and JL MOSFET have been compared in fig. 1.15. The bulk MOSFET enters from the flat band into the depletion mode followed by the inversion or ON state condition when the gate voltage gradually increases from the flat band voltage to beyond the threshold voltage the device. On the other hand, the JL MOSFET enters from the depletion to the partial depletion mode followed by the flat band condition when the gate voltage is increased from subthreshold regime to the above threshold regime.

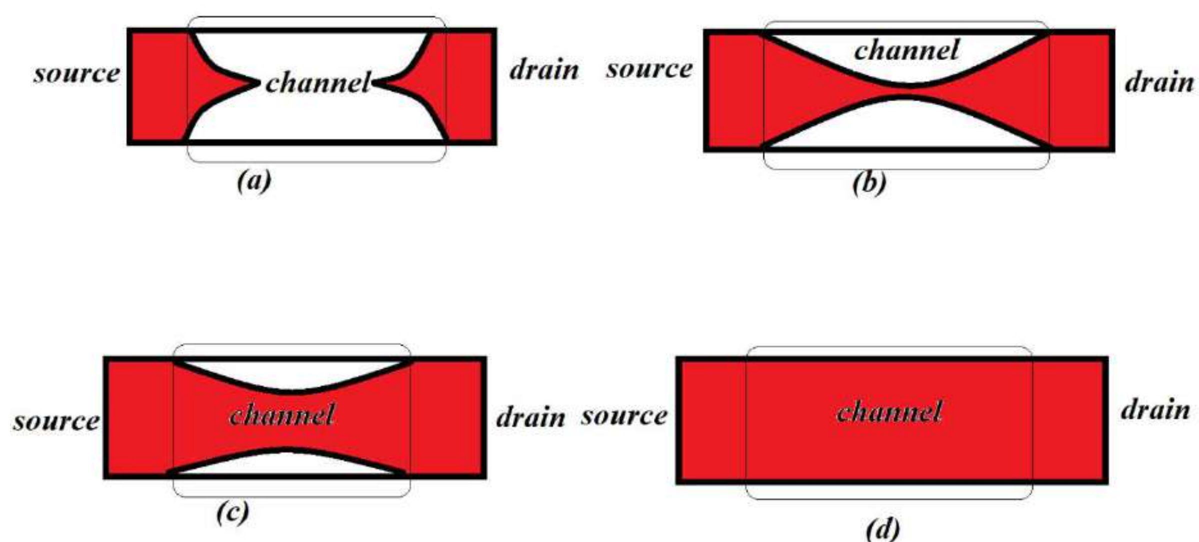

Fig. 1.13: Working of junctionless MOSFET, (a) when $V_{GS}<V_{th}$; (b) when $V_{GS}>V_{th}$; (c) when $V_{GS}=V_{FB}>>V_{th}$; (d) when the device acts as a simple resistor.

That is, the flat band condition is achieved after gate voltage exceeds the threshold voltage. Further, the threshold voltage variation with respect to the change in the doping is much more prominent in the JL MOSFET than the inversion mode MOSFET due to the high doping density in the JL MOSFET (Gnani *et al.*, 2011; Intekhab Amin and Sarin, 2013).

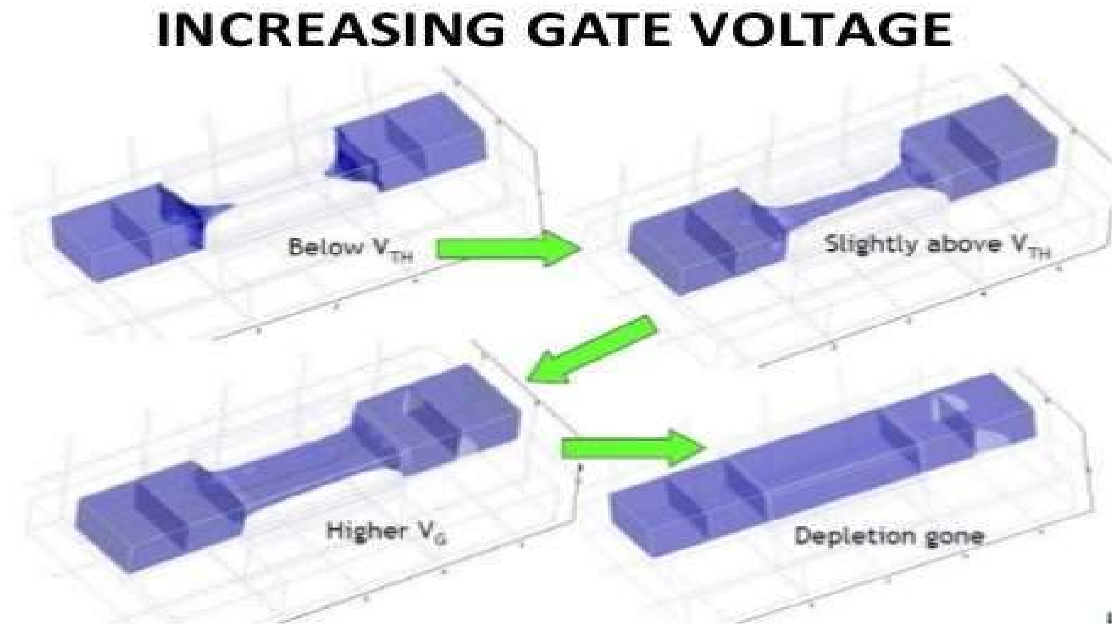

Fig. 1.14: Contour plots describing the working of junctionless MOSFET(Colinge *et al.*, 2011a).

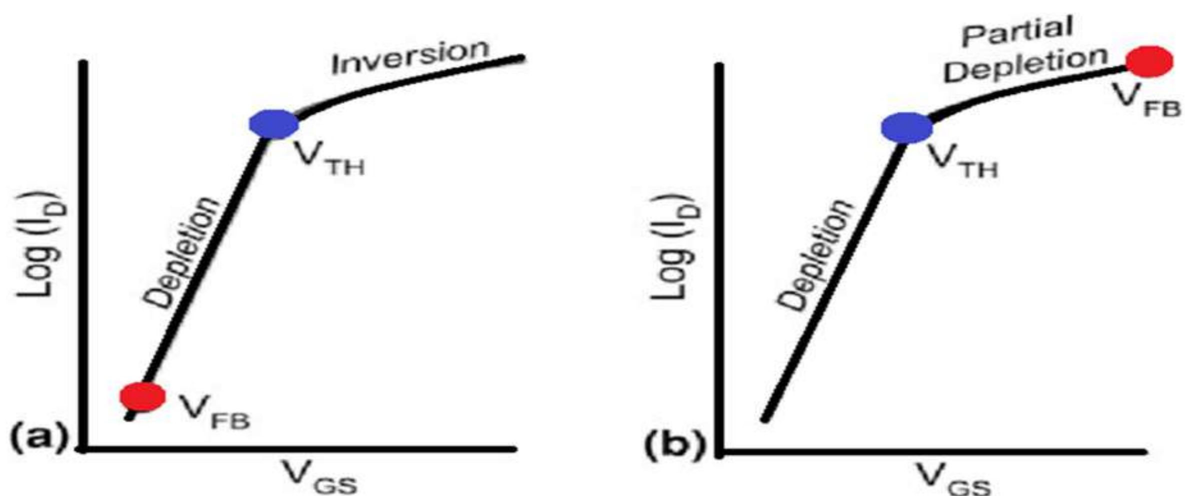

Fig. 1.15: I_D-V_{GS} (in logarithmic scale) comparison for (a) bulk MOSFET; (b) junctionless MOSFET.

The drain currents $I_{D(MOSFET)}$ and $I_{D(JL\,MOSFET)}$ of the inversion mode MOSFET and JL MOSFET are given by the following equations (Colinge *et al.*, 2011a):

$$I_{D(MOSFET)} = \mu \frac{C_{ox}W}{L}(V_{DD} - V_{th})^2 \quad (1.4)$$

$$I_{D(JL\,MOSFET)} = q\mu N_D \frac{T_{si}W}{L} V_{DD} \quad (1.6)$$

where C_{ox} is the oxide capacitance per unit area, T_{si} is the channel thickness, W is the channel width, L is the channel length, μ is the carrier mobility, V_{DD} is the drain voltage and I_D is the drain current of the MOSFET.

It is observed that drain current of the conventional MOSFETs working on the inversion mode depends of oxide capacitance which again depends on the oxide thickness. But, the drain current equation (1.6) of the basic JL MOSFET shows that the drain current is independent on the oxide thickness. Further, the drain current in the JL MOSFET is increased with the channel doping while the current in conventional MOSFET is decreased with increased doping due to the increase in the threshold voltage of the device.

Now the transit time delays τ_{MOSFET} and $\tau_{JL\,MOSFET}$ of the conventional MOSFET and JL MOSFET are given by (Colinge *et al.*, 2011a).

$$\tau_{MOSFET} = \frac{L^2}{\mu V_{DD}} \quad (1.7)$$

$$\tau_{JL\,MOSFET} = \frac{C_{ox}L^2}{qN_D T_{Si}} \quad (1.8)$$

Note that the transit time delay in the surface inversion based MOSFET can be reduced by reducing the channel length (L) since increasing in V_{DD} is against the scaling rules. However, the delay parameter can be reduced by increasing the oxide thickness (which reduces C_{ox}), reducing the channel length (L), increasing the channel doping and increasing the channel

thickness of the JL MOSFET. However, it may be mentioned that the high channel doping in JL MOSFET may reduce the carrier mobility due to impurity scattering, which in turn, may affect the speed of operation of the device. In brief, the optimization of the speed of operation of the JL MOSFET is much easier than the conventional MOSFETs.

Though the JL MOSFETs have several advantages over conventional inversion mode MOSFETs such as the better adaptability to scaling, lower cost of fabrication (due to not having any junction in the channel), lower SCEs, lower I_{OFF} and higher speed of operation, however, it suffers from the following drawbacks. The doping concentration in the source and drain regions are relatively smaller than those of the conventional MOSFETs. As a result, the contact resistances of the source and drain electrodes in the JL MOSFET are higher than those of the conventional MOSFETs. The combined effects of the degraded mobility due to impurity scaling and increased source (drain) contact resistance make the I_{ON} current of the JL MOSFET much smaller than that of the inversion mode MOSFET. Further, the requirement of a high work function gate material to fully deplete the highly doped channel in the JL MOSFET in its OFF state operation is also challenging from practical fabrication point of view (Intekhab Amin and Sarin, 2013). The effect of random dopant fluctuation (RDF) phenomenon in the highly doped channel may also affect the threshold voltage (V_{th}) of the device (Tocci, 2010). It is necessary to engineer basic JL MOS structures to minimize the aforementioned drawbacks as discussed in the following section.

1.3.2 Junctionless Accumulation Mode (JAM) MOSFET: A Modified Junctionless MOSFET Structure

In this section, we will consider a modified form of the basic JL MOSFET structure, called the junctionless accumulation mode (JAM) MOSFET shown in fig. 1.16. The JAM MOSFET structure was first fabricated and reported by S. Barraud *et. al.* in 2012 (Barraud *et al.*, 2012).

Unlike a uniform heavy doping in all the source, channel and drain regions, the JAM MOSFETs have higher doping concentrations in the source and drain regions than the channel region as shown in fig. 1.16 (b). The higher doping in the source and drain regions reduces the source and drain contact resistance, which in turn, makes the I_{ON} higher than the basic JL MOSFET structure. Further, the JAM structure provides also the flexibility of using lower doping concentration in the channel and lower work function material for the gate electrode (than those of the JL MOSFETs) to channel carrier mobility and hence to achieve an acceptable I_{ON}/I_{OFF} ratio (Trivedi, Kumar, Haldar, S. S. Deswal, *et al.*, 2016). Thus, the stringent requirement of a thin channel can be relaxed and the RDF can be reduced by lowering the doping level in the channel of the JAM MOSFETs (Kim *et al.*, 2013).

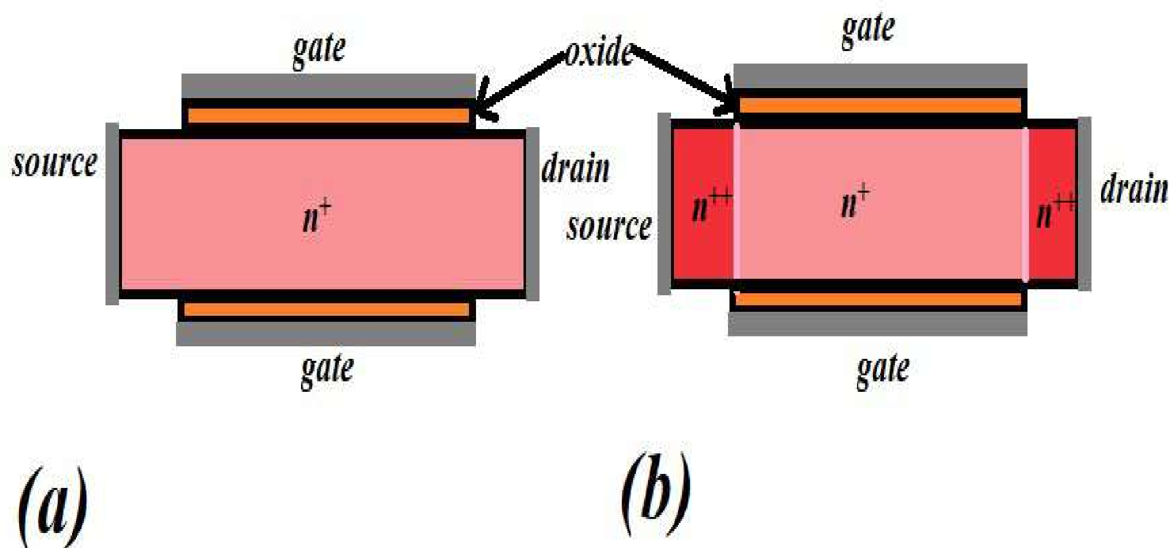

Fig. 1.16: Pictorial representation of double gate (a) basic junctionless MOSFET; (b) JAM MOSFET.

From fabrication point of view, the JAM MOS structure requires an additional implantation step which is still economical from the view of the improved electrical characteristics. The working of JAM MOSFET is almost similar to that of classical junctionless structure. It also works in bulk conduction mode but the flat band condition is reached much earlier than

classical junctionless device as shown in I_D-V_{GS} curve in fig. 1.17 (Baliga, Syau and Venkatraman, 1992). The JAM MOSFET works in accumulation mode and gives a much higher on-current at lower V_{GS} than that of the JL MOSFET. The JAM structure minimizes/removes most of the drawbacks of the JL MOSFETs as discussed earlier.

Due to the bulk conduction in the channel, the vertical channel electric field of the JAM MOSFET is nearly same as that of the JL MOSFET but the lateral electric fields near the channel/drain and source/channel junctions are higher than the channel region due to doping concentration gradients at the junctions. The similar vertical electric field makes the gate leakage current in the JAM structure nearly same as that of the JL MOSFET. However, the high lateral electric fields at the source/channel and drain/channel junction may play significant roles in determining the performance of the JAM MOSFETs (Sahay and Kumar, 2017b). This high field at the channel/drain junction may lead to undesired HCEs and GIDL phenomenon in the JAM MOSFET (Sahay and Kumar, 2017b). The present thesis deals with some theoretical investigations of the electrical performances optimization of gate engineered, channel engineered and gate dielectric engineered JAM MOS structures.

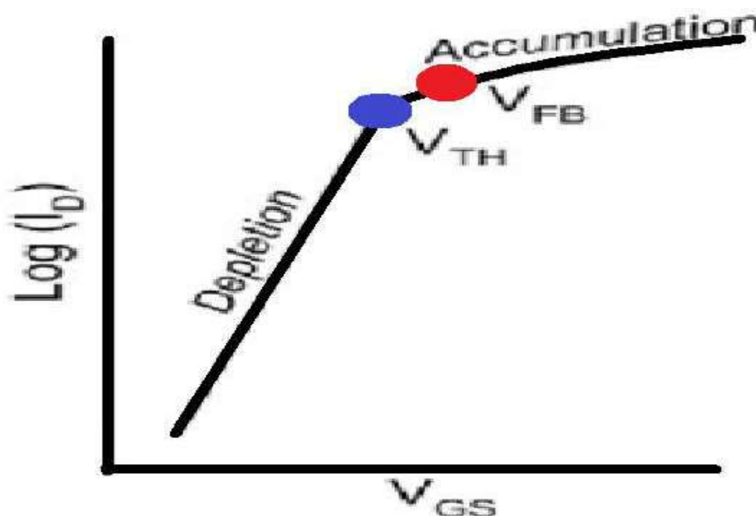

Fig. 1.17: I_D-V_{GS} (in logarithmic scale) of JAM MOSFET.

Thus, the following section is devoted discuss various performance improvements techniques in various forms of engineered JAM MOS structures.

1.4 Engineered JAM MOSFET Structures

The high electric field at the channel/drain junction of the JAM MOSFET may lead to HCE-induced trapped charges, GIDL and leakage current at negative gate bias (Sahay and Kumar, 2017b). Further, it is also desirable to have a high I_{ON} current and low I_{OFF} current to boost up the I_{ON}/I_{OFF} ratio of the device. Various techniques such as the gate engineering, channel doping engineering, gate dielectric engineering and source/drain engineering have been reported in the literature to increase the I_{ON}/I_{OFF} and reduce the HCEs in the inversion mode MOSFETs and JL MOSFETs. They are briefly discussed in the following subsections.

1.4.1 Gate Engineering Technique

The gate engineering technique is basically the modification of the gate structure to boost up the performance of a MOS device. One or the combination of various gate engineering techniques discussed below could be adopted to enhance the performance of JAM MOSFET.

1.4.1.1 Use of multiple-gate structure engineering

The multiple gates in the MOSFETs are used to enhance the control of the gate over the channel for decreasing the SCEs (Song *et al.*, 2009). Various forms of gate structures such as the double gate JL/JAM MOSFET (Holtij *et al.*, 2014), tri-gate JL MOSFET (Holtij, Kloes and Iñíguez, 2015), gate-all-around (GAA) JL/JAM MOSFET (Singh *et al.*, 2011) and nanotube JL/JAM MOSFET (Sahay *et al.*, 2017) have been reported in the literature. Double gate structures use two gates on two sides of the channel which may be a planar structure shown in fig. 1.18) or a Fin-FET-type structure shown in fig. 1.19 (Lee, 2005). The tri-gate structure can be obtained from the double-gate Fin-FET structure of fig.1.19 by maintaining thin oxides in

the top as well as other two sides as shown in fig. 1.20. There are also other tri-gate structures obtained by using an omega-gate (Gao and Chiang, 2013; Chiang, 2015), a pi-gate (Chiang *et al.*, no date) and an inverted-T gate (Chiang, 2016) as shown in fig 1.21. The tri-gate MOS structures have better gate control than double-gate structures. When the channel totally wrapped by the gate in the MOSFETs, they are called gate all-around (GAA) MOS structures. The GAA structure could be a Quadruple- GAA JAM as shown in fig. 1.22, triangular GAA JAM (Mohammad Najmzadeh *et al.*, 2012) and cylindrical JL/JAM structure (Trivedi, Kumar, Haldar, S. S. Deswal, *et al.*, 2016). The cylindrical GAA MOSFETs use a cylindrical channel wrapped from all sides as shown in fig. 1.23. The cylindrical GAA has the advantage over other types of GAA structures due to redundancy of corner effects (i.e. accumulation of charges at the corners) (Xiao-ju *et al.*, 2007). Another novel GAA structure with an inside and outside gate is shown in fig. 1.24 (Sahay *et al.*, 2017). Although this nanotube structure has a better gate control than a simple cylindrical GAA structure but it is very complex to fabricate with the present CMOS technology. The cylindrical GAA MOS structures provide the highest control of the gate over the channel which results in smaller SCEs among all GAA structures. That is why, we have considered the performance analysis of the cylindrical GAA structure based JAM MOSFET in the present thesis.

1.4.1.2 Gate material engineering

Gate material or gate electrode engineering is used to improve the performance of the JL/JAM MOSFET. In this technique, multiple metal-like materials are used in a non-overlapping cascaded manner in place of using a single gate electrode to redistribute the electric potential and fields in the channel region (Lou *et al.*, 2012). The work function values of the metals should be arranged in descending order from the source towards the drain for optimum performance of the device

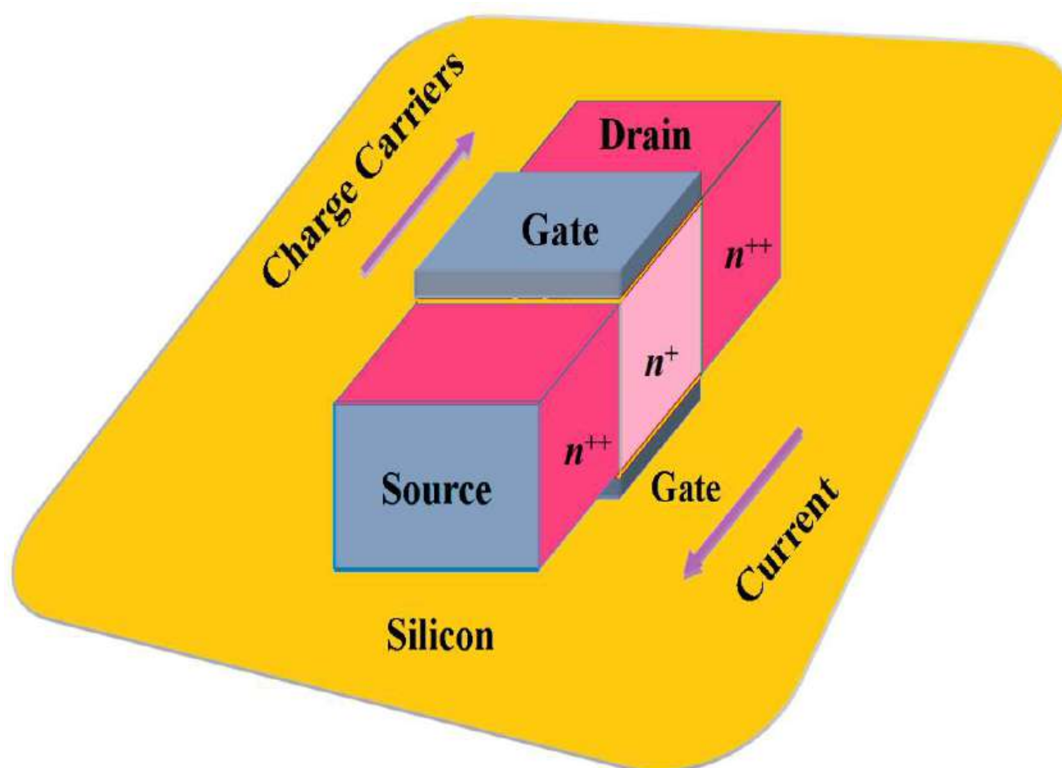

Fig. 1.18: Planar double gate JAM MOSFET.

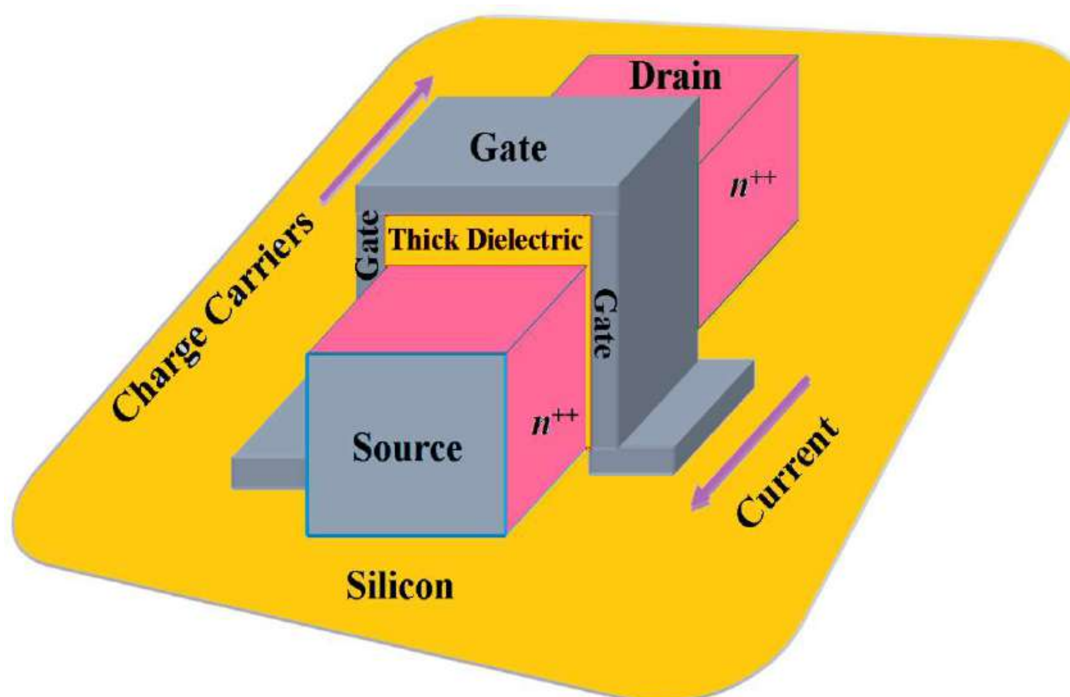

Fig. 1.19: Fin-FET type double gate JAM MOSFET.

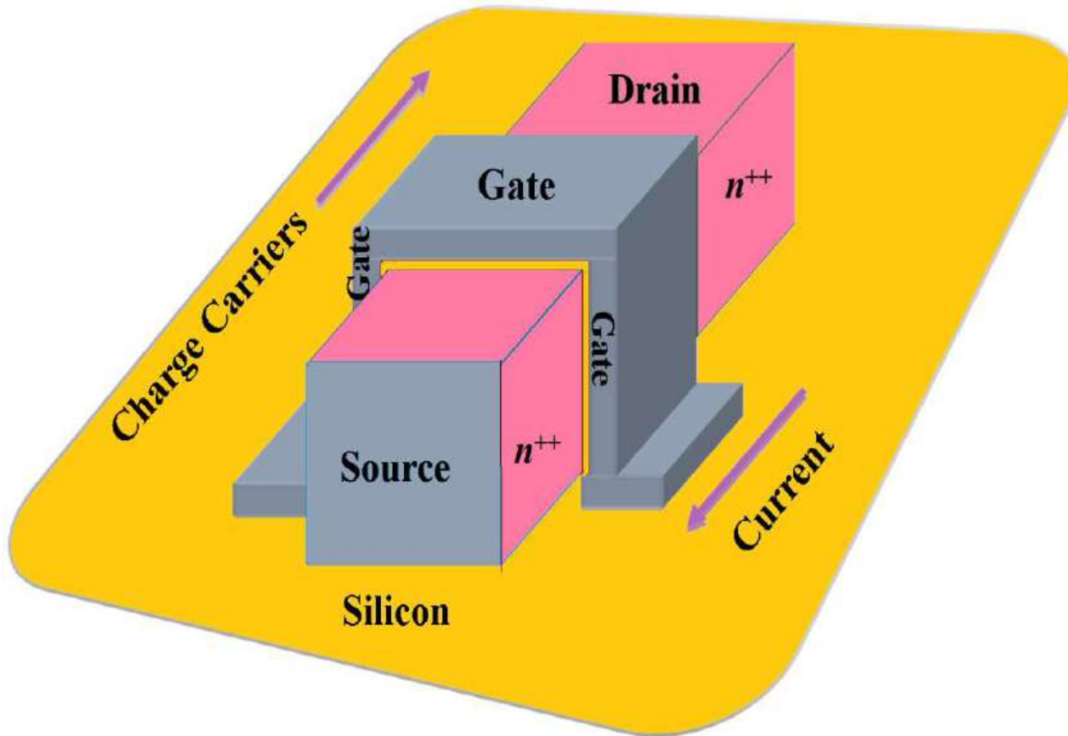

Fig. 1.20: Simple Tri-gate JAM MOSFET.

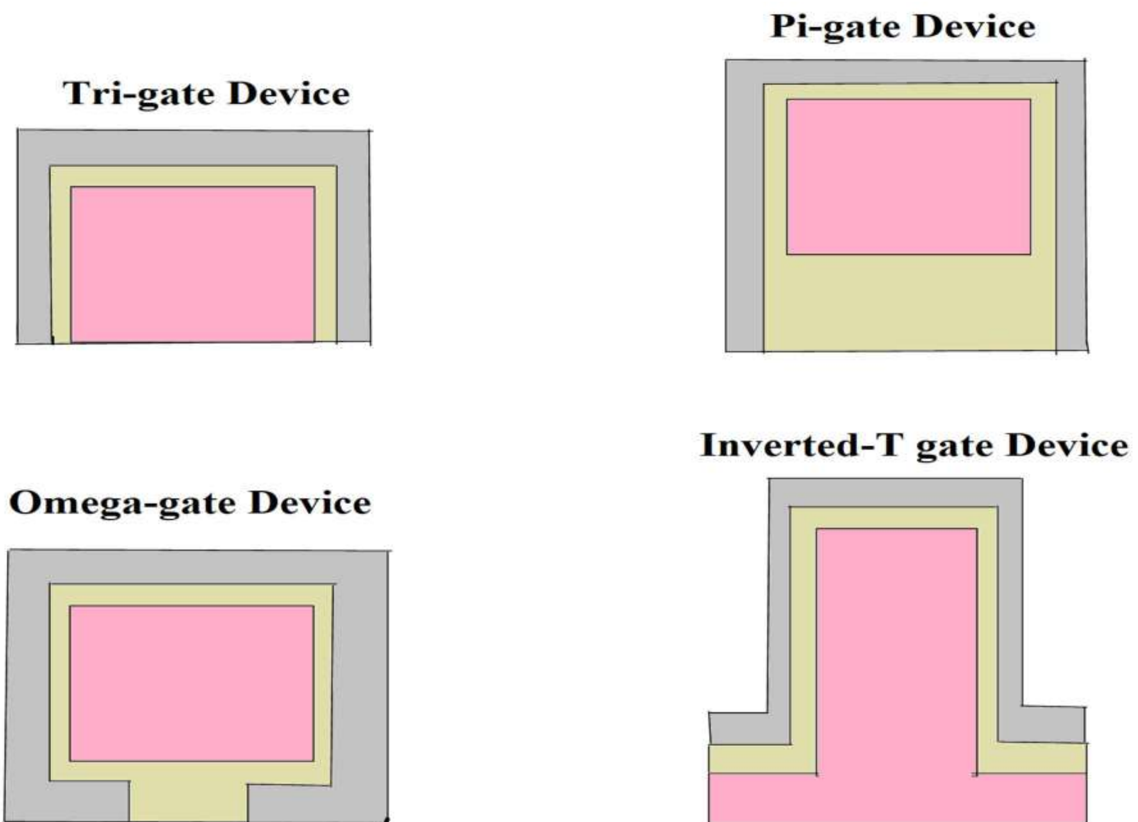

Fig. 1.21: Various types of tri-gate devices.

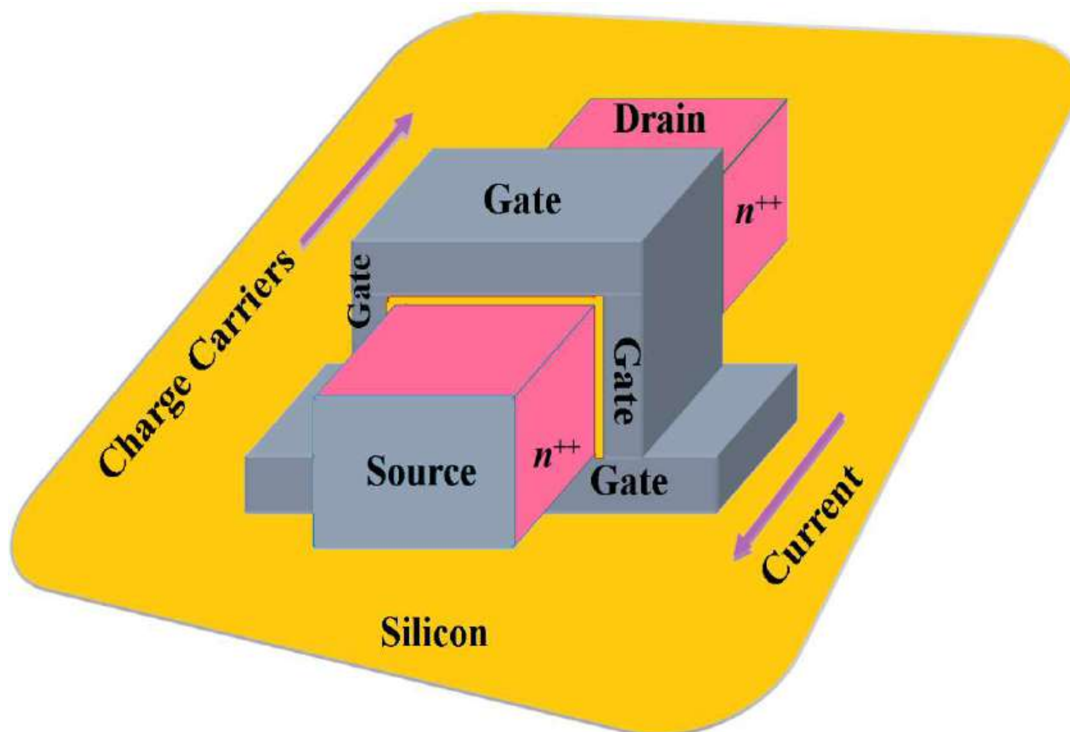

Fig. 1.22: Quadruple GAA JAM MOSFET.

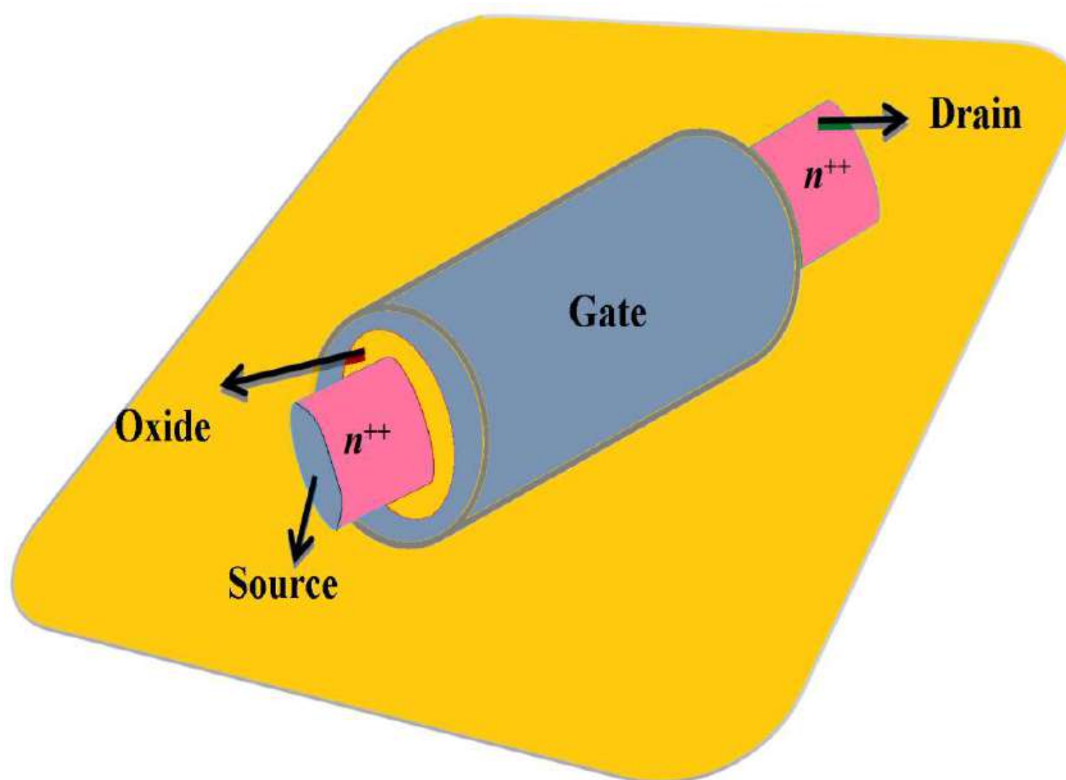

Fig. 1.23: Cylindrical GAA JAM MOSFET.

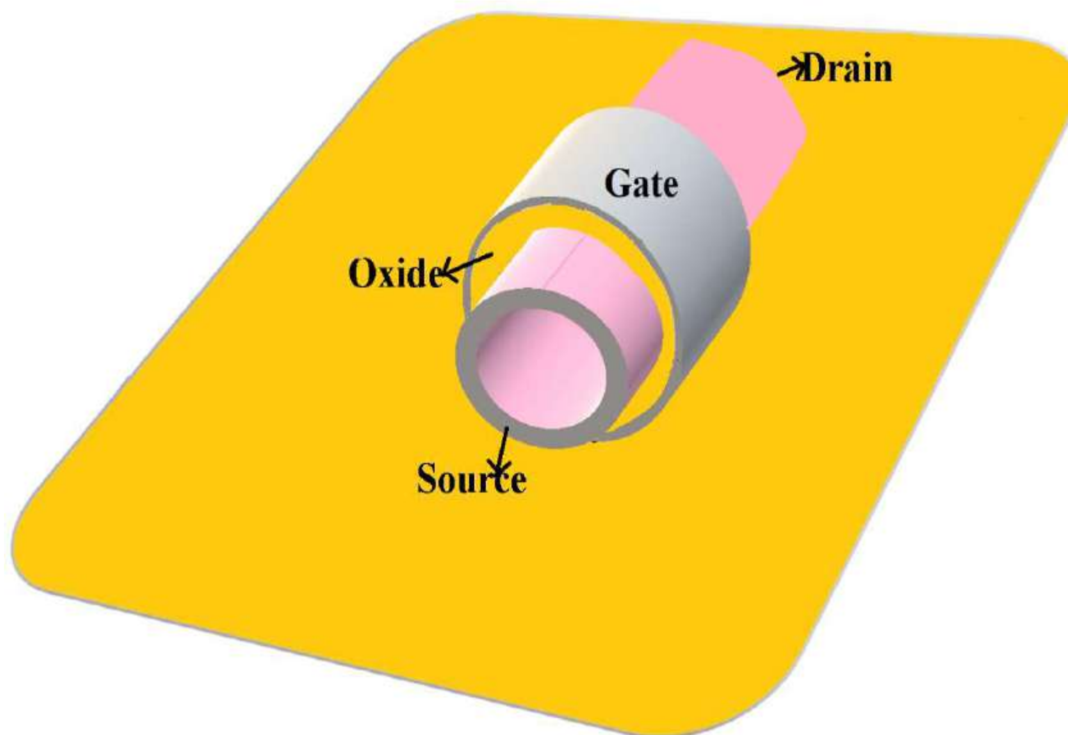

Fig. 1.24: Cylindrical nanotube JAM MOSFET.

(Baruah and Paily, 2014; Li, Y. Q. Zhuang, *et al.*, 2014; Sahay and Kumar, 2016a). The gate-electrode metal place at the source side has the highest work function while the work function of the metal at the drain side should be the lowest one.The gate-metal near the source side controls the injection of carriers from the source to the channel and is thus called the control gate of the device. On the other hand, the gate-metal at the drain side reduces the electric field at the drain side of the channel and is called the screening gate.

The schematic of a dual material gate (DMG) JAM structure is shown in fig. 1.25. The DMG is the simplest form of the gate material engineered structure used to increase the carrier transport efficiency, transconductance, and the drain output resistance in the device by adjusting the channel potential and electric field distributions along the channel (Baruah and Paily, 2014; Li, Y. Q. Zhuang, *et al.*, 2014). The DMG structure also improves the DIBL, SCEs

and subthreshold characteristics of the MOSFETs (Baruah and Paily, 2014). The DMG structure has been explored to decrease L-BTBT induced GIDL in JAM MOSFET (Sahay and Kumar, 2016a).

In principle, multiple gate-electrodes can be connected in a cascade to form various gate-electrode engineered structures. Triple-material-gate (TMG) structures are reported to have better performance characteristics over the DMG structures (Li, Y. Zhuang, *et al.*, 2014). However, the fabrication of multiple gate-electrode materials based structure other than the DMG structure is extremely difficult in the nanoscale gate-length MOSFETs. The fabrication of DMG structure has already been reported by Lin et al. (Lin *et al.*, 2002).

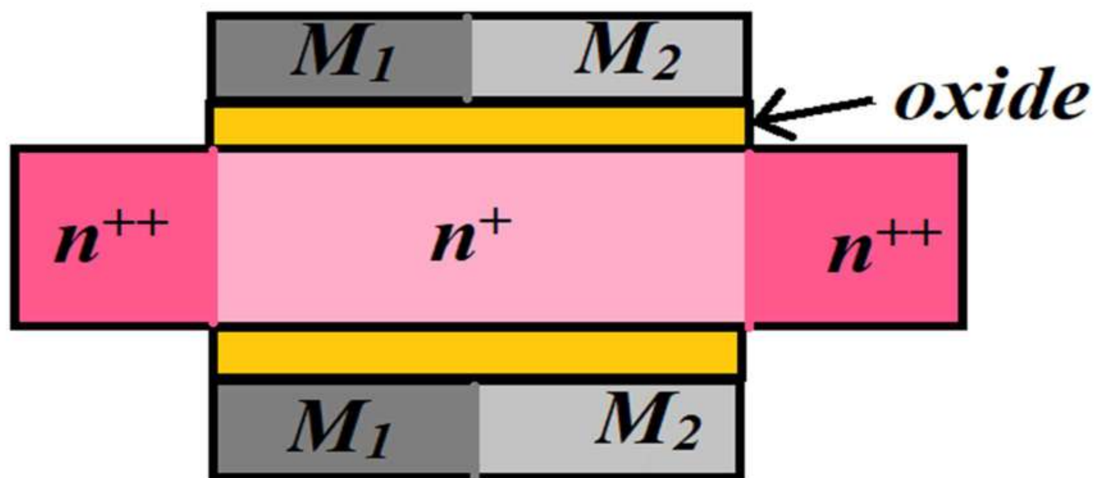

Fig. 1.25: Schematic of DMG JAM MOSFET.

1.4.2 Channel doping engineering technique

In this method, different doping concentrations are used at different sections of the channel of a MOSFET. The doping concentration in the channel can be varied laterally or vertically. A graded channel JAM MOSFET was reported by Chen et al. (Chen *et al.*, 2013a) where the

channel was divided into two regions with a lower doping concentration in the source side than that of the drain side as shown in fig. 1.26. Such a channel doping is shown to reduce the DIBL and HCEs, and to increase the threshold voltage of the device.

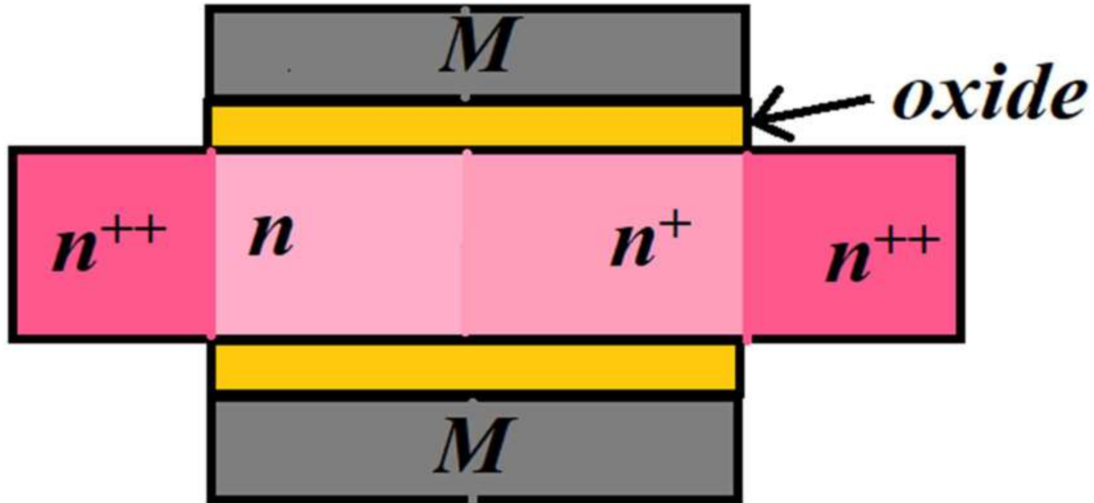

Fig. 1.26: Schematic of laterally graded channel JAM MOSFET.

Channel doping can also be varied in a graded way in a vertical direction. Vertically graded channel devices are called core-shell MOS devices as shown in fig. 1.27. Analytical modeling of vertically graded double gate JL MOSFET was reported by Jaiswal and Kranti (Jaiswal and Kranti, 2019). Simulation studies of tri-gate and cylindrical vertically graded JL MOSFETs have been also reported in the literature (Kumar *et al.*, 2015; Lee *et al.*, 2015).

A non-uniform doping profile can also be used in channel of the MOSFETs. In this direction, the most commonly used doping profile is the Gaussian function defined by

$$f(y) = N_{peak}\, exp\left[-\frac{(y-R_p)^2}{2\sigma^2}\right] \tag{1.9}$$

where N_{peak} is the peak doping concentration, R_p is the projected range, σ is the straggle and "y" represents the vertical direction of doping variation in the channel.

An analytical model of Gaussian doped double gate JL MOSFET was reported by Kumar et al. (Kumari *et al.*, 2018b, 2018a). The Gaussian doping profile provide a better flexibility in optimizing the device performance by controlling N_{peak}, R_p and σ .

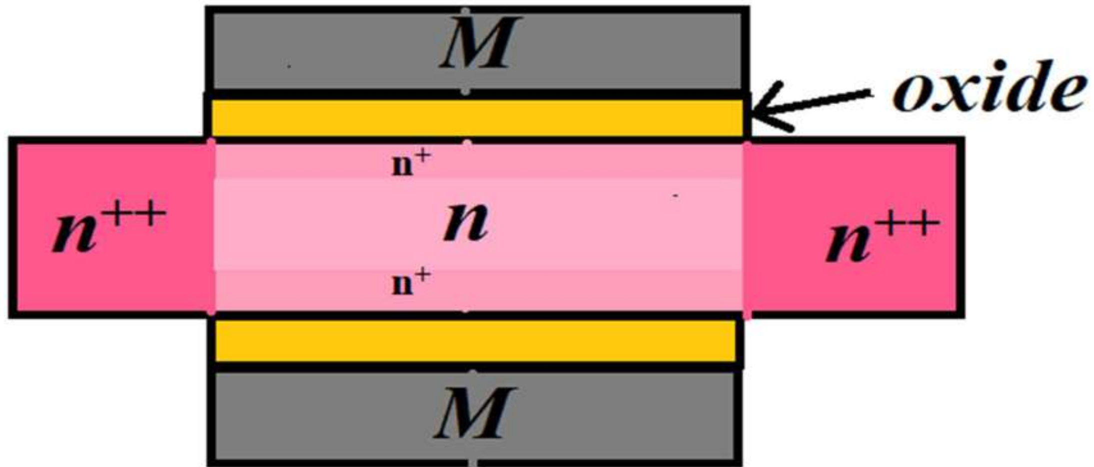

Fig. 1.27: Schematic of vertically graded channel core-shell JAM MOSFET.

1.4.3 Gate dielectric engineering technique

In this technique, the conventional SiO_2 gate oxide is replaced by a different dielectric material (e.g. HfO_2) or a laterally/vertically stacked structure of two different dielectrics. According to the International Technology Roadmap for Semiconductors (ITRS) (ITRS, 2016), the moderns MOS transistors in CMOS ICs require an oxide thickness of 1 nm or even less for achieving higher driving current. Such a thin oxide layer can result in a large gate leakage current, which in turn, can increase the static power loss. Therefore, the SiO_2 is replaced by a high-k dielectric to achieve the same equivalent gate-oxide capacitance but at larger oxide-thickness to reduce the gate leakage current. The high-k dielectric should have the same equivalent oxide thickness (EOT) as that of the SiO_2 where the EOT is defined as

$$EOT = t_{high-} \left(\frac{k_{SiO_2}}{k_{high-}}\right) \tag{1.10}$$

where t_{high-} is the thickness of the high-k layer, k_{SiO_2} is the dielectric constant of the SiO2 and k_{high-k} is dielectric constant of the high-k material.

Since $k_{high-} > k_{SiO_2}$, we observe that $t_{high-k} > EOT$. In other words, we can get the same effect of SiO_2 but at higher oxide thickness. This certainly reduces the gate-leakage current by reducing the probability of the direct tunneling of carriers from channel to the gate. The high-k layer also increases the drive current and reduces the DIBL of the device (Sharma *et al.*, 2016). However, placing a high-k layer directly over the silicon channel may create surface irregularities and may result in the interface trap charges, which in turn, may affect the performance of the MOSFETs. Therefore, the high-k layer may be grown over a thin thermally generated SiO_2 layer to form a vertically stacked gate-oxide structure (Goel *et al.*, 2020) (Kumar *et al.*, 2016) as shown in fig. 1.28.

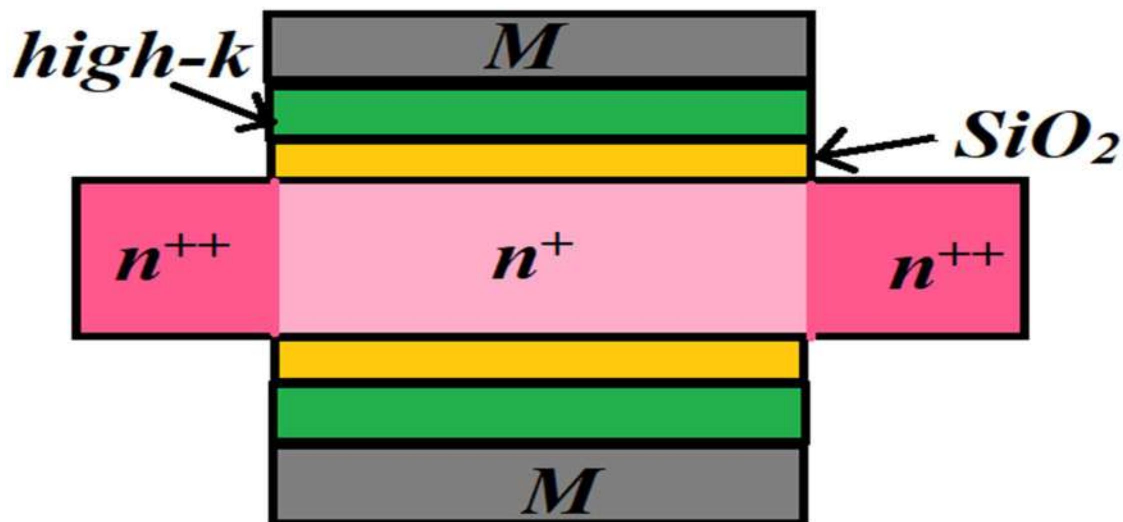

Fig. 1.28: Schematic of vertically stacked gate oxide in JAM MOSFET.

Although the vertically stacked high-k/SiO_2 oxide structure improves the drive current and reduces the gate leakage current but it increases the HCEs due to high electric field at channel/drain interface (Sahay and Kumar, 2017b). High electric field increases the band

overlapping between the valance band of the channel and conduction band of the drain thereby enhancing L-BTBT induced GIDL phenomenon (Sahay and Kumar, 2017b). The tunnelling of electrons from the channel to the drain leaves behind holes which may get multiplied through impact ionization due to high electric field and generate hot carriers (Sahay and Kumar, 2017b). The high field may also create trap charges at the channel/oxide interface and degrades the device operation (Pratap *et al.*, 2015). The left behind holes also contribute to the parasitic n-p-n BJT action with source and drain forming emitter and collector and accumulated holes in the substrate as the base of the BJT, respectively. This reverse biased BJT action (due to positive drain voltage) significantly increases the leakage current of the MOSFETs. To avoid this drawback, a laterally stacked high-*k*/ SiO_2 gate oxide structure shown in fig 1.29 is preferred over the vertically stacked structure in the literature (Ghosh, Akram and Bal, 2014) to reduce GIDL in junctionless MOSFET. A combination of SiO_2 and vacuum dielectric at the drain side is suggested by Pratap et al. (Pratap *et al.*, 2016) to reduce the HCEs. Though the vacuum dielectric at the drain side reduces the HCEs but it increase the gate leakage, reduces the drive current and also reduces the stability of the device (Pratap *et al.*, 2016).

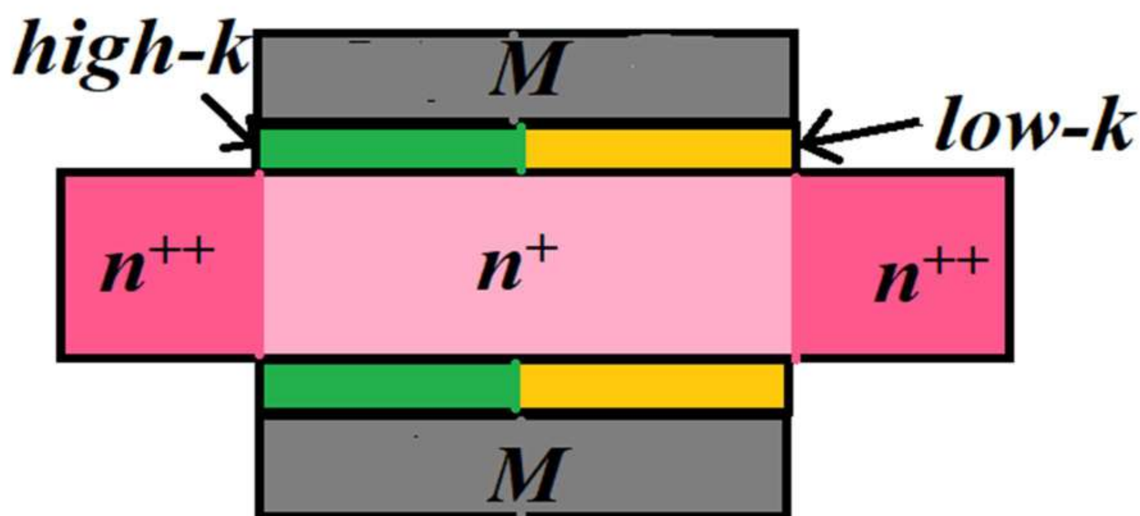

Fig. 1.29: Schematic of horizontally stacked gate oxide in JAM MOSFET.

The combination of both the vertically stacked and laterally gate stacked gate oxide structure has also been reported to reduce the leakage current, SCEs and HCEs with enhanced drive current in the MOSFETs.

1.4.4 Source/drain engineering technique

Several source/drain engineering techniques such as the gate overlap/underlap (Jaiswal and Kranti, 2018), dielectric pocket engineering (Singh *et al.*, 2016)and elevated source/drain (Tang *et al.,* 2013) have been proposed for the performance enhancement of the JAM/JL MOSFET. The underlap technique is used to reduce SCEs in JAM MOSFET (Jaiswal and Kranti, 2018). A schematic of the gate underlapped JAM MOSFET structure is shown in fig. 1.30. The underlapped technique extends the depletion region towards the source (drain) sides beyond the gate edges of the device to increase the effective channel length. The increased channel length, in turn, reduces the SCEs. The dielectric pocket (DP) engineering is also reported to improve the I_{ON}/I_{OFF} current ratio, SS characteristics, and DIBL of the JL MOSFETs (Singh *et al.*, 2016). The schematic of a dielectric pocket engineered JAM MOSFET is shown in fig. 1.31.

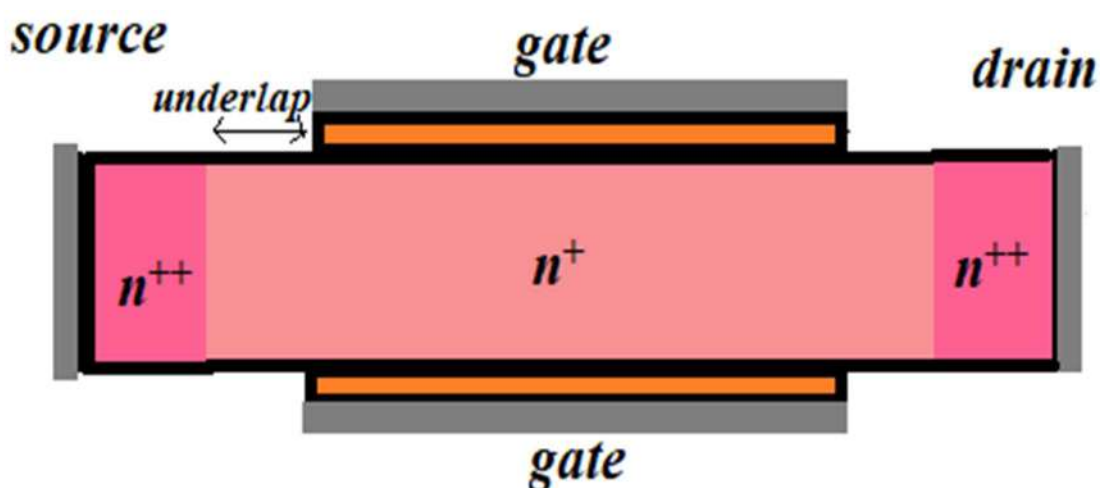

Fig. 1.30: Schematic of gate underlapped JAM MOSFET.

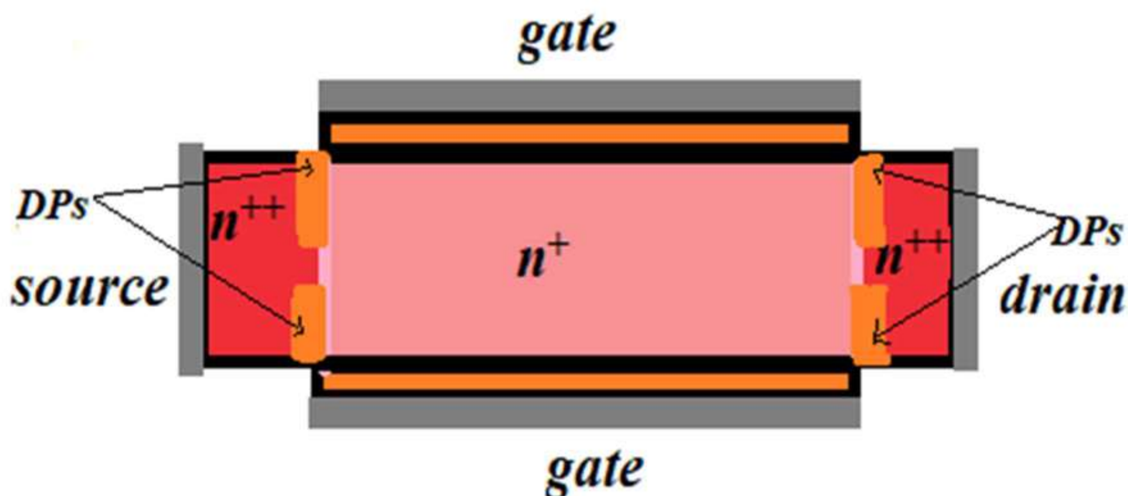

Fig. 1.31: Schematic of dielectric pocket JAM MOSFET.

The device characteristics can be controlled by changing the length and thickness of the DPs. In the elevated source/drain engineering technique, the height of the source/drain is raised above the gate-oxide to improve the drive current of the device. (Tang *et al.,* 2013) have reported an elevated source/drain JAM MOSFET to increase its drive current.

1.5 Review of State-of-the-Art Research on JL/JAM MOSFET

It is discussed that the cylindrical GAA structure in MOS transistors provides the best control over the channel to reduce the SCEs. Further, JAM MOS structure has superior performance parameters over the conventional JL MOS structure. Various other engineering techniques such as the gate-oxide structure engineering and channel engineering can be explored for improving the performance of the MOS transistors. In view of the above, the present thesis is aimed to investigate the performance of some engineered JAM MOSFET structures through theoretical and simulation based analyses. This section is thus devoted to discuss some important state-of-the-art research on the JL/JAM MOSFETs.

1.5.1 Experimental Research on JL/JAM MOSFET

In this subsection, we will consider some state-of-art research on working JL/JAM MOSFETs. The JL MOSFET was first fabricated in Tyndall National Institute by J. P. Colinge *et al.* (J. Colinge *et al.*, 2010; J. P. Colinge, Lee, Ferain, *et al.*, 2010) in 2010 as discussed earlier. They fabricated a tri-gate junctionless MOSFET with a uniformly doped channel. The device showed smaller mobility degradation due to surface scattering than the conventional inversion mode MOSFETs. The JL MOSFET possessed smaller SCEs and better scalability as already discussed in Sec 1.3. In the same year of 2010, Lee *et al.* (C. Lee *et al.*, 2010) fabricated and experimentally analyzed the performances of a tri-gate nanowire inversion mode MOSFET, an accumulation mode P-type MOSFET and a JL MOSFET. It was observed that the temperature sensitivity of the threshold voltage is higher but that of the GIDL is smaller in the JL MOSFET than other two devices. Further, the phonon scattering was shown to be less in the JL MOSFET than other MOS structures.

In 2011, Choi et al. (Choi *et al.*, 2011) fabricated the cylindrical gate GAA JL MOSFET for the first time in the literature. They compared the performance of the cylindrical gate GAA JL MOSFET with that of the conventional inversion-mode MOSFET with the same geometric parameters.

Barraud *et al.* (Barraud *et al.*, 2012) experimentally demonstrated a high-*k* stacked metal gate, tri-gate nanowire JAM MOSFET in 2012. In the same year, Najmzadeh *et al.* fabricated a dense array of triangular high-*k* gate stacked GAA JAM MOSFET (M. Najmzadeh *et al.*, 2012) with sub 5 nm cross-section from a top-down SOI platform. Further, they investigated the effect of quantum confinement on the performance of the device. It was shown that the impurity scattering in the highly doped channel was mainly responsible for the mobility degradation in the JAM MOSFET. Rudenko *et al.* (Rudenko *et al.*, 2012) experimentally investigated the performance of a JL pi-gate MOSFET. In 2012, Goto *et al.* (Goto *et al.*, 2012)

experimentally demonstrated the mobility of channel carriers was significantly higher than the bulk mobility.

In 2013, Trevisoli *et al.* (Trevisoli *et al.*, 2013) compared measured leakage currents of the high-*k* stacked JL MOSFET and inversion mode MOSFET. The GIDL was found much smaller in JL MOSFET than that measured in the inversion mode MOSFET. Further, the gate current was observed to be weakly dependent on both the channel doping and temperature. In the same year, Park *et al.* (Park *et al.*, 2013) investigated the effect of back biasing tri-gate JAM MOSFET and reported that the JAM structure is more sensitive to the back-biasing effect due to the bulk conduction. Further, the effective mobility of the JAM MOSFET was found significantly high below the flat band voltage under back bias operation.

Jeon *et al.* (Jeon *et al.*, 2013a) compared the performance parameters of a working high-*k*/metal (EOT=1.2 nm) gate stacked tri-gate SOI JAM MOSFET with a silicon thickness of 9 nm with those of the inversion mode MOS device. In another work, Jeon *et al.* (Jeon *et al.*, 2013) investigated the effect of the channel width variation on the electrical properties of a tri-gate SOI JAM MOSFET. The device was a high-*k* gate stacked tri-gate device fabricated on a (100) SOI wafer. In the same year, Jeon *et al.* (Jeon *et al.*, 2013b) analysed the low-temperature electrical characteristics of planer high-*k* gate stacked JAM MOSFET fabricated on (100) SOI wafer. Tang *et al.* (Tang *et al.*, 2013) illustrated the performance of an elevated source/drain JAM MOSFET. Moon *et al.* (Moon *et al.*, 2013) demonstrated the fabrication of a vertically 3-D gate stacked quad-gate GAA nanowire JAM MOSFET on a bulk substrate.

In 2016, Park *et al.* (Park *et al.*, 2016) experimentally investigated the subthreshold conduction characteristics of a high-*k*/metal gate stacked SOI planer JAM MOSFET fabricated on (100) SOI wafers. The JAM MOSFET was shown to have a lower effective barrier height at source (drain)/silicon channel junction as compared to that of the conventional inversion-

mode MOSFET. However, JAM MOSFET showed smaller SCEs than the inversion counterpart.

Recently, Jeon *et al.* (Jeon *et al.*, 2020) has experimentally investigated the controlling of the effective channel thickness of the high-k/metal gate-stack JL MOSFET by substrate bias. They also reported the effect of substrate-bias on various electrical characteristics of the JL MOSFET.

1.5.2 Review of Simulation-based Studies on JL/JAM MOSFET

In this sub-section, we will review some simulation-based state-of-art research on JAM/JL MOSFETs. Some important works on device level analyses are considered first. Then some literatures on memory circuit applications of JL/JAM MOSFET are discussed.

1.5.2.1 Device Level Simulation Studies on JL/JAM MOSFETs

In 2009, Lee *et al.* (Lee *et al.*, 2009) used ATLAS-3D TCAD simulator to show smaller SCEs, DIBL, subthreshold swing (SS) degradation of the tri-gate JL MOSFET over conventional inversion mode MOSFETs. The SS of less than 80 mV/dec was reported for a 5 nm gate length device. In the next year, Lee *et al.* (Lee *et al.*, 2010) reported that the shortening of gate length has lesser effect on the DIBL and SS of the tri-gate JL MOSFETs than the inversion mode counterpart. It was also shown that the variation in threshold voltage with the shortening of gate-length can be further reduced by using a gate underlap/overlap JAM MOSFET structure. The threshold voltage was shown to be dependent on the fin width. It was further shown that an increased doping level in the source/drain region could enhance the drive current of the JAM MOSFET without affecting other device characteristics.

Colinge *et al.* (Colinge *et al.*, 2011b) observed that though there are nearly similar electrical characteristics in both the JL MOSFET and inversion mode device but their working principles

are completely different. Unlike the surface inversion mode, the JL MOSFET was demonstrated to work on the bulk conduction mode. Further, the drain current was shown to be independent of the oxide capacitance but it was dependent on the channel doping concentration. A dual material gate JL cylindrical gate MOSFET was simulated Lou *et al.* (Lou *et al.*, 2012). It was shown that the proposed structure better performance in terms of higher ON-current, larger I_{ON}/I_{OFF} current ratio, higher transconductance g_m, higher unity-gain frequency f_T, higher maximum oscillation frequency f_{max}, and smaller DIBL over the conventional JL MOSFETs. Najmzadeh *et al.* (Najmzadeh *et al.*, 2012) investigated the corner effects in equilateral triangle based GAA JAM MOSFET under subthreshold to strong accumulation regime. It was shown that the corners of the proposed structure could accumulate and deplete more electrons than the flat sides or the channel center in above flat-band and below flat-band voltage of operations, respectively. However, no significant corner effect was observed in the inversion mode MOSFET. Chen *et al.* (Chen *et al.*, 2013b) simulated a JL MOSFET with a laterally graded channel doping using the Monte Carlo simulator (MC) with quantum corrections. The laterally graded device was shown to outperform the convention JL MOSFET in terms of higher drain current, transconductance and cut-off frequency. The graded JL MOSFET was shown to possess lower output conductance, higher early voltage and higher intrinsic gain than their basic JL MOSFET structure. Ghosh *et al.* (Ghosh, Akram and Bal, 2014) simulated a horizontally stacked heterodielectric junctionless MOSFET to demonstrate the L-BTBT induced GIDL. The horizontally stacked gate oxide consisted of a high-*k* dielectric at the source side and a low-*k*/SiO_2 at the drain side. The proposed structure was shown to have lower L-BTBT induced GIDL than the conventional JL MOSFET with only low-*k* or only high-*k* as a gate oxide. An effective method to realize the volume depletion in the JL SOI MOSFET was demonstrated by Sahay *et al.* (Sahay and Kumar, 2016c). The OFF-state current was shown to be reduced significantly by replacing SiO_2 with HfO_2 in the buried oxide (BOX)

of the device. It was also shown that the high-*k* BOX could reduce both the gate capacitance C_{gg} and gate-to-drain Miller capacitance C_{gd} of the device. Kumar *et al.* (Kumar and Sahay, 2016) used a hybrid channel with p^+ layer below the n^+ active device layer in the JL MOSFET to reduce the BTBT-induced parasitic BJT action. The p^+ layer worked as hole sink (HS) to result in a significantly low OFF-state leakage current. Sahay *et al.* (Sahay *et al.*, 2016) used a core-shell structure based JL MOSFET with a p^+ core to reduce the L-BTBT induced GIDL current by achieving effective volume depletion in the nanowire of larger width in the device. Reduced L-BTBT induced parasitic BJT action and enhanced I_{ON}/I_{OFF} ratio were achieved in the core-shell JL MOSFET. The L-BTBT induced GIDL current of a cylindrical gate JL MOSFET was compared with JAM MOSFET by Sahay *et al.* (Sahay and Kumar, 2016b). Both the drive current and GIDL leakage current were found to be higher in the JAM MOSFET than their respective values of the JL MOSFET. It was then shown that the dual-material (DM) gate in JAM MOSFET improve the drive current but reduce the OFF-current in the device. Sahay *et al.* (Sahay and Kumar, 2017c) also simulated an extended back gate based double-gate (DG) JL MOSFET to get lower subthreshold swing, lower off-state leakage current and higher I_{ON}/I_{OFF} ratio by quantum confinement-induced bandgap widening. Sahay *et al.* (Sahay and Kumar, 2017a) investigated the diameter dependent leakage current characteristics in the cylindrical gate JL MOSFET. It was shown that the leakage current was dependent on the L-BTBT induced parasitic BJT action for diameter below 10 nm. The leakage current for diameters below 7 nm is very small due to lowering in the L-BTBT tunnelling probability. The device was shown to possess a significantly large off-state leakage current for a diameter above 15 nm due to inefficient volume depletion (Sahay and Kumar, 2017a).

Gupta *et al.* (Gupta and Kranti, 2017) demonstrated the impact ionization induced steep switching in JL MOSFET operating under high drain bias voltages. Both the positive and negative temperature coefficients were observed for the threshold voltage (V_{th}) of the device.

Threshold is decreased with the decrease in temperature due to the dominance of the bipolar effects over the thermal generation of carriers. On the other hand, V_{th} is reduced with an increase in temperature for unipolar characteristics at higher temperatures. Kumari *et al.* (Kumari *et al.*, 2018b) investigated the performance of a Gaussian doped double gate (DG) JL MOSFET. It was reported that the device would give the best performance provided that the peak of the Gaussian doping profile was placed at the oxide/channel interface of the channel. Gupta *et al.* (Gupta and Kranti, 2019) simulated a bi-directional vertically stacked JL MOSFET for operating as both p-MOS and n-MOS in CMOS logic and memory circuit applications.

Recently, Garg *et al.* (Garg, Singh and Singh, 2020) simulated a dual-channel single gate JL MOSFET where two channels were considered on both sides a vertically trenched gate. The proposed structure with a heavy channel doping offered a peak g_m, f_T and f_{max} of 2304 μS/μm, 548 GHz and 830 GHz, respectively, at gate length of 20 nm. Goel et al. (Goel *et al.*, 2020) simulated a dual material (DM) vertically stacked cylindrical gate (CG) JL MOSFET for high-frequency applications. The device showed better performance over the conventional CG JL MOSFET, underlap CG JL MOSFET and underlap DM CG JL MOSFET.

1.5.2.2 Review of JL/JAM MOSFETs in Memory Circuit Applications

In this section, we will review some state-of-art literature related to the application of JL/JAM MOSFETs in memory circuits. Kranti *et al.* (Kranti *et al.*, 2010) used TCAD tool to analyze the performance of a 6-T SRAM cell using 20 nm JL MOSFET. They observed a high static noise margin (SNM) of 185 mV, retention noise or hold margin (RNM) of 381 mV, and write current (I_{WR}) of 33 mA along with a low leakage current (I_{LEAK}) of 2 pA at a supply voltage (V_{DD}) of 0.9 V with pullup ratios of 1. Saini *et al.* (Saini, 2016) improved the performance of a 6-T SRAM cell using asymmetric spacers in 20 nm channel length JAM FinFETs. They used a Dual-*k* spacer at the source side and low-*k* spacer (Dual-*k*S) at the drain

side of the JAM FinFET device. The SRAM cell showed improved performance metrics as compared to SRAMs circuits using low-*k* based JAM FinFET and inversion mode MOSFET even at low supply voltages. The performance of a 6-T SRAM cell designed by using vertically stacked gate oxide-based DG JL MOSFET was analyzed by Tayal *et al.* (Tayal and Nandi, 2018). The high-*k* gate dielectric in the device was shown to improve the static noise margin (SNM) and access time (AT) of the memory cell. Recently, Panigrahi *et al.* (Panigrahi, Sahu and Lenka, 2020) analyzed the performance of a DG JL MOSFET with a Gaussian doping in the channel. They also designed of a 6-T SRAM cell using their proposed device and compared its performance uniformly doped DG JL MOSFET based SRAM cell. Improvement in signal-to-noise margin (SNM) was observed in the proposed SRAM cell without compromising with write access time (AT).

1.5.3 Analytical Modeling of JL/JAM MOSFETs: A Brief Review

Analytical modeling of nanoscale MOS transistors is becoming difficult day by day due to enhanced complexity in the structure of the device to suppress the SCEs in the device. That is why, most of the researchers these days follow TCAD based analysis of the advanced MOS transistors as discussed above. However, the modeling is an important requirement for understanding the physical insight of any device. The present thesis deals with both the TCAD simulation and analytical modeling based investigations of some novel cylindrical gate GAA JAM MOSFETs. Therefore, we will now review some important works on the modeling of JL/JAM MOSFETs in this subsection. Note that the 1-D and 2-D Poisson equations are used the potential function modeling of long-channel and short-channel MOS transistors respectively. That is why, reviews of the 1-D and 2-D models are discussed separately in the following.

1.5.3.1 Review of some 1-D models

In this section, we will discuss some literatures on 1-D analytical models suitable for long channel MOS devices. Jiménez *et al.* (Jiménez *et al.*, 2004) developed an analytical model for the undoped long channel cylindrical gate (CG) MOSFET by solving the 1-D Poisson's equation and current continuity equation without using the charge-sheet approximation (Sallese *et al.,* 2011). The model was valid for all the operating regimes (i.e. linear, saturation, subthreshold) without using any fitting parameters. Yu *et al.* (Yu *et al.*, 2007) presented an explicit model for undoped long channel DG and cylindrical gate (CG) MOSFETs. Cho *et al.* (Cho *et al.*, 2008) developed an analytic current-voltage (I-V) model for long channel doped CG MOSFETs.

A charge-based analytical model for DG JL MOSFET was reported by Sallese *et al.* (Sallese *et al.*, 2011). The model was shown to be valid for all regimes of operation staring from the deep depletion to accumulation regime. Duarte *et al.* (Duarte, Choi and Choi, 2011) derived a full range drain current using 1-D continuous charge model for a DG JL MOSFET. The Poisson's equation was solved by assuming a parabolic approximation for the channel potential in the subthreshold and linear regimes by considering both doped and mobile charges in the channel. The Pao–Sah integral was used for formulating drain current of the device. In another work, Duarte *et al.* (Duarte *et al.*, 2012) developed a non-piecewise drain current model for the long channel CG JL MOSFET by using the Pao–Sah integral and a continuous charge model reported in (Duarte, Choi and Choi, 2011).

Jazaeri *et al.* (Jazaeri, Barbut and Sallese, 2013) formulated a charge-based model for the electrical characteristics of a symmetric DG JL MOSFET. The technological constraints and design limitations of ultrathin body DG JL MOSFETs, relationships between the silicon thickness and the doping concentration, and the compatibility with design requirements in terms of the OFF-state-current and voltages were investigated in details.

Jin *et al.* (Jin *et al.*, 2013a) reported a unified analytical continuous current model applicable for both the DG JAM MOSFET and doped inversion mode MOSFETs. Effects of both the symmetric and asymmetric DG structures were studied for both the doped and inversion/accumulation charges in the channel. The model considers the undoped case as an initial solution to total Poisson's equation with doped charges. Jin *et al.* (Jin *et al.*, 2013b) also developed a continuous current model for the CG JAM MOSFET by considering both the depletion and accumulation charges.

Lime *et al.* (Lime *et al.*, 2014) developed a 1-D compact explicit model for the electrical characteristics of a CG JL MOSFET. The Poisson's equation was solved in the cylindrical coordinates using parabolic potential approximations to obtain a compact model for the drain current of the device. Yu (Yu, 2014) reported a unified analytical current model for p-type and n-type CG JAM MOSFETs using parabolic channel potential approximation based continuous charge model in the cylindrical coordinate system. The model was valid from low to high-doping concentrations in the channel. Hur *et al.* (Hur *et al.*, 2015) in 2015 developed a core compact model for multiple gate JL MOSFET using parabolic potential assumption. An analytical (I-V) model for the DG JL MOSFET was reported by Hwang *et al.* (Hwang, Yang and Lee, 2015). The channel potentials, electric field, mobile charges, and drain current were modelled without any implicit function or special functions. Separate models were developed for full depletion, partial depletion, and accumulation mode of operations of the device. Yesayan *et al.* (Yesayan, Jazaeri and Sallese, 2016) reported charge-based 1-D model for the CG JL MOSFETs by considering the interface trapped charges. Shalchian *et al.* (Shalchian, Jazaeri and Sallese, 2018) reported a charge-based 1-D model for ultrathin DG JL MOSFETs including quantum confinement effects. The analytical derivation was based on the first-order correction to the infinite quantum well assumption.

1.5.3.2 Review of some 2-D models

In this subsection, we will discuss some important reported works on 2-D short channel modeling of MOS devices. Hamid *et al.* (El Hamid, Iñíguez and Roig Guitart, 2007) formulated a 2D analytical model for the threshold voltage, DIBL and SS of the short channel undoped CG MOSFET by considering only the mobile charges in the channel. The 2D potential function was obtained by adding two potential functions obtained by the 1-D Poisson's equation and 2-D Laplace equation. A compact potential-based model for the SS of undoped CG MOSFET was proposed by Ray *et al.* (Ray and Mahapatra, 2008). The model was shown to be valid for weak and strong inversion regime of both long and short-channel transistors. Trevisoli *et al.* (Trevisoli *et al.*, 2012) derived a surface potential based analytical drain current model for triple gate JL MOSFET. Chiang *et al.* (Chiang, 2012; Chiang, 2012) reported a 2-D threshold voltage model for DG and CG JL MOSFETs by considering only the depletion charges. A subthreshold drain current model was reported by Chiang *et al.* (Chiang and Liou, 2013) for the CG JL MOSFET by including the quantum confinement effects. Li *et al.* (Li *et al.*, 2013) reported a 2-D model for the subthreshold characteristics for the CG JL MOSFET using the superposition principle. A subthreshold current model using the superposition principle was reported by Jin *et al.* (X. Jin, Liu, Kwon, *et al.*, 2013) for both the asymmetric and symmetric DG JL MOSFETs. Jazaeri *et al.* (Jazaeri *et al.*, 2013) reported an analytical model for the subthreshold characteristics of ultrathin symmetric DG JL MOSFETs. The 2D-Poisson equation was solved by parabolic approximation technique for modelling the drain current, DIBL and SS of the DG JL MOSFETs. A subthreshold model for the 2D potential was reported by Baruah *et al.* (Baruah and Paily, 2014) for a dual material (DM) DG JL MOSFET with a high-*k* spacer. Mangla *et al.* (Mangla *et al.*, 2014) formulated the channel charge and potential models for the quasi-ballistic nanoscale DG MOSFETs. The subthreshold characteristics of short-channel dual and triple-material gate JL MOSFETs were reported by Li *et al.* (Li, Y. Q. Zhuang, *et al.*, 2014; Li, Y. Zhuang, *et al.*, 2014). Holtij *et al.* (Holtij *et al.*, 2014; Holtij, Kloes and Iñíguez, 2015)

developed compact models for the electrical characteristics of short-channel DG and Tri-gate JL MOSFETs. Huang *et al.* (Huang *et al.*, 2015) developed a surface potential-based quasi-ballistic model for DG MOSFETs with only one extracted parameter. Sharma *et al.* (Sharma *et al.*, 2016) modelled the electrical characteristics of horizontally stacked high-*k* and vacuum with vertically stacked SiO_2 gate-oxide structure based CG JL MOSFETs.

A surface potential based drain current model was proposed by Baruah *et al.* (Baruah and Paily, 2016) for DG JL MOSFETs by considering both the depletion and accumulation charges. Pratap *et al.* (Pratap *et al.*, 2016) developed a potential-based total drain current model for dual material gate asymmetric, horizontally stacked gate-oxide (Al_2O_3 and vacuum) III-V material based CG JL MOSFETs for hot carrier reliability. Trivedi *et al.* (Trivedi, Kumar, Haldar, S S Deswal, *et al.*, 2016) reported an analytical 2-D model for CG JAM MOSFET. They formulated a total drain current model for the device by considering depletion charges in Poisson's equation. However, they neglected the effect of the depletion regions in source and drain regions of the device. Oproglidis *et al.* (Oproglidis *et al.*, 2017) developed a charge-based compact analytical drain current model for the short-channel triple-gate JL MOSFETs by including the saturation velocity overshoot, series resistance, and mobility degradation effects. Jaiswal *et al.* (Jaiswal and Kranti, 2018) reported an analytical model for electrical characteristics of the underlapped DG JAM MOSFETs by considering only the depletion charges. Bae *et al.* (Bae and Yun, 2019) reported a compact analytical model for the subthreshold characteristics of DG JL MOSFETs by considering the effect of depletion regions in the source and drain extension regions.

Gola *et al.* (Gola *et al.*, 2019) reported a static and quasi-static charge-based drain current model of the tri-gate JL MOSFET by including the substrate bias induced effects. The effect of quantum confinement was also included for the better accuracy of the model. Different

capacitances of the device were also modelled. The circuit level performance of the proposed device in the inverter and ring oscillator circuits was analysed using Verilog-A model.

Duksh *et al.* (Duksh *et al.*, 2020) reported a 2-D analytical model for the channel central potential, threshold voltage, subthreshold current and subthreshold swing of the graded channel DG JL MOSFETs. Recently, Preethi *et al.* (Preethi and Balamurugan, 2020) have reported the surface potential, electric field, threshold voltage, drain current and SS of the dual material CG JL MOSFETs.

1.6 Major Observations from the Literature Review: Motivation behind the Present Thesis

After reviewing some important literatures in the above section, we will now summarize some important observations given below:

- The JL MOSFET has better scalability and higher speed of operation than the inversion mode MOSFETs due to the absence of any p-n junctions (Lee *et al.*, 2009).
- JL MOSFETs have smaller scattering, less temperature dependability, smaller mobility degradation with gate voltage, better SS, smaller DIBL, smaller leakage current and lower SCEs over the inversion mode MOSFETs due to the bulk mode of conduction in the former device (C. Lee *et al.*, 2010; J. Colinge *et al.*, 2010; J. P. Colinge, Lee, Ferain, *et al.*, 2010; Choi *et al.*, 2011). These properties make them better suited for analog and RF applications.
- Despite the important advantages of the JL MOSFET as described above, the device suffers from lower drive current due to higher source/drain resistance than the inversion mode MOS device. Further, the reduction in the carrier mobility due to highly doped channel and requirement of high gate work function to make the channel a fully depleted one under OFF state condition are also some important drawbacks of the JL MOSFETs. These drawbacks can be removed by modifying the JL MOSFET structure

in the form of the JAM MOSFET structure (Goto *et al.*, 2012; M. Najmzadeh *et al.*, 2012).

- The JAM MOSFET has higher L-BTBT induced GIDL and gate leakage current than those of the JL MOSFETs due to the enhanced lateral field at drain/channel interface of the former device (Sahay and Kumar, 2017b). Both the dual-material-gate (DMG) approach and graded channel approach have been reported to reduce the lateral field and hence the GIDL and gate leakage current of the JAM MOSFETs (Lou *et al.*, 2012; Chen *et al.*, 2013b; Sahay and Kumar, 2016b; Wang *et al.*, 2017; Li, Y. Q. Zhuang, *et al.*, 2014). It can thus be assumed that the simultaneous exploration of the DMG and graded channel concepts in JAM MOSFETs will certainly reduce the L-BTBT-induced GIDL and gate leakage currents of the device. However, to the best of our knowledge, there are no theoretical models for the gate leakage current and GIDL of the CG JAM MOSFETs.
- The use of horizontally stacked high-*k* and SiO_2 (hetero-dielectric) in the JAM MOSFETs decreases the GIDL and increases the ON-current (Ghosh, Akram and Bal, 2014). Asymmetric hetero-dielectric CG JL MOSFETs with III-V channel materials show reduced HCEs (Pratap *et al.*, 2016). However, no theoretical analysis has been available for investigating the combination effects of graded channel and hetero-dielectric gate oxide on the performance parameters of any MOS transistor. Further, theoretical modeling of the effects of quantum confinements on the threshold voltage of CG JAM MOSFETs could be interesting to many.
- An engineered JL MOSFET with both lateral and vertical stacking of gate-oxide has been reported by Sharma *et al.* (Sharma *et al.*, 2016). A DMG structure is shown to reduce both the SCEs and HCEs (Li, Y. Q. Zhuang, *et al.*, 2014). Modeling of electrical characteristics of short channel intrinsic MOSFETs by considering only the mobile

charges has been reported in the literature (El Hamid, Iñíguez and Roig Guitart, 2007; Ray and Mahapatra, 2008). On the other hand, the 2-D modeling of JL/JAM MOSFETs by considering only the depletion charges has been also reported (Chiang, 2012; Li *et al.*, 2013; Pratap *et al.*, 2016; Sharma *et al.*, 2016). Though 2-D modeling for JL MOSFET by considering both accumulation and depletion charges have been reported in the literature (Trevisoli *et al.*, 2012; Gola *et al.*, 2019) but it is based on some fitting or smoothing parameters to connect different regions of operations of the device. Thus a 2-D potential functional based analytical continuous compact model for engineered JL/JAM MOSFET by considering both accumulation and depletion charges could be very useful for the researchers interested in the physics based modeling of MOS devices.

- A unified model valid for both the inversion and JAM DG MOSFET is presented in the literature (X. Jin, Liu, Wu, *et al.*, 2013). A similar model for the CG JAM has been reported (X. S. Jin *et al.*, 2013). However, reported models are 1-D in nature and hence are valid only long channel devices. The 2-D compact unified continuous modeling for the electrical characteristics of the short-channel JAM and inversion MOSFETs could be of interests to many researchers.
- Performance analysis of uniformly doped JL MOSFET based 6-T SRAM circuits has been reported in the literature (Kranti *et al.*, 2010; Saini, 2016; Tayal and Nandi, 2018; Gupta and Kranti, 2019). Gaussian doped DG JL MOSFET based 6-T SRAM cell has been recently reported by some researchers (Panigrahi, Sahu and Lenka, 2020). However, the performance analysis of the Gaussian doped CG JAM MOSFET based 6-T SRAM cells are yet to be reported in the literature.

In brief, there is an ample opportunities for carrying out research in the modeling and simulation and circuit implementation of engineered JAM MOSFETs. The above observations have motivated to outline the scopes of the present thesis discussed in the following section.

1.7 Scopes and Organization of the Thesis

The objective of the present thesis is to investigate the device and circuit level performance analysis of some engineered CG JAM MOSFET structures through theoretical modeling and TCAD based simulations. 2-D analytical models have been developed by considering only depletion charges as well as by considering both the depletion and accumulation charges of the engineered CG JAM MOSFETs. Both the gate material engineering and gate oxide engineering have been explored for the performance improvement of the devices. Attempt has been made to achieve the combined benefits dual material (DM) gate structure and laterally stacked High-k/SiO_2 gate-oxide structure in the JAM MOSFETs. On the other hand, the graded channel (GC) engineering is combined with the vertical Gaussian doping engineering for improving the device and circuit level performances of the CG JAM MOSFETs. The above channel engineered CG JAM MOSFETs have been also used to design a 6-T SRAM cell. TCAD tool COGENDA^{TM} has been used to validate the theoretical models developed in this thesis. The Verilog-A model has been implemented in Cadence^{TM} for investigating the performance of the 6-T SRAM cell under study.

The thesis contains total 7 chapters including the present chapter. The contents of the remaining Chapters 2-7 are briefly outlined in the following:

Chapter-2 presents the 2-D analytical modeling and simulation of CG GC DM JAM MOSFET. The expressions for the potential functions and electric fields have been obtained by solving the 2-D Poisson's equation using the superposition technique. The threshold voltage was obtained by the minimum central potential method. An expression for the total drain

current including GIDL and gate leakage current has also been derived. The validity of the proposed analytical models is shown by comparing the model results with commercially available TCAD COGENDA^{TM} simulation data. The better performance characteristics of the CG GCDM JAM MOSFET is shown over the CG-GC JAM and CG-DM JAM MOSFETs.

Chapter-3 presents the 2-D analytical modeling and simulation of CG HDGC JAM MOSFET using similar method as discussed in Chapter-2. The threshold voltage was obtained by the minimum central potential method as in Chapter-2. The effects of quantum confinement on the threshold voltage are included by solving the Poisson-Schrödinger equation. Models for the drain current model, GIDL, transconductance, and output conductance are also developed. The validity of the model is achieved by comparison the model results with TCAD data. The better electrical characteristics of the CG HDGC JAM MOSFET in terms of lower SCEs and HCEs, higher drive current and larger I_{ON}/I_{OFF} ratio over CG-GC and CG JAM MOSFETs have been discussed.

Chapter-4 considers a 2-D compact DC analytical model of the CG HDGCDM JAM MOSFET. The expressions of the potential and electric fields have been obtained by solving Poisson's equation by considering both the depletion and accumulation charges. The potential functions for all the operating regimes (depletion and accumulation) have been developed. The effects of quantum and electrical confinements, the effect of temperature on mobility and the effect of interface trap charges have also been included in the model for better accuracy. Threshold voltage has been modeled by depletion approximation and minimum central potential method. Models for the drain current, GIDL, transconductance and output conductance have also been modeled. Validity of the proposed models is established by comparing them with the commercial TCAD data. Better electrical performance characteristics of the proposed CG HDGCDM JAM MOSFET structure over the CG JAM MOSFET have been shown.

Chapter-5 presents a unified quasi ballistic 2-D analytical model for CG JAM and CG inversion MOSFET. Both the accumulation and depletion charges have been considered in the 2D Poisson's equation for obtaining the potential function. A continuous potential model across all operating regimes (depletion and accumulation) is derived. The threshold voltage is modeled by the minimum potential method. The drain current model by considering the backscattering factor (free carrier path) has been developed for all operating regimes. The transconductance and output conductance have also been modeled. The validity of the model is shown by comparing the model results with the TCAD simulation data. Though the CG inversion MOSFET shows higher drive current and transconductance over the CG JAM MOSFET but the CG JAM MOSFET possesses lower SCEs and higher I_{ON}/I_{OFF} over the inversion MOSFET.

Chapter-6 investigates TCAD based device and circuit level analysis the Gaussian doped CG JAM MOSFETs. Both the DC and RF/Analog performances of the device have been discussed in details. The Verilog-A model implemented in Cadence^{TM} has been used for the performance analysis of a 6-T SRAM circuit designed by the proposed Gaussian doped CG JAM MOSFETs under study. Various performance parameters such as the signal-to-noise margin (SNM), N-curve analysis, and access time (AT) of the 6-T SRAM cell have also been studied. Effect of the Gaussian profile parameters on the performance of the SRAM was also investigated.

Chapter-7 summarizes the major findings of the present thesis. Finally, some future scopes of research in the related area of the present thesis have been outlined at the end of this chapter.