

CONTENTS

<i>List of Figures</i>	xi-xviii
<i>List of Tables</i>	xix
<i>List of Abbreviations</i>	xx-xxiv
<i>Preface</i>	xxv-xxviii

Chapter 1	Page No.
Introduction and Organization of the Thesis	01-52
1.1 Introduction	01
1.2 MOS Transistor Scaling	02
1.2.1 Power Management in CMOS ICs	05
1.2.2 Short Channel Effects (SCEs) in Classical MOSFETs	07
1.3 Non-Classical MOSFETs for Sustaining Scaling	14
1.3.1 Working of the Junctionless MOSFET	16
1.3.2 Junctionless Accumulation Mode (JAM) MOSFET: A Modified Junctionless MOSFET Structure	20
1.4 Engineered JAM MOSFET Structures	23
1.4.1 Gate Engineering Technique	23
1.4.1.1 Use of multiple-gate structure engineering	23
1.4.1.2 Gate material engineering	24
1.4.2 Channel doping engineering technique	29
1.4.3 Gate dielectric engineering technique	31
1.4.4 Source/drain engineering technique	34
1.5 Review of State-of-the-Art Research on JL/JAM MOSFET	35
1.5.1 Experimental Research on JL/JAM MOSFET	35
1.5.2 Review of Simulation-based Studies on JL/JAM MOSFET	38
1.5.1.1 Device Level Simulation Studies on JL/JAM MOSFETs	38
1.5.1.2 Review of JL/JAM MOSFETs in Memory Circuit Applications	41
1.5.3 Analytical Modeling of JL/JAM MOSFETs: A Brief Review	42
1.5.3.1 Review of some 1-D models	42
1.5.3.2 Review of some 2-D models	44
1.6 Summary of the Literature Review: Motivation behind the Present	47

Thesis	
1.7 Scope and Chapter Outline of the Thesis	50

Chapter 2

2-D Analytical Modeling and Simulation of Gate and Drain Leakage Currents in CG GC-DM-JAM MOSFET 53-79

2.1 Introduction	53
2.2 Analytical modeling	54
2.2.1 Modeling of Device Potential	55
2.2.2 Modeling of the lateral electric field	60
2.2.3 Modeling of threshold voltage	60
2.2.4 Modeling of threshold voltage roll-off and DIBL	61
2.2.5 Drain current modeling	62
2.2.6 Subthreshold slope modeling	64
2.2.7 Gate leakage current modeling	65
2.3 Result and discussion	66
2.4 Conclusion	79

Chapter 3

2-D Analytical Modeling and Simulation of Electrical Characteristics of Ultrathin Body CG HD-GC-JAM MOSFET 80-112

3.1 Introduction	80
3.2 Device fabrication and model formulation	81
3.2.1 Modelling of Channel Potential	83
3.2.1.1 Energy band gap correction for quantum effects	84
3.2.1.2 Modelling of the lateral electric field	88
3.2.2 Modelling of the threshold voltage	89
3.2.2.1 Modeling of threshold voltage roll-off and DIBL	91
3.2.3 Modelling of the Drain Current	91
3.2.3.1 Modelling transconductance and output conductance	93
3.2.3.2 Subthreshold slope modelling	94
3.3 Results and discussion	94
3.4 Conclusion	112

Chapter 4

A 2-D Compact DC Model for Engineered CG- JAM-MOSFETs Valid for All Operating Regimes 113-144

4.1	Introduction	113
4.2	Analytical model formulation	115
4.2.1	Modeling of device potential	117
4.2.1.1	Effect of band gap narrowing and device temperature	117
4.2.1.2	Effect of structural and electrical quantum confinement	118
4.2.1.3	Solving 1-D Poisson's equation	120
4.2.1.4	Solving 2-D Laplace's equation	122
4.2.1.5	Modelling of lateral electric field	124
4.2.2	Formulation of threshold voltage	124
4.2.2.1	Modelling of threshold voltage roll-off and DIBL	126
4.2.3	Total drain current modelling with GIDL	126
4.2.3.1	Subthreshold Slope modelling	129
4.3	Simulation setup	130
4.4	Result and discussion	132
4.5	Conclusion	144

Chapter 5

A Unified 2-D Compact Quasi-Ballistic Model for CG- JAM and Inversion Mode MOSFET 145-170

5.1	Introduction	145
5.2	Formulation of the 2-D analytical model	145
5.2.1	The solution of 1-D Poisson's equation	148
5.2.2	The solution of 2-D Laplace's equation	150
5.2.3	Threshold voltage formulation	152
5.2.4	Formulation of DIBL	153
5.2.5	Drain current modeling	153
5.2.6	Modeling of transconductance (g_m) and output-conductance(g_d)	155
5.3	Simulation setup and model validation	155
5.4	Results and discussion	158
5.5	Conclusion	170

Chapter 6

Effect of Gaussian Doping on Vertically Stacked Oxide CG- JAM MOSFET: An Electrical and Circuit Level Analysis 171-196

6.1	Introduction	171
6.2	Device structure and simulation procedure	172
6.2.1	Device structure	173
6.2.2	Simulation procedure	173
6.3	Results and discussion	177
6.3.1	DC analysis	177
6.3.2	RF analysis	181
6.3.3	Static and transient analysis of CMOS inverter	185
6.3.4	Static and dynamic analysis of 6T SRAM	189
6.4	Conclusion	195

Chapter 7

Conclusion and Future Scope	197-204	
6.1	Introduction	197
6.2	Chapter-Wise Summary and Conclusion	197
6.3	Future Scopes of Work	203
<i>References</i>	205-227	
<i>Author's Relevant Publications</i>	228	

LIST OF FIGURES

Fig 1.1:	Evolution of the semiconductor industry as the result of <i>Moore's law</i> (Internet resource, IR1).	3
Fig 1.2:	The ITRS roadmap of transistor development (Internet resource, IR2)	3
Fig 1.3:	Variation of supply voltage and threshold voltage against technology generation (Packan, 2007).	5
Fig 1.4:	Variation of power density against gate length scaling of MOS device (Meyerson, 2004).	6
Fig 1.5:	Variation of drain current against gate-to-source voltage of MOS device (Internet resource, IR3).	7
Fig 1.6:	(a) Variation of DIBL with the drain to source voltage (1 V and 50 mV) (b) energy band diagram representation of DIBL.	10
Fig 1.7:	The process of band to band tunneling (BTBT) in MOSFET giving rise GIDL.	11
Fig 1.8:	The mechanism of direct gate tunneling as gate oxide leakage.	11
Fig 1.9:	The mechanism of ballistic transport in MOSFET.	12
Fig 1.10:	Generation of hot carriers in bulk MOSFET device (Internet resource., IR3).	13
Fig 1.11:	TEM image of five gated nanoribbon and magnified image of a single nanoribbon, (Colinge et al., 2011a).	15
Fig 1.12:	Schematic structure of the basic bulk JL MOSFET structure	16
Fig 1.13:	Working of junctionless MOSFET, (a) when $V_{GS} < V_{th}$; (b) when $V_{GS} > V_{th}$; (c) when $V_{GS} = V_{FB} \gg V_{th}$; (d) when the device acts as a simple resistor.	17

Fig 1.14:	Contour plots describing the working of junctionless MOSFET (Colinge et al., 2011a).	18
Fig 1.15:	I_D - V_{GS} (in logarithmic scale) comparison for (a) bulk MOSFET; (b) junctionless MOSFET.	18
Fig 1.16:	Pictorial representation of double gate (a) classical junctionless MOSFET; (b) JAM MOSFET.	21
Fig 1.17:	I_D - V_{GS} (in logarithmic scale) of JAM MOSFET.	22
Fig 1.18:	Planar double gate JAM MOSFET.	25
Fig 1.19:	Fin-FET type double gate JAM MOSFET.	25
Fig 1.20:	Simple Tri-gate JAM MOSFET.	26
Fig 1.21:	Various types of tri-gate devices.	26
Fig 1.22:	Quadruple GAA JAM MOSFET.	27
Fig 1.23:	Cylindrical GAA JAM MOSFET.	27
Fig 1.24:	Cylindrical nanotube JAM MOSFET.	28
Fig 1.25:	Schematic of DMG JAM MOSFET.	29
Fig 1.26:	Schematic of laterally graded channel JAM MOSFET.	30
Fig 1.27:	Schematic of vertically graded channel core-shell JAM MOSFET.	31
Fig 1.28:	Schematic of vertically stacked gate oxide in JAM MOSFET.	32
Fig 1.29:	Schematic of horizontally stacked gate oxide in JAM MOSFET.	33
Fig 1.30:	Schematic of gate underlapped JAM MOSFET.	34

Fig 1.31:	Schematic of dielectric pocket JAM MOSFET.	35
Fig 2.1:	Cross-section view of cylindrical gate GCDM-JAM MOSFET.	55
Fig 2.2:	(a) Simulation model calibration against experimental Id-V _{gs} data of Junctionless-FET from (Fan et al., 2015). (b) Simulated energy band structure for all three devices. (c) Variation of Carrier temperature with a channel length (simulated). (d) A 3-D view of simulated cylindrical gate GCDMJAM- MOSFET.	69
Fig 2.3:	Central channel potential along the channel length at $V_{DS}=V_{GS}=0.1V$, $R=5$ nm, $L=40$ nm and 20 nm (a) for $L_1:L_2=1:3$; (b) $L_1:L_2=3:1$.	71
Fig 2.4:	(a) Central channel potential along the channel length at $V_{DS}=V_{GS}=0.1V$, $L_1:L_2=1:1$ and at $R=5$ nm, 7 nm; (b). Lateral electric field along the channel length at $V_{DS}=1$ V, $V_{GS}=0.1V$ -high field, $L_1:L_2=1:1$ and $R=5$ nm.	73
Fig 2.5:	Lateral electric field along the channel at ($V_{DS}=V_{GS}=0.1V$)-low field at (a). $L=40$ nm, 20 nm and $L_1:L_2=1:1$; (b). $L=40$ nm, $L_1:L_2=1:1$ and $L_1:L_2=3:1$.	74
Fig 2.6:	(a) Threshold voltage; (b) roll-off, variations with variation of channel length, at ($V_{DS}=0.5V$) for $L_1:L_2=1:1$.	75
Fig 2.7:	(a) Drain current (in log scale) variations with variation of gate voltage at $V_{DS}=1$ V; (b) GIDL current variations against drain voltage; (c) gate current variations with gate voltage at $V_{DS}=1$ V; (d) gate current variation with temperature at $V_{DS}=V_{GS}=1$ V; with $L_1:L_2=1:1$.	77
Fig 2.8:	(a) DIBL; (b) Subthreshold slope, with variation in channel length at $L_1:L_2=1:1$.	78
Fig 3.1:	A schematic of HDGC JAM MOSFET fabrication steps.	82
Fig 3.2:	3-D view of nanowire HDGCJAM- MOSFET.	82
Fig 3.3:	Cross-section view of nanowire HDGCJAM- MOSFET	83

Fig 3.4:	(a) Calibration of the simulation setup with the experimental results obtained in (Fan <i>et al.</i> , 2015); (b) Simulated carrier temperature variations against channel length for all compared devices.	96
Fig 3.5:	Contour plot of carrier temperature against device length for HDGC-JAM and JAM MOSFET.	97
Fig 3.6:	Central channel potential along the channel length (a) for $L=40$ nm, $L=20$ nm at $V_{DS}=V_{GS}=0.1$ V; (b) $L=40$ nm at $V_{GS}=0.1$ V, $V_{DS}=0.5$ V for three different devices structures.	98
Fig 3.7:	Central channel potential along the channel length for different $L_1:L_2$ (a) $L=40$ nm, $L=20$ nm at $V_{DS}=V_{GS}=0.1$ V; (b) $L=40$ nm at $V_{GS}=0.1$ V, $V_{DS}=0.5$ V of GC-JAM MOSFET.	99
Fig 3.8:	Central channel potential along the channel length for $L_1:L_2$ (a) $L=40$ nm, $L=20$ nm at $V_{DS}=V_{GS}=0.1$ V; (b) $L=40$ nm at $V_{GS}=0.1$ V, $V_{DS}=0.5$ V, of HDGC-JAM MOSFET.	100
Fig 3.9:	Lateral electric field along the channel ($V_{DS}=V_{GS}=0.1$ V) for HDGC-JAM, GC-JAM, and JAM MOSFETs, ($L=20$ nm and 40 nm) at (a) $V_{DS}=0.1$ V; (b) $V_{DS}=1$ V.	102
Fig 3.10:	Lateral electric field along the channel ($V_{DS}=V_{GS}=0.1$ V) with $L_1:L_2$ ratio (1:3, 1:1 and 3:1) for (a) HDGC-JAM; (b) GC-JAM.	103
Fig 3.11:	(a) Threshold voltage variations with the variation of channel length, ($V_{DS}=0.1$ V, 0.5 V and 1 V); (b) roll-off for HDGC-JAM, GC-JAM, and JAM MOSFETs.	104
Fig 3.12:	Threshold voltage variations with variation of channel length, ($V_{DS}=0.1$ V, 0.5 V and 1 V) for (a) HDGC-JAM; (b) GC-JAM, with $L_1:L_2$ ratio (1:3, 1:1 and 3:1).	105
Fig 3.13:	Threshold voltage variation with channel length in QM and CL for (a) HDGC-JAM, GC-JAM and JAM MOSFETs ($R=3$ nm); (b) HDGC-JAM ($L_1:L_2=1:1$) for ($R=1$ nm, 3 nm, and 5 nm).	106
Fig 3.14:	(a) Simulated energy band diagram for all compared devices; (b) GIDL against drain voltage variations at ($V_{GS}=-1$ V) for all devices considered for comparison in Table 3.1.	107

Fig 3.15:	(a) Drain current (logarithmic scale) considering GIDL against gate voltage variations at ($V_{DS}=1$ V, $L=20$ nm and $V_{DS}=1$ V, $V_{DS}=0.05$ V, $L=40$ nm); (b) g_m at $V_{DS}=1$ V; for all compared devices.	108
Fig 3.16:	(a) Drain current against drain voltage at $V_{GS}=1$ V, $V_{GS}=0.8$ V and $L=40$ nm; (b) g_d at $V_{GS}=1$ V; for all compared devices.	109
Fig 3.17:	(a) DIBL; (b) SS with variation in channel length for HDGC-JAM, GC-JAM and JAM MOSFETs.	110
Fig 4.1:	A 2-D cross-sectional view of CG-SHDGCDM-JAM MOSFET.	116
Fig 4.2:	A schematic of HDGC JAM MOSFET fabrication steps.	116
Fig 4.3:	(a) Calibration of the simulation setup with experimental results in (Choi <i>et al.</i> , 2011) (b) Validity of our model with modeled results of (Li <i>et al.</i> , 2014 ^[6] ; Trivedi, Kumar, Haldar, S. S. Deswal, <i>et al.</i> , 2016 ^[4] ; Banerjee and Sarkar, 2019 ^[9]).	132
Fig 4.4:	(a) Central potential variation at V_{GS} (0.1, 0.5, 1 V) (b) Lateral electric field variation at V_{GS} (0.1, 1 V); against length of the channel for ($L_1:L_2=1:3, 1:1, 3:1$) at for SHDGCDM-JAM.	133
Fig 4.5:	Central potential variation vs length of the channel (a) $V_{DS}=1$ V (b) $V_{DS}=0.1$ V; for $L=20$ nm and 40 nm at ($V_{GS}=0.1, 0.5, 1$ V). Lateral electric field vs length of the channel (c) $V_{DS}=0.1$ V, $V_{GS}=0.1$ V (d) $V_{DS}=1$ V, $V_{GS}=1$ V; at $L=20$ nm and 40 nm for JAM and SHDGCDM-JAM MOSFET.	135
Fig 4.6:	(a) Central potential vs V_{GS} at $z=L/2$ and $L=40$ nm for JAM and SHDGCDM-JAM MOSFET (b) Central Potential variation vs length of the channel for SHDGCDM-JAM ($R=3, 5, 7$ nm) at ($V_{GS}=0.1, 0.5, 1$ V).	136
Fig 4.7:	(a) Threshold voltage (b) Roll-off; vs channel lengths at $V_{DS}=1$ V for SHDGCDM-JAM and JAM MOSFET ($R=3, 5, 7$ nm).	137
Fig 4.8:	(a) I_D vs V_{GS} (log scale) for JAM and SHDGCDM-JAM at ($V_{DS}=1$ and 0.05 V; $L=40$ nm); inset –band diagram for devices (b) I_D vs V_{GS} (linear scale) for SHDGCDM-JAM at ($V_{DS}=1$ V; $R=5$ nm $L=40$ nm)	139

and device temperature ($T=200, 300, 400, 500 K$) (c) I_D vs V_{DS} for ($V_{GS}=1$ and $0.8 V$) (d) g_m at $V_{DS}=1 V$.

- Fig 4.9:** (a) DIBL (b) SS ($V_{DS}=1 V$; $R=1 nm$); vs channel lengths for JAM and SHDGCDM-JAM. **140**
- Fig 4.10:** (a) Central potential vs length of the channel at ($V_{GS}=0.1$ and $1 V$) (b) Threshold voltage (c) threshold voltage vs trapped charges density (d) I_D (log scale) vs V_{GS} ; at $V_{DS}=1 V$ for SHDGCDM-JAM and JAM MOSFET with \pm interface trapped charges at R_2 . **143**
- Fig 5.1:** A cross-sectional view of JAM and inversion mode MOSFET. **147**
- Fig 5.2:** Calibration of TCAD simulation setup with experimental results of, (a) junctionless MOSFET (Choi *et al.*, 2011), (b) IM MOSFET (Song *et al.*, 2006); (c) Validation of our proposed model with other reported 2-D models of junctionless MOSFET (Li *et al.*, 2013)^[8] and IM MOSFET (Liu and Li, 2012)^[29]. **157**
- Fig 5.3:** (a) Continuity of middle central potential with the variation of V_{GS} for $V_{DS}=0.5 V$ and $1 V$ ($L=40 nm$), (b) continuity of middle surface potential with the variation of V_{GS} for $V_{DS}=1 V$ ($L=20 nm$); in both JAM and IM MOSFET. **161**
- Fig 5.4:** Variation of central channel potential with position along the channel; (a) at $V_{GS}=0 V$ and $V_{DS}=1 V$, (b) at $V_{GS}=0.5 V$ and $V_{DS}=1 V$; for various channel lengths of $L= 40 nm, 20 nm$ and $10 nm$ for both JAM and IM MOSFET. **162**
- Fig 5.5:** (a) Variation of central channel potential with position along the channel at ($V_{GS}=1 V$ and $V_{DS}=1 V$) for various channel lengths of $L= 40 nm, 20 nm$ and $10 nm$ in both JAM and IM MOSFET, (b) variation of channel surface potential with position along the channel at ($V_{GS}=0 V, 0.5 V, 1 V$ and $V_{DS}=1 V$) for channel length of $L=20 nm$ in both JAM and IM MOSFET. **163**
- Fig 5.6:** Variation of central channel potential with position along the channel at $V_{GS}=0 V$ and $V_{DS}=1$ with channel length $L=20 nm$; (a) for radius $R=5 nm, 7 nm$ and $10 nm$, (b) for oxide thickness $t_{ox}=1 nm, 2 nm$ and $3 nm$; (c) for different channel doping concentration [JAM MOSFET (5×10^{17} - 5×10^{18}) and IM MOSFET (5×10^{16} - 5×10^{17})]; in both JAM and IM MOSFET. **164**

Fig 5.7:	(a) Variation of threshold voltage with the channel length, (b) variation of roll-off with channel length; at $V_{DS}=1$ V for compared devices.	166
Fig 5.8:	Variation of DIBL with channel length for compared devices.	166
Fig 5.9:	(a) Variation of drain current (I_D) with V_{DS} at $V_{GS}=1$ V, (b) variation of drain current (I_D) with V_{GS} at $V_{DS}=1$ V and 0.5 V (in both linear and logarithmic scale); for compared devices.	167
Fig 5.10:	(a) Variation of transconductance g_m with V_{GS} at $V_{DS}=1$ and 0.5 V, (b) variation of output conductance g_d with V_{DS} at $V_{GS}=1$ V in linear and logarithmic scale.	168
Fig 6.1:	2-D cross-section diagram of Gaussian doped channel in stacked oxide CG-JAM MOSFET.	173
Fig 6.2:	(a) Variation of channel doping against the radius of the channel for different straggle length (b) 2-D view of doping variations along channel radius for straggle length of 3 nm.	173
Fig 6.3:	Calibration of simulation models with experimental results in (Choi <i>et al.</i> , 2011).	175
Fig 6.4:	Calibration Verilog-A model with TCAD simulation of complimentary drain current characteristics for stacked oxide CG-JAM p-MOSFET and n-MOSFET to implement COMS inverter at straggle length=1nm and $V_{DS}=1$ V.	176
Fig 6.5:	The workflow of the circuit level simulation procedure.	176
Fig 6.6:	(a) I_D - V_{GS} at $V_{DS}=1$ V; (b) I_D - V_{DS} at $V_{GS}=1$ V at different straggle lengths.	179
Fig 6.7:	(a) Variation of Transconductance (g_m) and drain conductance (g_d) with V_{GS} , $\log(g_d)$ with V_{GS} (inset); (b) variation of intrinsic gain with V_{GS} at different straggle lengths.	180

Fig 6.8:	(a) Variation of capacitances C_{gg} , C_{gs} and C_{gd} with V_{GS} ; (b) Variation of f_T with V_{GS} for different straggle length.	183
Fig 6.9:	(a) Variation of gain bandwidth (GBW) product with V_{GS} ; (b) variation of transconductance frequency product (TFP) with V_{GS} for different straggle length.	184
Fig 6.10:	(a) Variation of transit time (τ) product with V_{GS} ; (b) variation of f_{max} with V_{GS} for different straggle length.	185
Fig 6.11:	(a) Variation of noise margin and gain of the inverter with straggle length; (b) variation of inverter current with straggle length.	187
Fig 6.12:	(a) Variations of transient characteristics of the inverter with straggle length; (b) variation in short circuit transient current with straggle length.	188
Fig 6.13:	Schematic of a 6T SRAM cell.	189
Fig 6.14:	(a) Variation of read noise margin (RNM) of SRAM with straggle length; (b) variation of write noise margin (WNM) with straggle length.	192
Fig 6.15:	(a) Variation in N-curve of SRAM with straggle length; (b) setup for N-curve measurement.	193
Fig 6.16:	(a) Assessment of RAT for different straggle lengths; (b) variation of RAT with straggle length.	194
Fig 6.17:	(a) Assessment of WAT for different straggle lengths; (b) variation of effective WAT with straggle length.	194

LIST OF TABLES

Table. 2.1: Specifications of different JAM MOSFET structures	67
Table. 3.1: Specifications of different JAM MOSFET structures	95
Table. 4.1: Comparison of different 2-D models	114
Table. 4.2: Specifications of Different Structures	131
Table. 5.1: List of various extracted parameters for simulation	156
Table. 5.2: Device physical and geometrical parameters	158
Table. 6.1: Device specifications	174
Table. 6.2: Specification of threshold voltage and I_{on}/I_{off} for various straggle lengths of Gaussian doped CG-JAM MOSFET	180
Table. 6.3: Transient parameters of CMOS Inverter	189