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Date: 15/01/2021

(***Kamalaksha Baral***)

Dedicated

To

The one omnipotent, omnipresent almighty who in the form of my parents, my supervisor and my colleagues have helped me sail through this journey

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LIST OF ABBREVIATIONS

Abbreviation	Details
JAM	Junctionless Accumulation Mode
JL	Junctionless
BTBT	Band-to-band Tunneling
DG	Double Gate
TFET	Tunnel Field Effect Transistor
1-D	One Dimensional
2-D	Two Dimensional
3-D	Three Dimensional
SCEs	Short Channel Effects
HCEs	Hot Carrier Effects
GAA	Gate All Around
MOS	Metal Oxide Semiconductor
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon-on-Insulator
IC	Integrated Circuit
GIDL	Gate Induced Drain Leakage
SS	Subthreshold Swing
SMG	Single Material Gate
TMG	Triple Material Gate
DMG	Dual/Double Material Gate
CMOS	Complementary Metal Oxide Semiconductor

BJT	Bipolar Junction Transistor
TEM	Tunneling Electron Microscope
BOX	Buried Oxide
DIBL	Drain Induced Barrier Lowering
TCAD	Technology Computer-Aided Design
ITRS	International Technology Roadmap for Semiconductors
EOT	Equivalent Oxide Thickness
DP	Dielectric Pocket
NW	Nanowire
DUV	Deep UV lithography
ALD	Atomic Layer Deposition
L-BTBT	Lateral-Band to Band Tunneling
HS	Hole Sink
DM	Dual Material
JLFET	Junctionless Field Effect Transistor
SNM	Static Noise Margin
RNM	Read Noise Margin
WNM	Write Noise Margin
SRAM	Static Random-Access Memory
6-T	6-Transistor
f_T	Unity Gain Frequency
TFP	Transconductance Frequency Product
GBW	Gain Bandwidth Product
f_{max}	Maximum Frequency of Oscillation
RAT	Read Access Time
WAT	Write Access Time

CG	Cylindrical Gate
GC	Graded Channel
GC-DM	Graded Channel Dual Material
HD-GC	Hetero-dielectric Graded Channel
SHD-GC-DM	Stacked Hetero-dielectric Graded Channel
RF	Radio Frequency
IM	Inversion Mode
AT	Access Time
BTE	Boltzmann Transport Equation
M-C	Monte-carlo
E_g	Energy Band Gap
Vel_0	Ballistic Velocity
E_C	Conduction Band energy
E_V	Valance Band Energy
q	Electronic Charge
T	Temperature in Kelvin
KT	Thermal Energy
V_T	Thermal Voltage
V_{th}	Threshold Voltage
I_D	Drain Current
$N_{S/D}$	Source/Drain Doping
N_{ch}	Channel Doping
g_m	Transconductance
g_d	Output-Conductance
I_{ON}	ON Current
I_{OFF}	OFF Current

I_{leak}	Leakage Current
V_{GS}	Gate-to-Source Voltage
V_{DS}	Drain-to-Source Voltage
t_{si}	Channel Thickness
w_{si}	Width of the Channel
t_{ox}	Oxide Thickness
R	Radius of the Channel
L	Length of the Channel
χ	Electron Affinity
ψ	Potential Function
nm	Nanometer
V	Voltage
L	Channel Length
eV	Electron Volt
mA	Milli Ampere
µm	Micro Meter
V_f	Quasi-fermi Level
ni	Intrinsic Concerntration
m_e	Effective Mass
h	Plank Constant
λ	Wave Function
U	Potential Energy
E	Discreatized Energy
r	Radial Coordinate
z	z-Coordinate

θ	Radial Coordinate
μ	Mobility
V_{tL}	Long Channel Threshold Voltage
SS	Subthreshold Slope

Preface

As the CMOS technology node is scaled down below 90 nm in accordance with Moore's law, a number of challenges have emerged in the optimized performance of the MOS transistors. The most important of them is the fabrication of sharp p-n junctions in a nanoscale inversion mode (IM) MOSFET. A severe increase in short channel effects (SCEs) and subthreshold power leakage with the decrease in channel length is also a major aspect of scaling. These challenges call for some unconventional MOS device structure. Junctionless (JL) MOSFETs are MOS devices that have no p-n junctions and thus are easier to fabricate in nanoscale. Conventional JL structures are highly doped structures with the same level of doping throughout the source, channel, and drain. These transistors have lower SCEs and subthreshold power leakage than conventional IM MOSFETs. Due to the bulk mode of operation, surface scattering and threshold voltage variability with temperature are also lower for these devices. However, low drive current and random dopant fluctuation (RDF) due to high doping is a drawback of conventional JL transistors. The low drive current is due to increased source/drain resistance and a decrease in mobility due to high doping. Junctionless accumulation mode (JAM) MOSFET, a modified version of conventional JL MOSFETs with higher doping in source/drain than the channel, with the same type of dopant is fast replacing conventional JL structure due to its high drive current. Although the JAM MOSFETs delivers high drive current but it suffers from gate leakage, gate induced drain leakage (GIDL) and hot carrier effects (HCEs) due to high drain /channel interface electric fields. Various device design engineering like multi-gate engineering (*i.e.,* double gate, tri-gate, gate all around, etc.), gate material engineering (*i.e.,* a combination of same or different materials with different work functions in cascade to form the gate electrode), gate oxide engineering (*i.e.,* lateral/vertical stacking of high-*k*/SiO2), channel engineering (*i.e.,* lateral graded channel, vertical graded channel, vertical Gaussian doping) and source/drain engineering (*i.e.,* elevated source/drain, source/drain underlap) reported enhancing the performance of JL MOSFETs can also be used in JAM MOSFET to enhance its performance and reduce these unwanted effects. In this perspective, the present thesis deals with some theoretical investigations of performance characteristics of some gate-electrode, gate-oxide structure engineered, channel engineered and simple cylindrical gate (CG) JAM MOSFET. Under gate-electrode engineering, the dual-

material (DM) gate structure has been explored to reduce the gate leakage current and SCEs. DM gate structure consists of cascade connection of gate electrodes with two different/same metal but with different workfunction in a non-overlapped way. The gate electrode near the source side is of a higher workfunction called control gate whereas the gate electrode near the drain side is of a lower workfunction called screen gate. The sum of the control and screen gate is the total length of the gate. Under gate-oxide engineering, we have explored the lateral and vertical stacking of high-k/SiO_2. Instead of using a single layer of SiO2 a vertical stacking with high-k increases the physical thickness of the gate dielectric which effectively reduces leakage current and interface states. Horizontal stacking of high-k/SiO_2 in a non-overlapped manner (with high-k in the source side and SiO_2 in the drain side) increases the on-state current and reduces the HCEs. Under channel engineering, we have explored the effectiveness of lateral graded doping and vertical gaussian doping. Lateral graded doping consists of lower doping at the source end of the channel and higher doping at the drain end of the channel. Vertical Gaussian doping consists of higher doping at the surface which progressively decreases as it reaches the center of the channel. Lateral graded doping suppresses SCEs, GIDL and DIBL whereas vertical Gaussian doping decreases subthreshold current, DIBL and enhances RF parameters. Quantum confinement effects along the width of the channel, effect of temperature and operation of the device in both depletion and accumulation region have been explored in this present thesis. Quasi-ballistic transport in simple JAM MOSFET has also been studied in the present thesis. Further, a compact DC model for doped IM MOSFET has also been formulated using the DC-compact model for JAM MOSFET. The overall chapter-wise layout of the thesis is presented below:

Chapter-1 presents a brief introduction of JL and JAM MOSFETs and their working mechanism. Various reported techniques applied for enhancing the performance of JAM MOSFETs have also been discussed. A brief review of various state-of-the-art fabrication-based simulation-based and analytical modeling-based literatures on JL/JAM MOSFET has been presented. Finally, based on the literature survey, the scopes of the present thesis have been outlined at the end of this chapter.

Chapter-2 presents 2-D analytical modeling of device potential, electric field, threshold voltage, roll-off, DIBL and SS of CG GC-DM JAM MOSFET. 2-D Poisson's equation in depletion approximation has been solved using the superposition principle by applying appropriate boundary conditions and the threshold voltage has been obtained using the

minimum central potential method. Further total drain current including GIDL and gate leakage current have also been modeled. Furthermore, the performance metrics of CG GC-DM JAM MOSFET have been compared with CG GC JAM and CG DM-JAM MOSFET based on electrical characteristics, for various control and screen gate length. The modeled results were corroborated with numerical simulation results from COGENDA™

Chapter-3 reports the 2-D analytical modeling of device potential, electric field and threshold voltage, roll-off, DIBL and SS of CG HD-GC JAM. The superposition principle has been used to solve 2-D Poisson's equation in depletion approximation in the same way as discussed in chapter-2. Threshold voltage has also been modeled similarly as in chapter-2. The effect of quantum confinement along the width of the cylindrical channel on threshold voltage has been implemented using quantum well approximation. The drain current has been modeled at negative gate bias considering GIDL. Further transconductance and output-conductance have also been modeled utilizing the drain current model. The performance metrics based on various electrical characteristics of CG HD-GC JAM MOSFET has been compared with CG GC JAM and CG JAM MOSFET for various control and screen gate length. Hence, the accuracy of the model was verified with numerical simulation data from COGENDA™

Chapter-4 presents a 2-D DC compact model for device potential, electric field, threshold voltage, roll-off, DIBL, SS, complete drain current including GIDL, transconductance and output conductance engineered JAM MOSFET. A device considering various reported device engineering is named CG-SHD-GC-DM JAM MOSFET. 2-D Poisson's equation considering both depletion and accumulation charges has been solved by the superposition principle using appropriate boundary conditions. The model thus formulated is continuous across various operating regimes (both depletion and accumulation). Effects of quantum and electrical confinements have been implemented in the proposed model. The effects of device temperature and interface trapped charges have also been applied in the formulated. Threshold voltage has been formulated by taking depletion approximation of the original potential equation by utilizing the minimum central channel potential principle. Drain current has been formulated in the same way as chapter-3. The performance metrics based on various electrical characteristics of engineered CG SHD-GC-DM JAM MOSFET have been compared with CG JAM MOSFET. Finally, the modeled results have been matched with numerical simulation data from COGENDA™ to verify the accuracy of the model.

Chapter-5 presents a unified 2-D model for device potential, threshold voltage, roll-off, DIBL, drain current, transconductance and output conductance CG JAM and IM MOSFET. The 2-D Poisson's equation considering both depletion and accumulation charges has been solved by the superposition principle using appropriate boundary conditions. The potential thus formulated is continuous across all operating regimes (depletion and accumulation regimes). The 1-D potential equation considered here is simpler and consists of a single equation as compared to the three components used in chapter-4. Threshold voltage has been formulated using the minimum central potential principle. The quasi-ballistic drain current has been modeled by utilizing Lundstrom's theory. The mean free carrier path and ballistic velocity have been extracted from the simulation to obtain the ballistic coefficient. The drain current considered here is continuous across all operating regimes as compared to drain current formulation in chapters 2-4. Finally, the modeled results have been verified with numerical simulation data from COGENDA^{TM}

Chapter-6 presents DC and RF analysis of vertically stacked high-*k*/SiO_2 CG JAM MOSFET with vertical Gaussian doping. DC analysis consists of threshold voltage, I_{ON}/I_{OFF} ratio, transconductance, output-conductance and intrinsic gain whereas RF analysis consists of capacitances, GBW, f_T, f_{max}, TFP and transit time. Further, a lookup table-based Verilog-A model has been created using the DC and RF analysis results from COGENDA^{TM}. The Verilog-A model is then used to simulate a CMOS inverter and a 6-T SRAM cell in CADENCE^{TM} platform. Thereafter various parameters such as SNM, gain, delay, short circuit power dissapation, RNM, WNM, N-curve analysis, RAT and WAT have been extracted from the simulated results.

Chapter-7 includes the summary and conclusions of this thesis. Some possible future scopes of research in the related area of the present thesis are also presented at the end of this chapter.