3

CHAPTER

QUASI-Z-SOURCE SERIES-PARALLEL MULTI-OUTPUT INVERTERS TOPOLOGIES FOR THREE-PHASE MICROGRID APPLICATIONS

3.1 Introduction

In the previous chapter, single-phase multi output quasi-Z-source based inverters have been proposed, which can be operated in series and parallel mode. These inverters have the ability to produce multiple single-phase AC outputs simultaneously, which can cater more than one load demands at a time without using any extra adopter or regulator in microgrid applications. However, they have certain limitations such as they cannot serve the three-phase (3-Φ) load applications as they can produce only single-phase AC outputs. Moreover, they are suitable only for low power applications and not for high power applications. Therefore, to overcome these problems, three-phase quasi-z-source series-parallel multi-output (QSPMO) inverter topologies for three-phase microgrid applications and three-phase residential load are proposed in this chapter. The detailed mathematical modelling, analysis of steady-state and dynamic behaviour and switching stress analysis are carried out. The closed loop operations of the proposed topologies are also performed in this chapter. The experimental results of 240 W lab prototypes are presented to validate the proposed three-phase *q*-ZS series-parallel multi-output inverter topologies. The next subsection contains a full description of the proposed inverters.

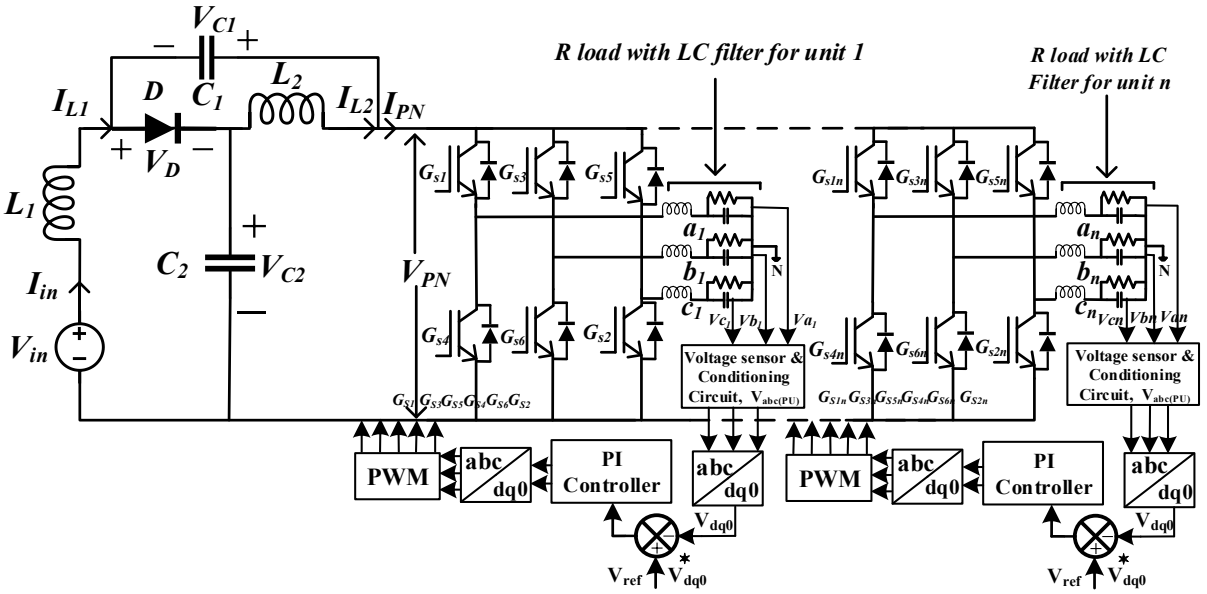
3.2 Three-Phase QSPMO Inverter Topologies with Regulated Multiple AC Outputs for Microgrid Applications and Residential Loads

This chapter proposes two three-phase QSPMO inverter topologies with controlled multiple AC outputs for three-phase microgrid applications and domestic loads. The proposed topologies are extension of the inverters proposed in the previous chapter and are developed from *q*-ZS inverter by replacing its main switch with the *n*-number series and parallel connected three-phase inverters. In the parallel mode, the topology yields *n*-number of parallel three phase AC outputs with different voltages and currents for different load conditions. For the series mode, topology yields *n*-number of three-phase series AC outputs constant load currents.

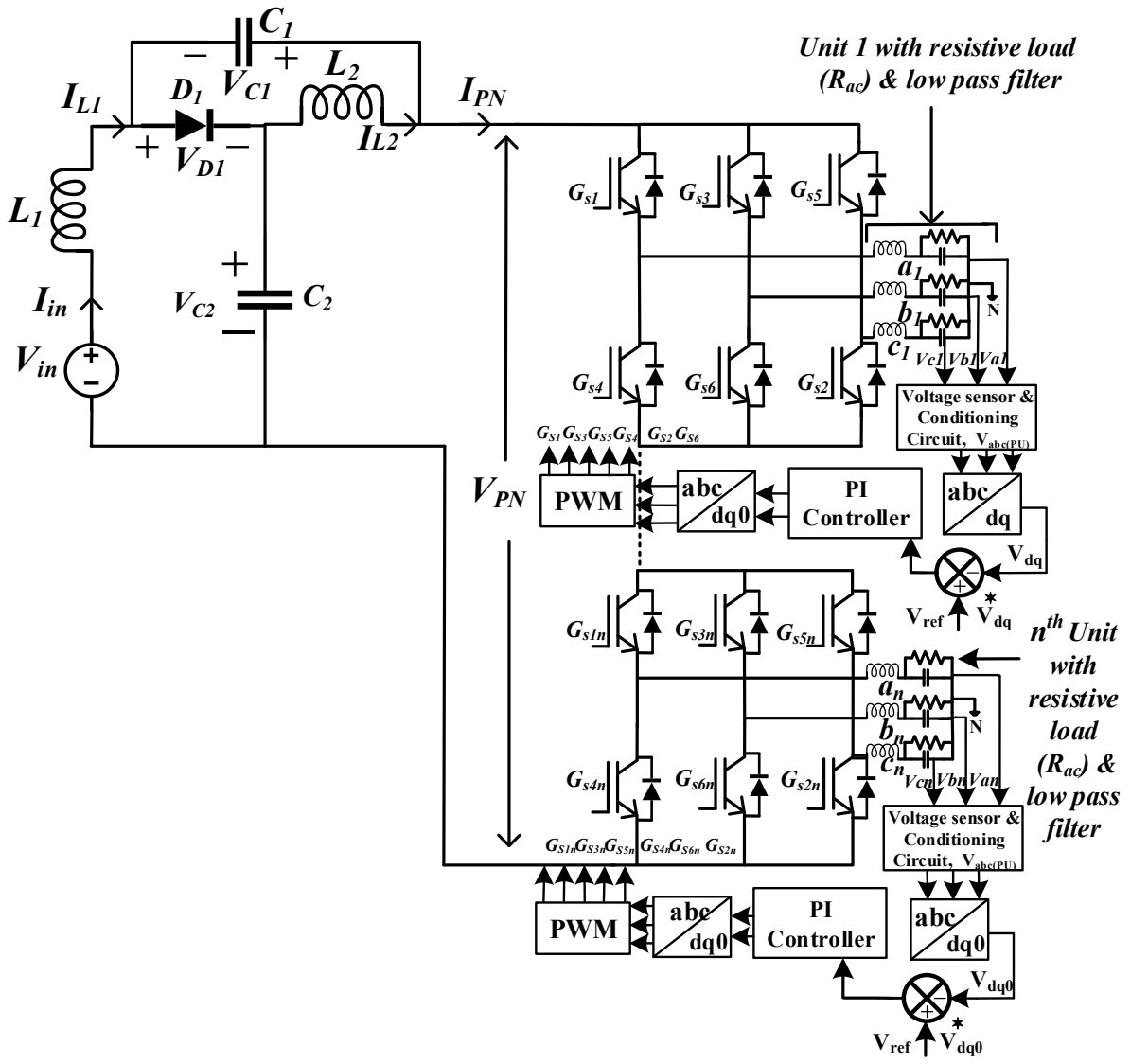
Unlike the voltage source derived multi-output inverters, the proposed inverters have all inherent properties of q-ZSI, like providing both buck–boost operations and protection in the condition of shoot-through. For generating switching signals in these inverters, sinusoidal pulse width modulation (SPWM) with constant frequency shoot-through (CFST) is used. The proposed topologies fulfil more than one three phase load demands simultaneously without any extra adaptor or regulator. In this chapter, the closed-loop control for proposed three-phase topologies have been implemented for two series/parallel 3-Φ output units, which are capable of supplying two 3-Φ AC outputs simultaneously. The same logic and analysis will be valid for *n* numbers of series/parallel output units.

3.2.1 Proposed Three-Phase QSPMO Inverters' Circuits

Figures 3.1(a) and (b) show the proposed three-phase QSPMO inverter circuits with parallel and series modes, respectively. In this work, the proposed topologies of three-phase QSPMO inverters are analysed and validated for two AC outputs (n = 2). The same methodology can be used to design the proposed inverters for more than 2 units.



(a)



(b)

Figure 3.1: Proposed 3-Φ QSPMO inverters' circuit (a) Proposed parallel mode and (b) Proposed series mode 3-Φ QSPMO inverters.

3.2.2 Operational Analysis of the Proposed Inverters

The proposed 3-Φ QSPMO inverters are operated in two different intervals; 1) shoot-through (ST) interval and 2) power interval. The switching period is assumed to be T, the power interval and shoot-through interval are T_1 and T_0, respectively. The detailed analysis for two inverter units (n = 2) are discussed in the following subsections.

3.2.2.1 Shoot-Through Interval

Figures 3.2(a) and (b) show the operation of proposed multi-output inverters and their equivalent circuits during the ST interval for the parallel and series mode connections,

respectively. From Figures 3.2(a) and (b), it may be noticed that during the ST period, the switches of the same leg conduct simultaneously and the diode *D* is reverse biased. In order to describe the circuit behaviour, the circuit is simplified by replacing the inverters by one switch and the equivalent circuit is shown in Figure 3.2(c). The impedance source network inductors L_1 and L_2 store energy and the capacitors C_1 and C_2 are discharged. In this interval, the switch-node voltage V_{PN} of the proposed 3-Φ QSPMO inverters is equal to zero. In ST interval, the governing equations are as follows:

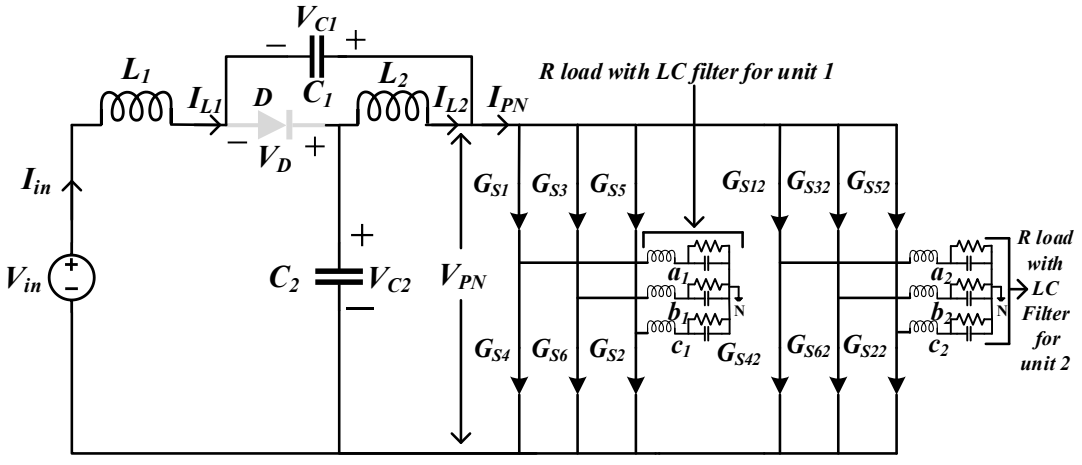
$$L_1 \frac{dI_{L1}}{dt} = V_{in} + V_{c1} \tag{3.1}$$

$$L_2 \frac{dI_{L2}}{dt} = V_{c2} \tag{3.2}$$

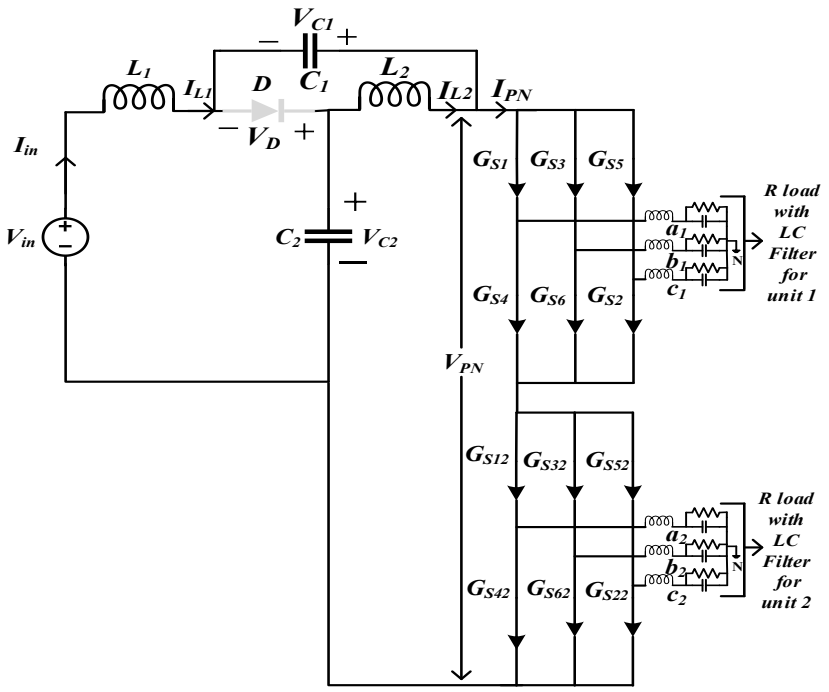
$$C_1 \frac{dV_{c1}}{dt} = -I_{L1} \tag{3.3}$$

$$C_2 \frac{dV_{c2}}{dt} = -I_{L2} \tag{3.4}$$

$$V_{PN} = 0 \tag{3.5}$$



(a)



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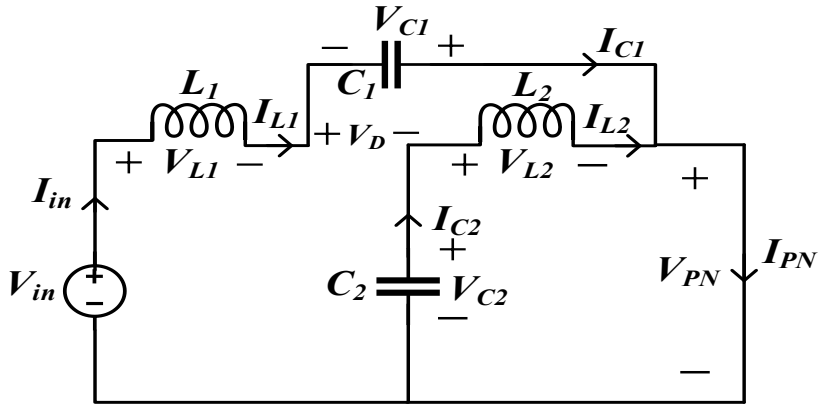


(c)

Figure 3.2: Proposed 3-Φ QSPMO inverters during the shoot-through interval (a) Proposed parallel mode inverter during the shoot-through interval, (b) proposed series mode inverter during the shoot-through interval, and (c) equivalent circuit during shoot-through interval.

3.2.2.2 Power Interval

Figure 3.3(a) and (b) show the operation of proposed multi-output inverter and their equivalent circuits during the PT for the parallel and series mode connections, respectively [86]-[90]. From Figure 3.3(a) and (b), it may be noticed that during power interval, the switches of the different legs conduct simultaneously ensuring power flow from source to load, and the diode D is forward biased. In order to describe the circuit behaviour, the circuit is simplified

by representing the inverter units with an inverted current source (I_{PN}). This inverted current source (I_{PN}) has potential difference V_{PN} as shown in Figure 3.3(c). As per the shown direction of the current source and the potential difference, the power is absorbed by the current source, which is equal to the power delivered to the actual load. The inductors L_1 and L_2 release energy and capacitors C_1 and C_2 get charged. In this state, switch-node voltage V_{PN} of the proposed 3-Φ QSPMO inverters is non-zero and it acts as the input to the inverter units. In the PT, the governing equations are as follows:

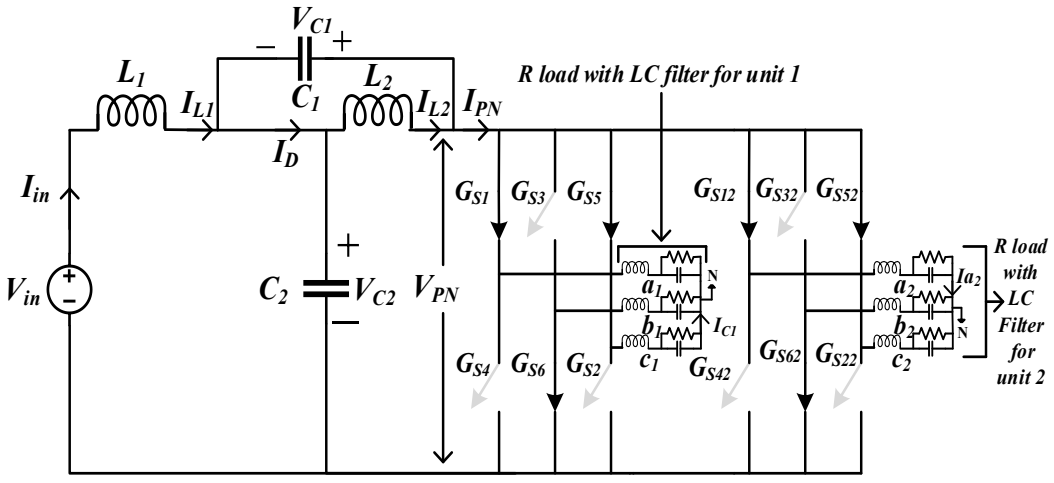
$$L_1 \frac{dI_{L1}}{dt} = V_{in} - V_{c2} \tag{3.6}$$

$$L_2 \frac{dI_{L2}}{dt} = -V_{C1} \tag{3.7}$$

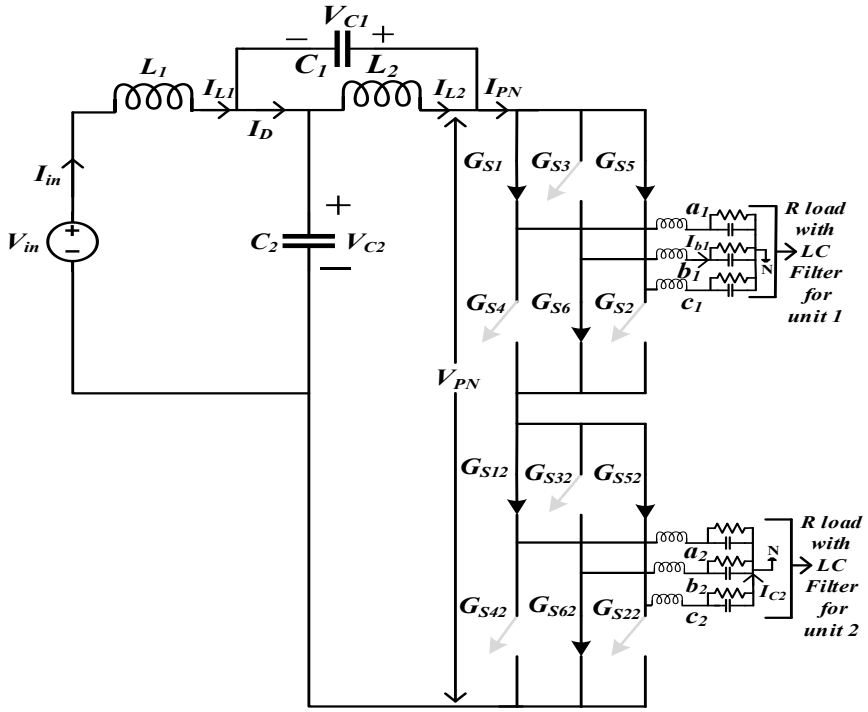
$$C_1 \frac{dV_{c1}}{dt} = I_{L2} - I_{pn} \tag{3.8}$$

$$C_2 \frac{dV_{c2}}{dt} = I_{L1} - I_{pn} \tag{3.9}$$

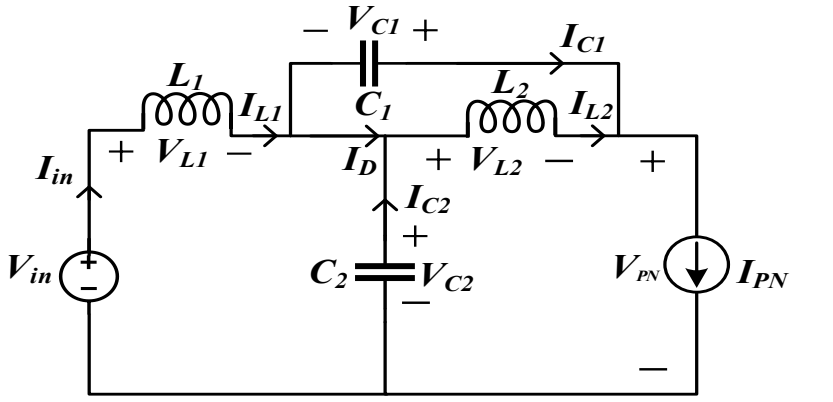
$$V_{PN} = V_{c1} + V_{c2} \tag{3.10}$$



(a)



(b)



(c)

Figure 3.3: Proposed 3-Φ QSPMO inverters during the power interval (a) Proposed parallel mode inverter during the power interval, (b) proposed series mode inverter during the power interval, and (c) equivalent circuit during power interval.

From (3.1-3.2) and (3.6-3.7), the following equations are obtained using volt-second balance on inductors L_1 and L_2.

$$V_{L1} = \overline{v_{L1}} = \frac{T_0(V_{in}+V_{c1})+T_1(V_{in}-V_{c2})}{T} = 0 \tag{3.11}$$

$$V_{L2} = \overline{v_{L2}} = \frac{T_0 V_{C2}-T_1 V_{C1}}{T} = 0 \tag{3.12}$$

On solving the above, the following is obtained.

$$V_{C1} = \frac{D}{1-2D}V_{in};\ V_{C2} = \frac{1-D}{1-2D}V_{in};\ V_{PN} = \frac{1}{1-2D}V_{in} \tag{3.13}$$

Similarly, the following can be obtained from (3.3-3.4) and (3.8-3.9) using the Charge balance on capacitors C_1 and C_2.

$$I_{C1} = \overline{i_{C1}} = \frac{T_0(-I_{L1})+T_1(I_{L2}-I_{PN})}{T} = 0; \tag{3.14}$$

$$I_{C2} = \overline{i_{C2}} = \frac{T_0(-I_{L2})+T_1(I_{L1}-I_{PN})}{T} = 0 \tag{3.15}$$

Solving the (3.15), the following is obtained.

$$I_{L1} = \frac{(1-D)}{(1-2D)} I_{PN}\,;\; I_{L2} = \frac{(1-D)}{(1-2D)} I_{PN} \tag{3.16}$$

The inverter's peak switch node voltage V_{PN} can be expressed as follows

$$\hat{V}_{\mathrm{PN}} = \frac{1}{1-2D} V_{in} = BV_{in} \tag{3.17}$$

where B is the boost factor of the proposed 3-Φ QSPMO inverters.

The peak value of the fundamental component of AC output is given by

$$\widehat{(v_{AC})}_{fundamental} = \hat{v}_0 = \frac{M}{2} V'_{PN} = \frac{M}{2}\left(\frac{1}{1-2D}\right) V_{in} \tag{3.18}$$

where $V'_{\mathrm{PN}} = V_{\mathrm{PN}}$ for parallel mode, $V'_{\mathrm{PN}} = V_{\mathrm{PN}}/2$ for series mode and M is the modulation index.

$$\frac{\widehat{(v_{AC})}_{fundamental}}{V_{in}} = G\;; \quad G = \frac{M}{2}\left(\frac{1}{1-2D}\right) \tag{3.19}$$

3.2.3 Variation of AC Gain and Boost Factor with Respect to Modulation Index and Shoot-Through Duty Cycle

Figure 3.4 shows the graphical representation of variation of different voltage gains with respect to modulation index (M), boost factor (B) and ST duty cycle (D). The gain produced by the proposed inverters are same as of traditional ZSIs. This gain G of the inverter can be varied by varying D. Figure 3.4(a) depicts the graph showing variation of ratio of output AC voltage and switch node voltage with respect to M. As the M increases, the AC gain (G) of the proposed inverters also increases linearly, which can be verified by (3.19). Variation in B with respect to D is shown in Figure 3.4(b). As the D increases, the B also increases in hyperbolic manner and finally become infinite at $D = 0.5$, which can be verified from (3.17). A graphical 3-dimension representation of variation of the ratio G of output AC voltage V_{AC} and input DC voltage V_{in},

with respect to D and M are shown in Figure 3.4(c). Figure 3.4(d) shows the operating region of the proposed inverters.

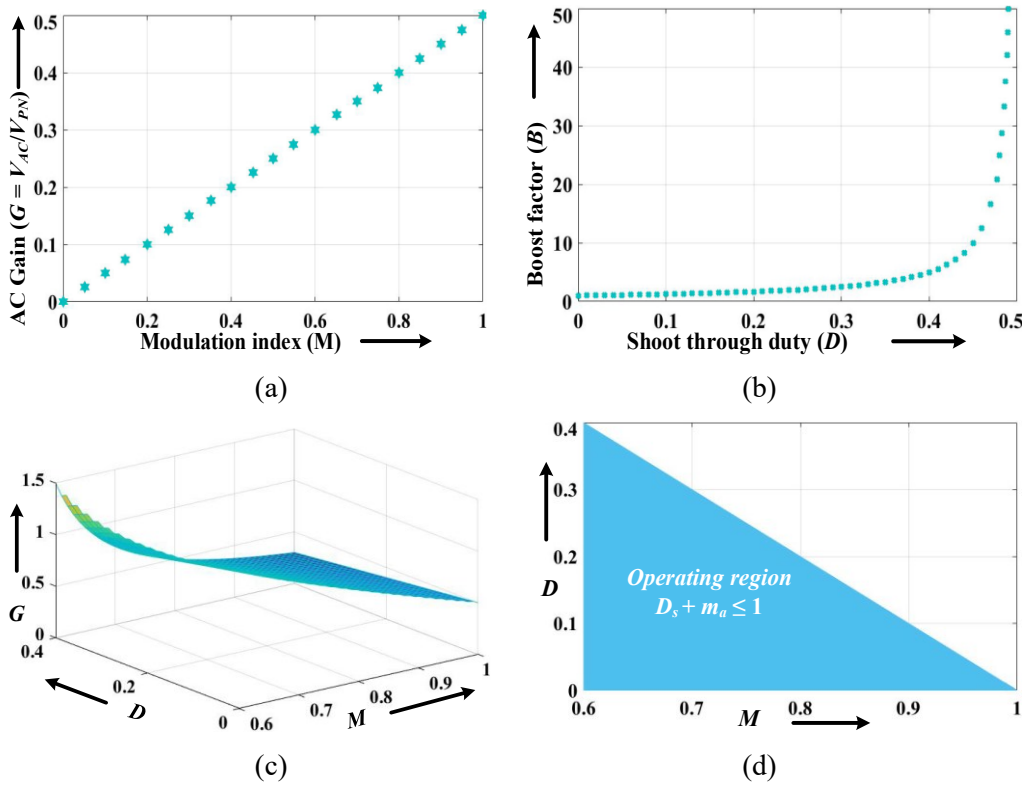


Figure 3.4: (a) Variation of AC gain w.r.t. M, (b) plot between B and D, (c) 3D plot and (d) Operating region of the proposed inverters.

3.3 AC Power Expression for the Proposed 3-Φ Inverters

The AC power expression for the proposed multi-output inverters (n = 2) with parallel and series mode of operations is given in the following subsections. The following constraint for SPWM with shoot-through states for the proposed inverters is as follows:

$$D + M \leq 1 \tag{3.20}$$

3.3.1 Parallel Mode Operation of the Proposed Topology

In this mode of operation, the switch node voltages of inverter units 1 and 2 (V_{PN1} and V_{PN2}) are the same (V_{PN}) as the inverter units are connected in parallel. The peak AC voltages ($\hat{v}_{01}$ and $\hat{v}_{02}$) are equal for the same reference voltages (V_{ref}) and balanced AC loads. The peak AC voltages ($\hat{v}_{01}$ and $\hat{v}_{02}$) are different for different reference voltages (V_{ref}) of the inverter

units. Here, the reference voltage (V_{ref}) for inverters units is the required peak AC output voltage ($\hat{v}_0$). For the same reference voltage (V_{ref}), the $\hat{v}_{01}$ and $\hat{v}_{02}$ are given by

$$\hat{v}_{01} = \hat{v}_{02} = \frac{M}{2} V_{PN} = \frac{M}{2}\left(\frac{1}{1-2D}\right) V_{in} \tag{3.21}$$

The ratio of peak AC voltage and input voltage (V_{in}) can be written as

$$\left(\frac{\widehat{(v}_{AC})_{fundamental}}{V_{in}}\right) = \left(\frac{\hat{v}_0}{V_{in}}\right) = G = \frac{M}{2}\left(\frac{1}{1-2D}\right) \tag{3.22}$$

The expression of rms AC output voltage gain (G_{AC}) is given by

$$G_{AC} = \frac{V_{o,rms}}{V_{in}} = \frac{M}{2\sqrt{2}}\left(\frac{1}{1-2D}\right) \tag{3.23}$$

The rms AC output voltage ($V_{o,rms}$) is given as

$$V_{o,rms} = \frac{M}{2\sqrt{2}}\left(\frac{1}{1-2D}\right)\ V_{in} \tag{3.24}$$

The three-phase AC power output ($P_{3-\emptyset}$) of both the inverters units at the same V_{ref} is given as

$$P_{(3-\emptyset)} = 6\,\frac{V_o^2{}_{,rms}}{R} = 6\,\frac{M^2\,B^2\,V^2{}_{in}}{8\,R} \tag{3.25}$$

Similarly, the three-phase AC power output (P_0) of both the inverter units at different V_{ref} is given as

$$P_0 = 3\,\frac{(M^2{}_1 + M^2{}_2\ )B^2\ V^2{}_{in}}{8\,R}, \quad \left(B = \frac{1}{1-2D}\right) \tag{3.26}$$

where M_1 and M_2 are the modulation indices of inverter units 1 and 2 respectively and B is the boost factor. From (3.25) and (3.26), it is clear that $P_{3-\emptyset}$ depends on M and D.

3.3.2 Series Mode Operation of the Proposed Topology

In this mode of operation, the switch node voltage (V_{PN}) is equally divided across the inverter bridges for balanced AC load and the peak AC voltages ($\hat{v}_{01}$) and ($\hat{v}_{02}$) are equal for the same voltage reference.

$$\hat{v}_{01} = \hat{v}_{02} = \frac{M}{2}\frac{V_{PN}}{2} = \frac{M}{4}\left(\frac{1}{1-2D}\right) V_{in} \tag{3.27}$$

The ratio of peak AC voltage and V_{in} can be written as

$$\left(\frac{\widehat{(v_{AC})}_{fundamental}}{V_{in}}\right) = \left(\frac{\hat{v}_0}{V_{in}}\right) = G_{AC} = \frac{M}{4}\left(\frac{1}{1-2D}\right) \tag{3.28}$$

The rms AC output voltage gain (G_{AC}) is given as

$$G_{AC} = \frac{M}{4\sqrt{2}}\left(\frac{1}{1-2D}\right) \tag{3.29}$$

The rms AC output voltage ($V_{o,rms}$) is given as

$$V_{o,rms} = \frac{\hat{v}_0}{\sqrt{2}} = \frac{M}{4\sqrt{2}}\left(\frac{1}{1-2D}\right) V_{in} \tag{3.30}$$

The three-phase AC power output $P_{(3-\emptyset)}$ of a single unit is given as

$$P_{(3-\emptyset)} = 3\frac{V_{o,rms}^2}{R} = 3\frac{M^2 B^2 V^2 in}{32 R}, \quad \left(B = \frac{1}{1-2D}\right) \tag{3.31}$$

The three-phase AC power output (P_0) of both units is given as

$$P_0 = 6\frac{V_{o,rms}^2}{R} = 6\frac{M^2 B^2 V^2 in}{32 R}, \quad \left(B = \frac{1}{1-2D}\right) \tag{3.32}$$

From (3.32), it is clear that the $P_{(3-\emptyset)}$ depends on M and D. The voltage $\hat{v}_0$ is directly proportional to the modulation index of the inverter unit. Therefore, as the V_{ref} is increased, the M increases, due to which output power increases and vice versa.

In this way, using the series and parallel connection of n-number of three-phase qZSIs, the topology is able to give multiple AC outputs with boost capability. Any disturbance in the input voltage or load parameter can easily be taken care of using a feedback control loop. Consequently, the voltage output becomes smooth and constant in nature. Therefore, the power from the proposed inverters can easily be injected into the AC microgrid and simultaneously can be used for residential three-phase loads.

3.4 Switching Stress of the Proposed 3-Φ QSPMO Inverters

The stress analysis of each front end component of the circuit is similar as the stress analysis presented in the previous chapter. The voltage stresses and current stresses in context with the proposed inverters are represented in the Table 3.1 and Table 3.2, respectively. In case of parallel mode topology, if the number of inverter units are increased then the overall

output power of the proposed inverters increases. Therefore, to meet the output power, input current ($I_{in} = I_{L1} = I_{L1}$) increases, and thus, the current stresses on inductors increase with increased no of output units. However, in case of series mode as the no of output unit increases, voltage stresses on capacitors C_1 and C_2 are increased.

TABLE 3.1

VOLTAGE STRESS OF EACH COMPONENTS IN DIFFERENT INTERVALS

Components	ST interval	Power interval
L_1	$\frac{(1-D)\,V_{in}}{(1-2D)}$	$\frac{(-D)\,V_{in}}{(1-2D)}$
L_2	$\frac{(1-D)\,V_{in}}{(1-2D)}$	$\frac{(-D)\,V_{in}}{(1-2D)}$
C_1	$\frac{(D)\,V_{in}}{(1-2D)}$	$\frac{(D)\,V_{in}}{(1-2D)}$
C_2	$\frac{(1-D)\,V_{in}}{(1-2D)}$	$\frac{(1-D)\,V_{in}}{(1-2D)}$
D	$\frac{(D)\,V_{in}}{(1-2D)}$	0
V_{PN}	0	$\frac{(D)\,V_{in}}{(1-2D)}$

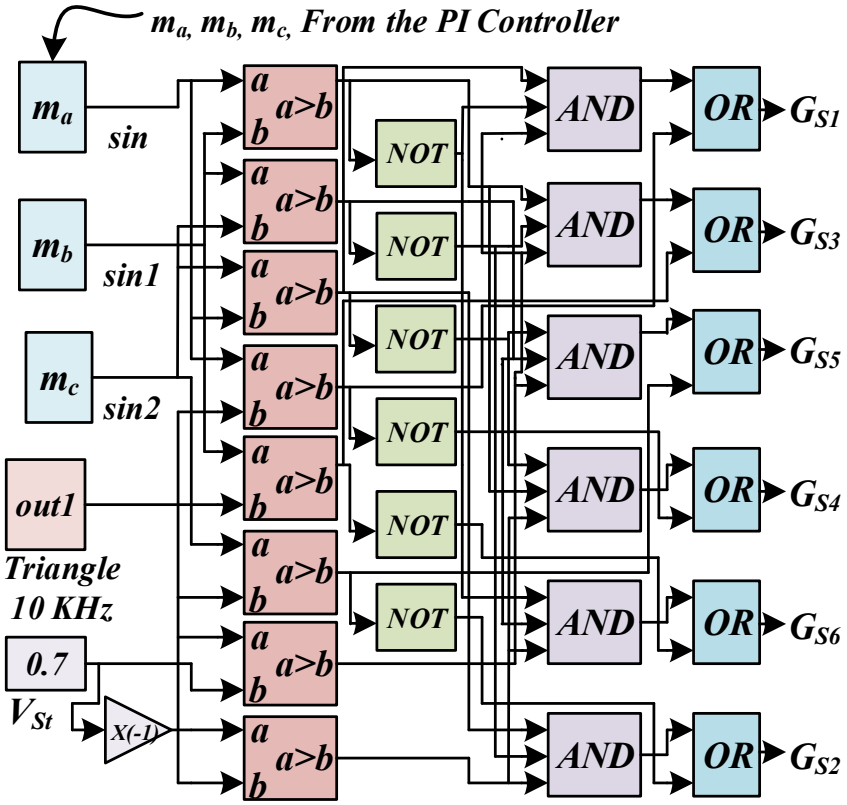
TABLE 3.2

CURRENT STRESS OF EACH COMPONENTS IN DIFFERENT INTERVALS

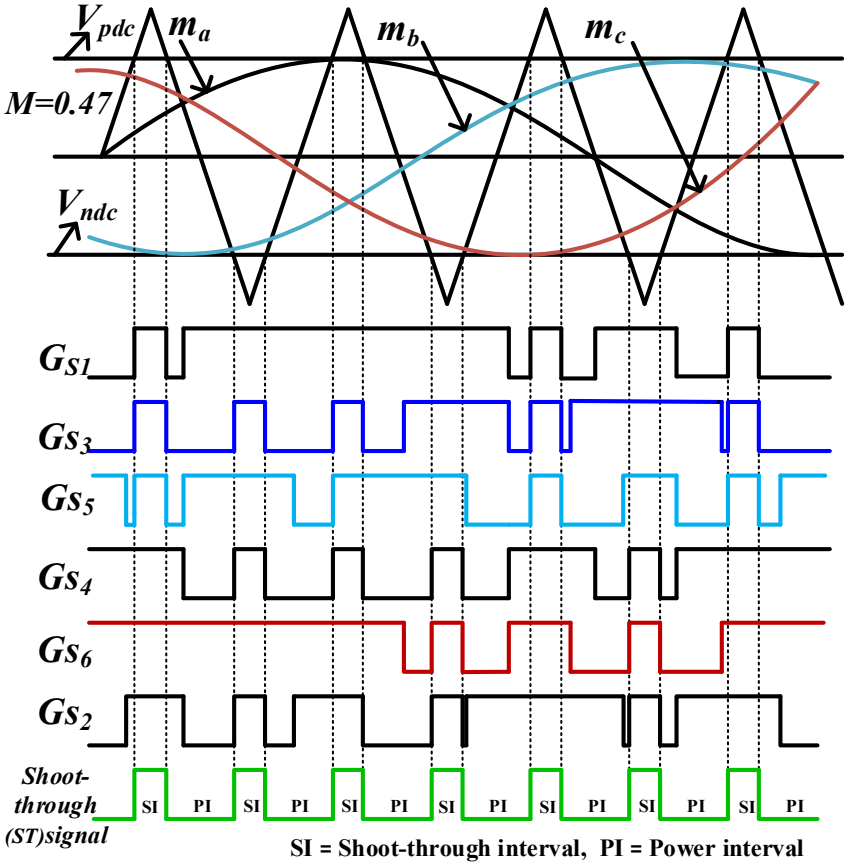
Components	ST interval	Power interval
L_1	I_{in}	I_{in}
L_2	$\frac{-(1-D)\,I_{pn}}{(1-2D)}$	$\frac{(1-D)\,I_{pn}}{(1-2D)}$
C_1	$\frac{-(1-D)\,I_{pn}}{(1-2D)}$	$\frac{(D)\,I_{pn}}{(1-2D)}$
C_2	$\frac{-(1-D)\,I_{pn}}{(1-2D)}$	$\frac{(D)\,I_{pn}}{(1-2D)}$
D	0	$\frac{I_{pn}}{(1-2D)}$

3.5 Pulse Width Modulation for the Proposed Inverters

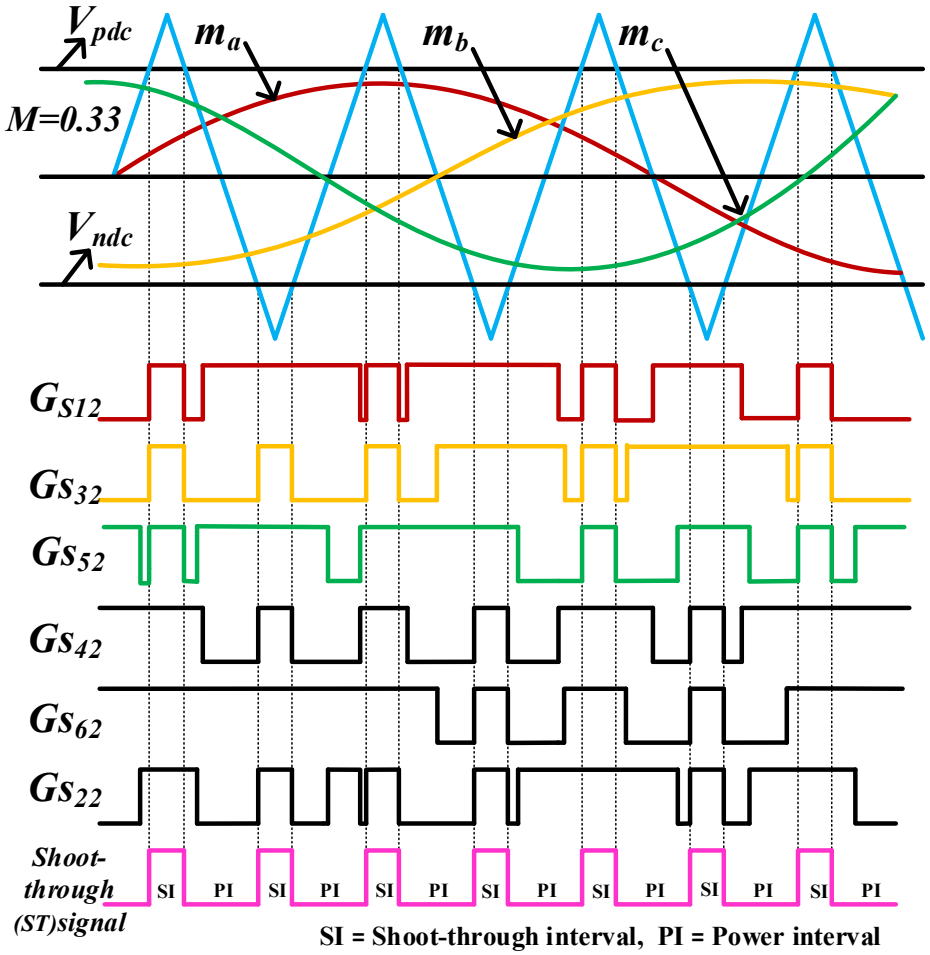
To operate the proposed inverters, the modulation technique is implemented using a digital signal processor (DSP) (TI-TMS320F28335) [91]-[96]. The modulation scheme of the proposed topology with switching signals are shown in Figure 3.5. The block diagram logic for generating pulses is shown in Figure 3.5(a). The waveforms related to SPWM and corresponding switching signals are shown in Figures 3.6(b) and (c) for units 1 for V_{ref} = 35 V and 2 for V_{ref} = 25 V, respectively. The corresponding value of M is 0.47 and 0.33 for unit 1 and unit 2, respectively. The value of D = 0.3 for $\hat{V}_{PN}$= 150V and input voltage 60 V. The modulating signals for units 1 and 2 are different according to V_{ref} of the two units. However, the ST signals are same for both the units (D =0.3) to maintain V_{PN} constant at input of both the output units. In Figure 3.5(b), the signals G_{s1} to G_{s6} are switching signals for switch 1 to switch 6 respectively for unit 1. The proposed inverters are similar to a normal voltage source inverter during the power interval and the switching signals in power interval and the switching signals in that power interval are generated by comparing three phase modulating signals (m_a, m_b, m_c) with triangular carrier wave. To generate ST state signals, the carrier wave is compared with the two constant *dc* signals (positive V_{pdc} and negative V_{ndc}). The ST signals are produced for all the switches of the inverters, if the carrier wave is greater than the positive constant *dc* signal V_{pdc} or less than the negative *dc* signal V_{ndc}. The switching signals of the unit 2 are generated in the same way and shown in Figure 3.5 (c).


m_a, m_b, m_c, From the PI Controller
m_a
sin
m_b
sin1
m_c
sin2
out1
Triangle
10 KHz
0.7
V_{St}
X(-1)
a
b
a>b
NOT
AND
OR
G_{S1}
G_{S3}
G_{S5}
G_{S4}
G_{S6}
G_{S2}

(a)


V_{pdc}
m_a
m_b
m_c
M=0.47
V_{ndc}
G_{S1}
G_{S3}
G_{S5}
G_{S4}
G_{S6}
G_{S2}
Shoot-through (ST)signal
SI
PI
SI = Shoot-through interval, PI = Power interval

(b)



(c)

Figure 3.5: Modulation scheme for proposed three-phase inverters (a) Control logic diagram, (b) PWM pulses of inverter unit 1 with V_{ref} = 35 V (M = 0.47), (c) PWM pulses of inverter unit 2 with V_{ref} = 25 V (M = 0.33).

3.6 Controller for the Proposed QSPMO Topologies

Figure 3.6 shows the block diagram of the control scheme for the proposed 3-Φ QSPMO inverter topologies. The three-phase output voltages (v_a, v_b and c_c) of the proposed topologies are sensed and transformed into *dq* components (V_d, V_q) using Park's transformation and compared with references voltages $V_{d(ref)}$ and $V_{q(ref)}$. Then the error signal is fed to PI compensator. The required modulated signal is obtained from the PI controller ($m_{d(req)}$, $m_{q(req)}$). Further $m_{d(req)}$ and $m_{q(req)}$ are converted into modulating signals m_a, m_b and m_c using inverse Park's transformation. By comparing modulating signals with the triangular carrier waveform along with positive *dc* voltage (V_{pdc}) and negative dc voltage (V_{ndc}) for ST, switching pulses are generated and fed to the inverter switches.

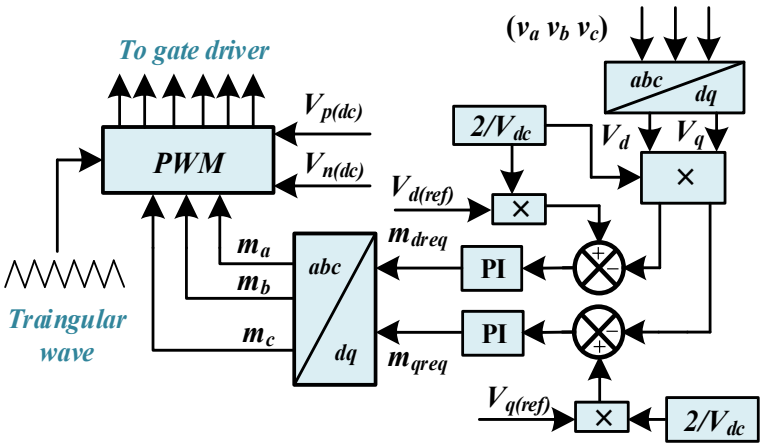


Figure 3.6: Block diagram of control scheme for the proposed 3-Φ QSPMO inverters.

3.7 Experimental Verification of the Proposed Topologies

The performance of the proposed 3-Φ QSPMO inverter topologies for two simultaneous AC outputs (n = 2) is validated through experimental results. Figure 3.7 depicts the overall implementation of the proposed concept. A DSP board (TI-TMS320F28335) is used to generate the pulses for the proposed inverters. For experimental validation, a 240 W laboratory prototype for parallel and series mode was fabricated in the laboratory. The parameters of the whole system are listed in Table 3.3. A detailed discussion of steady state and dynamic results of the proposed parallel and series mode 3-Φ QSPMO inverter are given in subsequent subsections. Figure 3.8 depicts the proposed inverters' experimental setup.

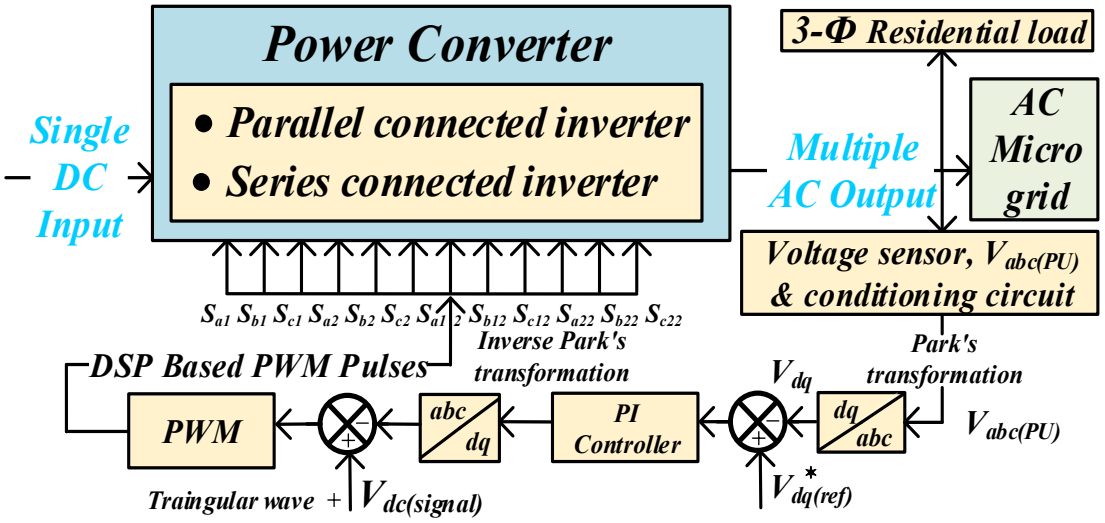


Figure 3.7: Overall implementation of proposed 3-Φ QSPMO inverter topologies.

TABLE 3.3

LIST OF THE PARAMETERS WITH THEIR VALUES

PARAMETER	VALUES
Inductor	$L_1 = L_2 = 1.5$ mH
Capacitance	$C_1 = C_2 = 470$ uF
Carrier frequency	$f_s = 10$ kHz
Fundamental frequency	50 Hz
Filter inductor	2 mH
Filter capacitor	10 uF
COMPONENTS	**MANUFACTURER**
Inverter switches	IRFP260N (I.R.Corp.)
Diode	RURG5060 (Fairchild)
Gate drivers	FOD3184 (Fairchild)
Voltage transducer	LEM LV25-P (Mouser.in)
DSP (TI-TMS320F28335)	Texas instrument

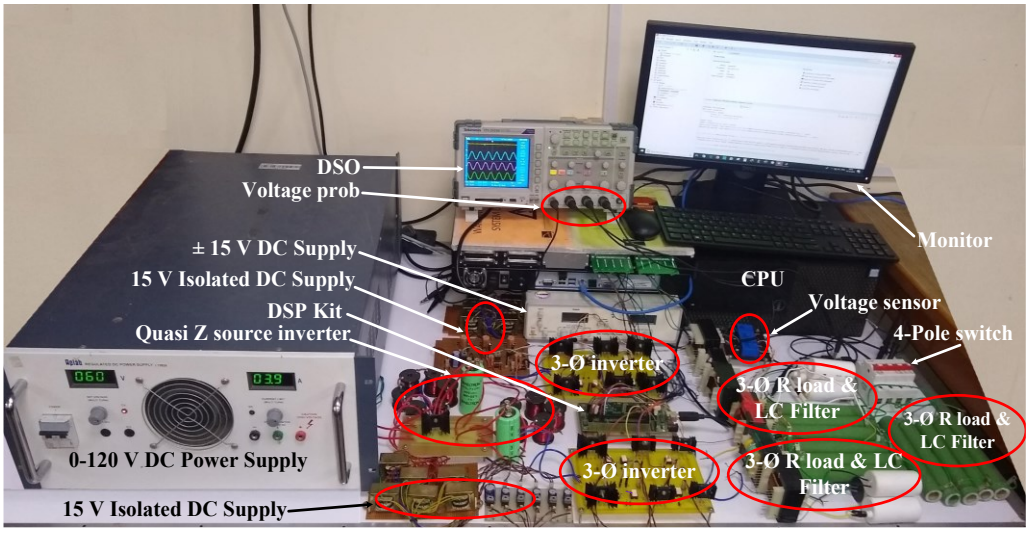


Figure 3.8: Photograph of the experimental prototype.

3.8 Parallel Mode of the Proposed Inverters

The proposed 3-Φ QSPMO inverters is operated in parallel mode for 240 W application with input voltage (V_{in}) 60 V and $D = 0.3$ for both the inverter units.

3.8.1 Steady-State Response of Proposed Parallel Mode Inverters with Equal Reference Voltages

Figure 3.9(a) shows the input voltage (V_{in}), the voltage across capacitor C_1 (V_{C1}= 45 V), the voltage across the capacitor C_2 (V_{c1}=105 V) and the voltage waveforms across the diode (V_D =150 V) of the proposed 3-Φ QSPMO inverters. The values of V_{c1} and V_{c2} are equal to the theoretical values calculated using (3.13). It is observed that the diode is forward biased during power interval thus the voltage across the diode is zero. Further, in ST interval, diode is reverse biased and thus the voltage across the diode is negative. Figure 3.9(b) shows the input voltage (V_{in}), switch node voltages of inverter units 1 and 2 (V_{PN1} and V_{PN2} = 150 V), which are equal

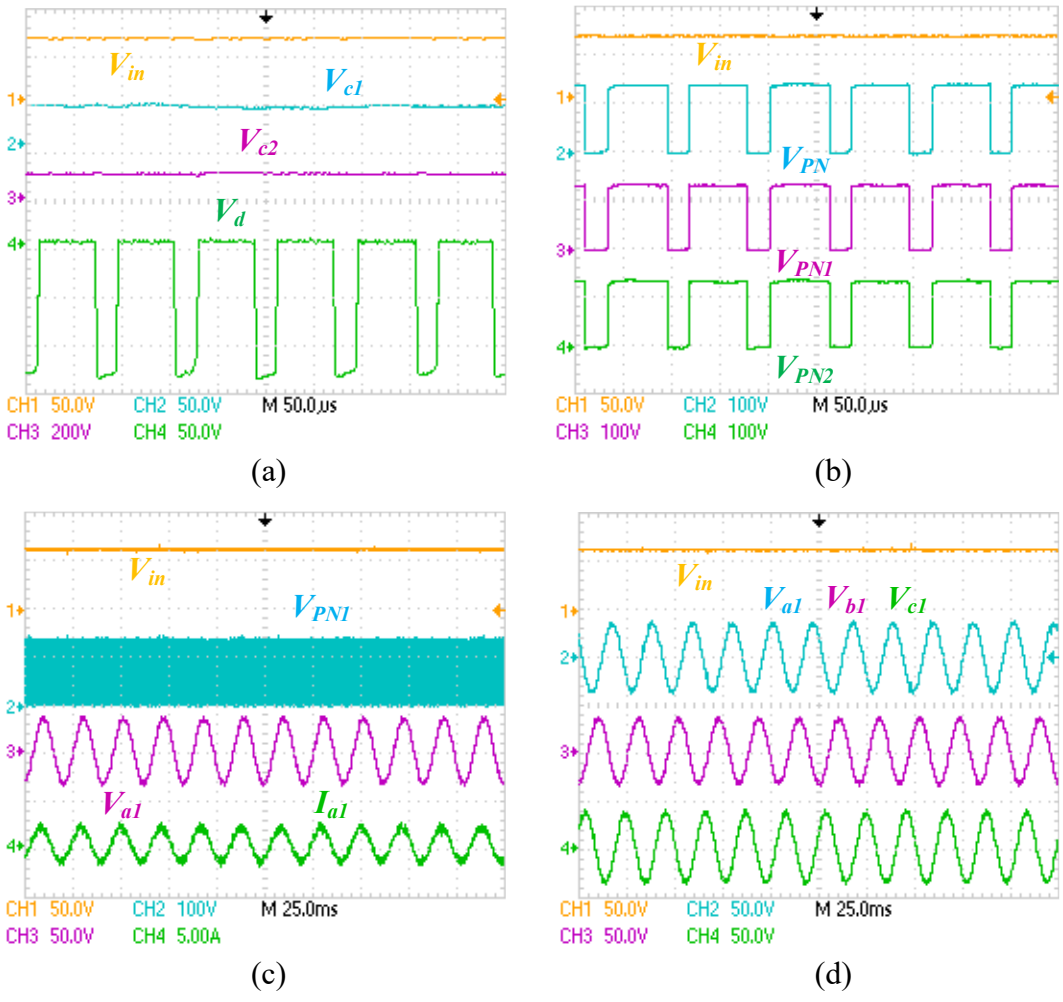
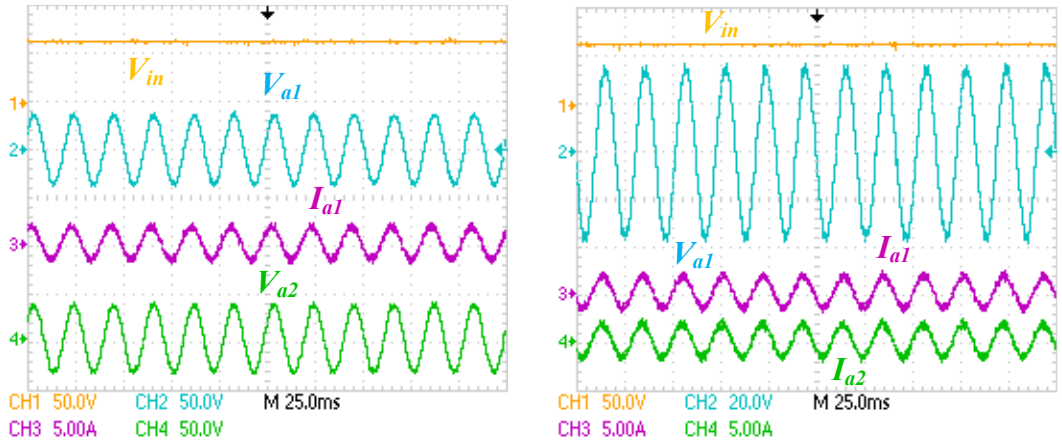


Figure 3.9: Steady-state response of proposed topology during parallel mode operation for equal V_{ref} for both units, (a) Input voltage V_{in}, capacitor voltage V_{c1}, V_{c2} and voltage switching waveform of diode (V_d), (b) V_{in}, V_{PN}, V_{PN1} (switch node voltage across Inverter unit 1) and V_{PN2}, (c) V_{in}, V_{PN1}, V_{a1} (phase voltage) and I_{a1} (phase current of inverter unit 1), (d) V_{in}, three-phase voltages of inverter unit 1.

to V_{PN} as the inverter units are connected in parallel. Figure 3.9(c) shows the input voltage (V_{in}), switch node voltages (V_{PN}) and voltage and current of phase *a* of inverter unit 1 which is equal to the theoretical value. With reference voltage (V_{ref}) of 35 V, voltage of the phase *a* is 70 V (peak-peak) and current is 3.5 A (peak-peak) with a load resistance of 20 Ω per phase. Figure 3.9(d) shows V_{in} = 60 V and three-phases output voltages of inverter unit 170 V (peak-peak), while the reference voltage (V_{ref}) is at 35 V. All the three-phases are 120^0 apart from each other having same magnitude (70 V peak-peak). This indicates that the system is balanced and stable.

Figure 3.10 shows the behaviour of two inverter units for same AC reference voltage, V_{ref} = 35 V (AC peak) for both the units. Figure 3.10(a) depicts V_{in} = 60 V, output voltage 70 V (peak-peak) and current 3.5 A (peak-peak) of phase *a* for inverter unit 1, and output voltage 70 V (peak-peak) of phase *a* for inverter unit 2. The reference peak AC voltage is at 35 V. It is also clear that the phase voltage of inverter 1 and 2 have the same magnitude and phase angle. Figure 3.10(b) shows the input voltage, phase *a* voltage, phase *a* current of inverter unit 1 and output current of phase *a* of unit 2 with reference voltage of 35 V. It can be seen that the phase current of unit 1 and current of unit 2 are same. It indicates that both unit are stable, balanced with same reference voltage.

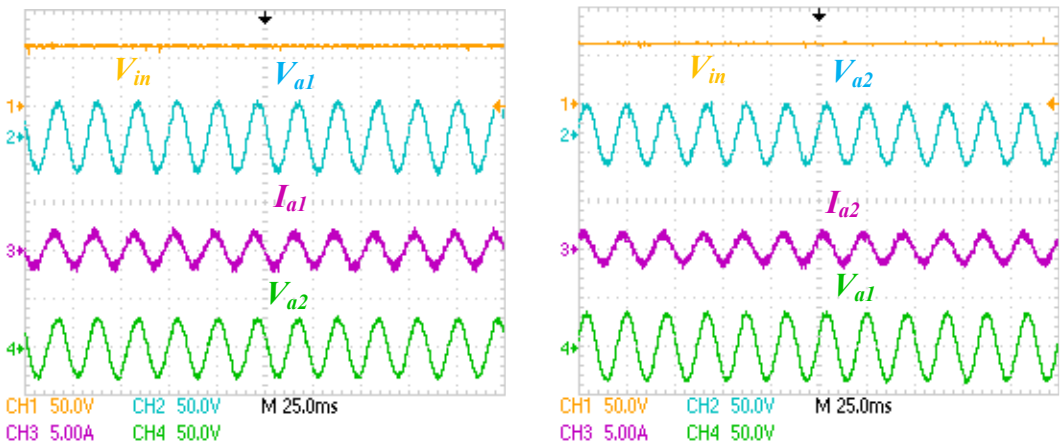


(a) (b)

Figure 3.10: Steady-state Response of proposed topology during parallel operation with phase voltage and current (a) V_{in}, phase voltage and current (V_{a1} and I_{a1}) of unit 1, phase voltage (V_{a2}) of unit 2, (b) V_{in}, V_{a1}, I_{a1} of unit 1, I_{a2} of unit 2.

3.8.2 Steady-State Response of Proposed Parallel Mode Inverter with Different Reference Voltages

Figure 3.11 shows the performance of the two inverter units for different AC peak reference voltages, V_{ref1} = 35 V and V_{ref2} = 30 V. Figure 3.11(a) shows that V_{in} = 60 V, output voltage (V_{a1}) = 70 V (peak-peak), phase *a* current (I_{a1}) = 3.5 A (peak-peak) of unit 1 and output voltage (V_{a2}) = 60 V (peak-peak) of unit 2. The V_{ref} is at 35 V and 30 V for units 1 and 2, respectively. Figure 3.11(b) shows V_{a2} = 60 V (peak-peak), I_{a2} = 3 A (peak-peak) of unit 2 and V_{a1} = 70 V (peak-peak) of unit 1. Thus, it is clear that the two units are stable and the three-phase AC outputs are balanced and magnitudes corresponding to the reference voltages.



(a) (b)

Figure 3.11: Steady-state Response of proposed topology during parallel operation with phase voltage and current at different V_{ref}, (a) V_{in}, V_{a1}, I_{a1} of unit 1 at V_{ref} = 35 V, V_{a2} of unit 2 at V_{ref} = 30 V, (b) V_{in}, V_{a2}, I_{a2} of unit 2 at V_{ref} = 30 V, V_{a1} of unit 1 at V_{ref} = 35 V.

3.8.3 PWM Signals of the Proposed Parallel Mode Inverters with Equal Reference

Figures 3.12(a) and (b) show the PWM pulses of upper side and lower side switches of inverter unit 1. Figures 3.12(c) and (d) show the PWM pulses of the upper side and lower side switches of inverter unit 2.

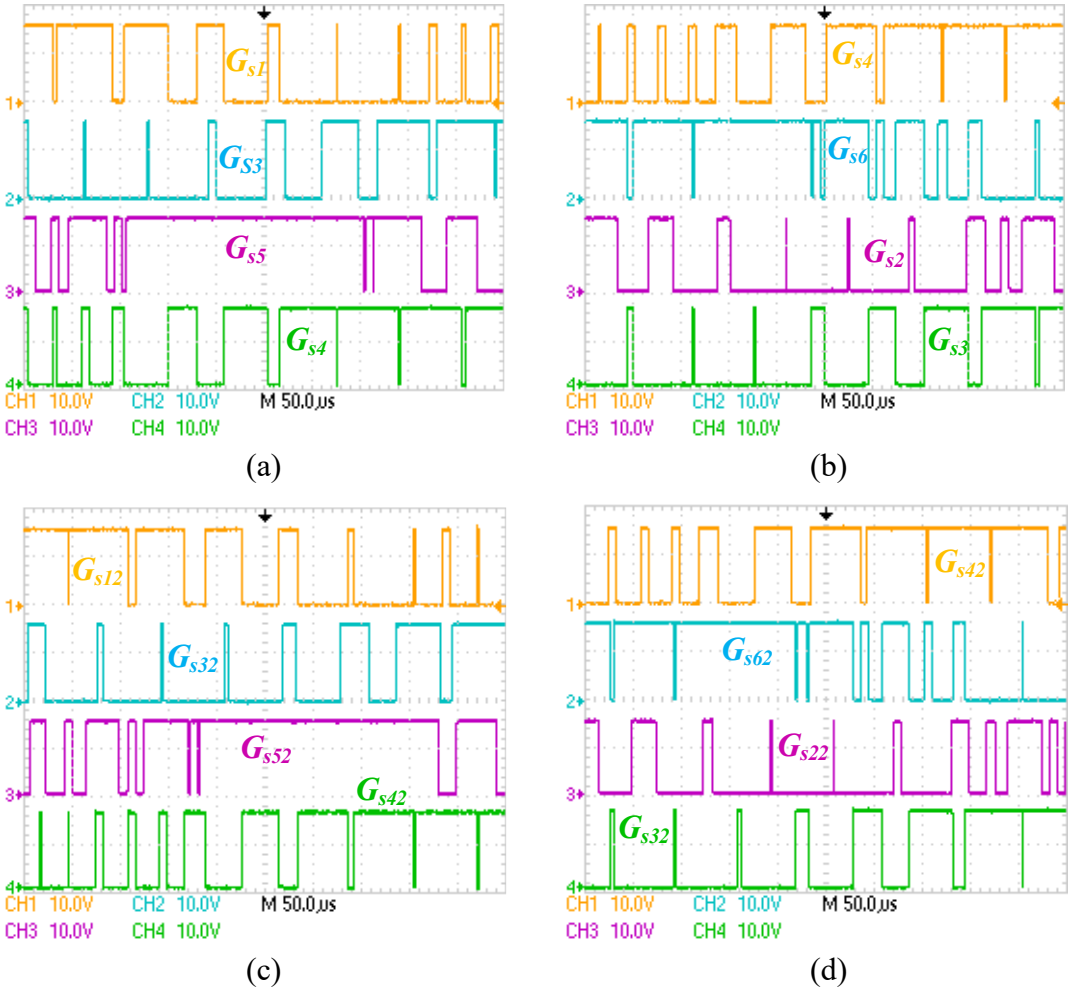
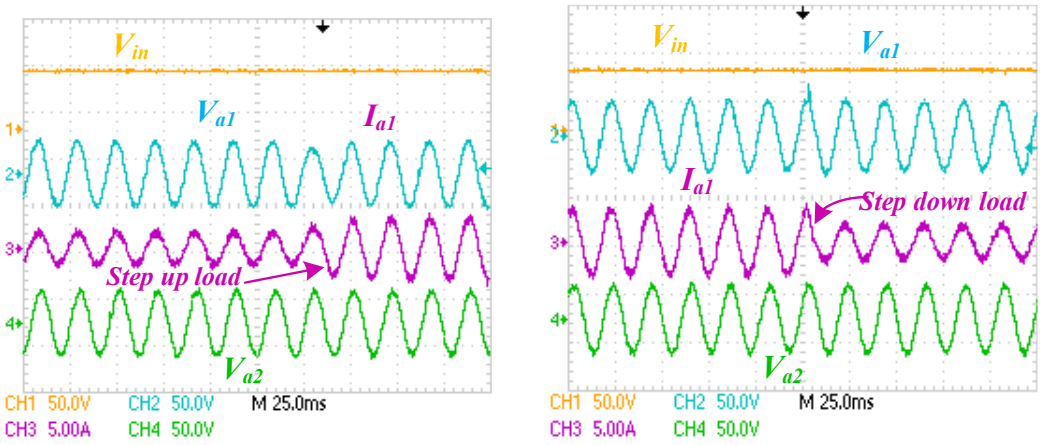


Figure 3.12: PWM pulses of proposed topology during parallel operation (a) PWM pulses of upper switches and G_{s4} of inverter unit 1, (b) PWM pulses of lower switches and G_{s3} of inverter unit 1, (c) PWM pulses of upper switches and G_{s42} of inverter unit 2 and, (d) PWM pulses of lower switches and G_{s32} of inverter unit 2.

3.8.4 Dynamic Response of Proposed Parallel Mode Inverters with the Same Reference Voltages

Figure 3.13 shows the dynamic response of the proposed topology at the same V_{ref} = 35 V for both units with change in load resistance in unit 1. In Figure 3.13(a), it is changed from 20 Ω to 10 Ω and the corresponding load current increases from 3.5 A (peak-peak) to 7 A (peak-peak). As the load current increases, the phase *a* voltage of unit 1 (V_{a1}) slightly decreases and then restores to its original position in a short time (in one cycle). It indicates that the proposed topology is stable and has good dynamic response. The phase *a* voltage of unit 2 (V_{a2}) remains constant at V_{ref} = 35 V. Similarly, Figure 3.13(b) shows the step-down load change at

same V_{ref} = 35 V. As the load resistance changes from 10 to 20 Ω of unit 1, the current decreases from 7 to 3.5 A (peak-peak). A transient for very small (negligible) period appears in phase voltage of unit 1, whereas the phase voltages of units 2 remain unaffected.



(a) (b)

Figure 3.13: Dynamic response of proposed topology during parallel operation at same reference voltages with load change in unit 1 (a) and (b) Step-up and Step-down dynamics with unit 2 at V_{ref} = 35 V.

Figure 3.14 shows the dynamic behaviour with load change in both the units with V_{ref} = 35 V for both the units. Figures 3.14(a) and (b) show I_{a2} of unit 2, which remains unaffected during the change in phase current (I_{a1}) of unit 1 for step-up and step-down load change of unit 1. This show the decoupled behaviour of the two units. In Figure 3.14(c), load current of unit 2 increases from 3.5 to 7 A (peak-peak) as the load is changed from 20 to 10 Ω. V_{a1} of unit 1 remains unaffected during this load change. The phase voltage of unit 2 slightly decreases but it restores within one cycle. Similarly, Figure 3.14(d) shows V_{in}, V_{a1} of both the units and phase *a* current of unit 2 for step-down load change in unit 2. The current decreases from 7 to 3.5 A (peak-peak) as the corresponding load resistance is changed from 10 Ω to 20 Ω. In this case, the AC voltage outputs of units 1 and 2 remain unaltered. This indicates the good dynamic behaviour and stable closed-loop operation of the proposed topology.

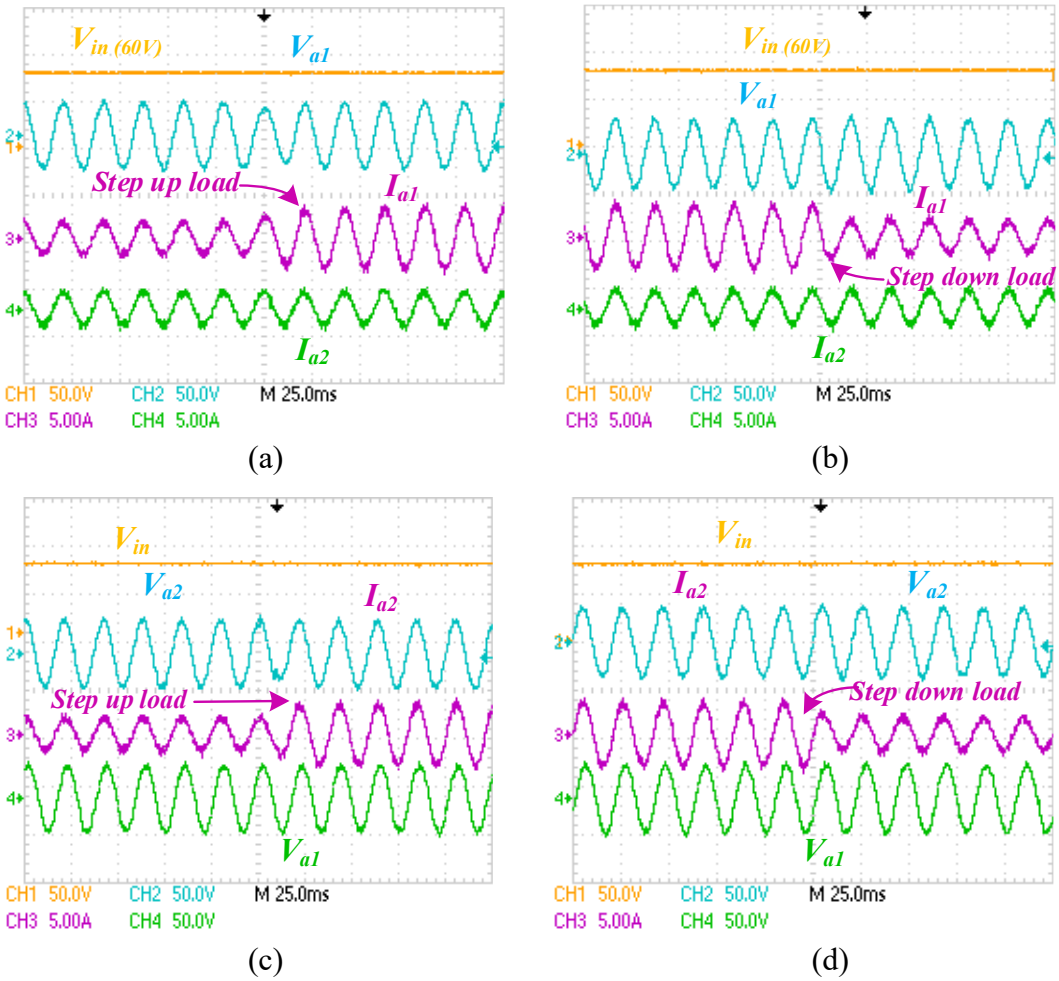
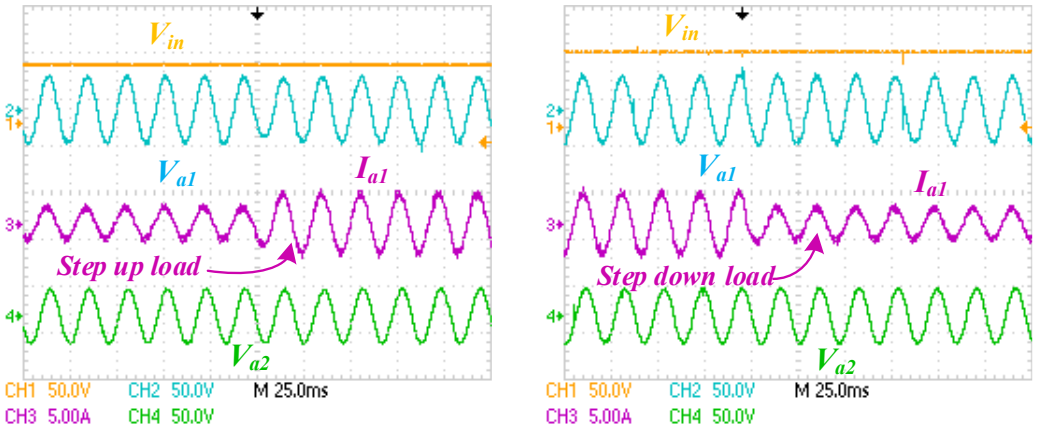


Figure 3.14: Dynamic response of proposed topology during parallel operation at same reference voltages with load change, (a) and (b) I_{a2} of unit 2 with Step-up and Step down load dynamics in unit 1 at V_{ref} = 35 V, (c) V_{in}, V_{a2}, I_{a2} of inverter unit 2 and V_{a1} of inverter unit 1 at V_{ref} = 35 V with step up load change in unit 2, (d) V_{in}, V_{a2}, I_{a2} of inverter unit 2 and I_{a1} of inverter unit 1 at V_{ref} = 35V with step down load change in unit 2.

3.8.5 Dynamic Response of Proposed Parallel Mode Inverters with Different Reference Voltages

Figures 3.15 and 3.16 show the dynamic response of proposed parallel mode topology when both the units have different reference voltages, V_{ref} = 35 V for unit 1 and V_{ref} = 30 V for unit 2. Figures 3.15(a) and (b) show V_{in}, V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) for step-up and step-down of load in unit 1. In Figure 3.15(a), current increases from 3.5 A to 7 A (peak-peak) for load resistance change from 20 Ω to 10 Ω. In Figure 3.15(b), current decreases from 7 A to 3.5 A (peak-peak) as the load resistance is changed from 10 Ω to 20 Ω but V_{a2} remains constant at 60 V (peak-peak). The voltage of other unit changes slightly for

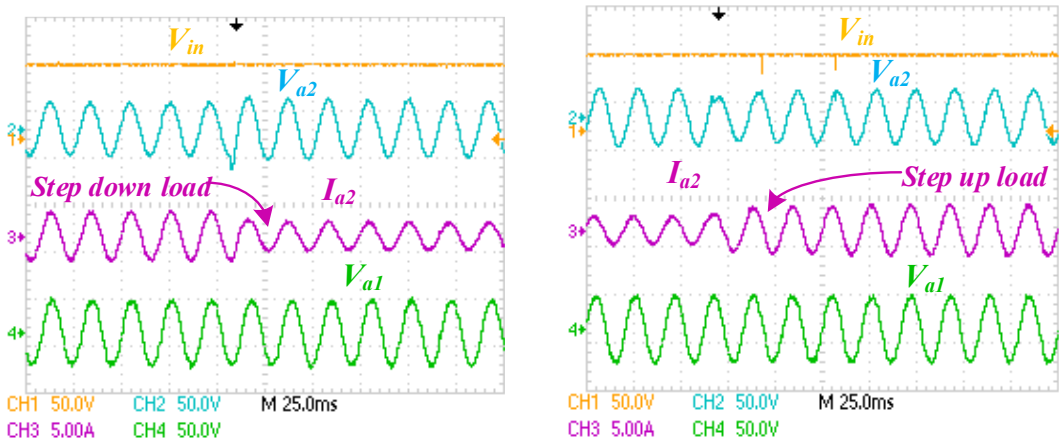
very small period and it restores within one cycle. This ensures good dynamic response of the system.



(a) (b)

Figure 3.15: Dynamic response of proposed topology during parallel operation at different reference voltage with load change in unit 1 (a) and (b) Step up and step down dynamics while inverter unit 1 is at $V_{ref=}$ 35V and unit 2 at $V_{ref=}$ 30V.

Figures 3.16(a) and (b) show the dynamics with same step-down and step-up load change in unit 2. In Figure 3.16(a), the load resistance of unit 2 is increased from 10 to 20 Ω and in Figure 3.16(b), the load resistance is decreased from 20 to 10 Ω. For load change in unit 2, the voltages of the other unit (unit 1) remains unchanged. The voltages of unit 2 slightly changes but restores within one cycle. This shows the good dynamic response of the system with different voltage references for two units.

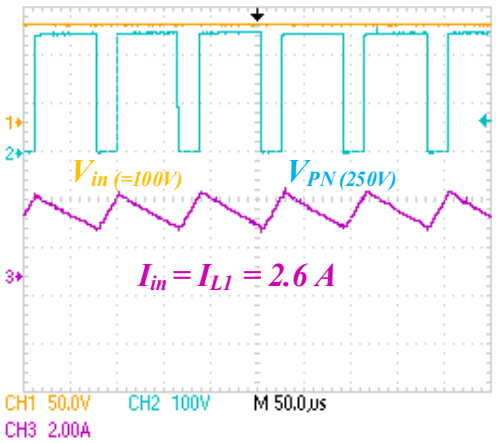


(a) (b)

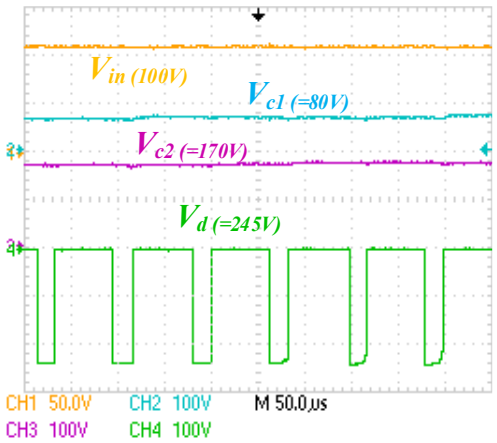
Figure 3.16: Step up and step down dynamic response of proposed parallel mode inverter with different reference voltages, (a) and (b) Step down and Step up dynamics with V_{ref} of inverter unit 1 at 30 V and unit 2 at 35V, respectively.

3.9 Series Mode of the Proposed Inverters

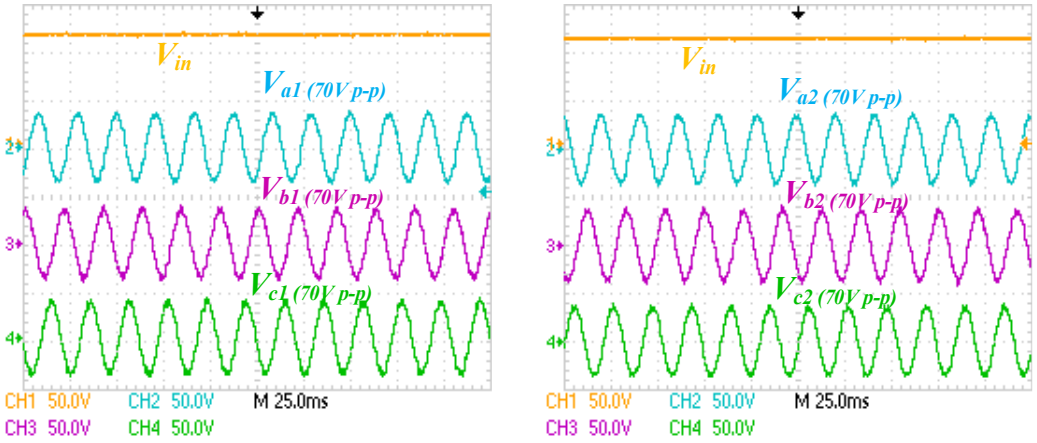
The proposed series mode 3-Φ QSPMO inverters is operated with V_{in} = 100 V and D = 0.3. The reference voltages (V_{ref}) for both the inverter units is 35 V. The responses for the proposed topology are shown in Figure 3.17. Figure 3.17(a) shows the input voltage (V_{in} = 100 V), switch node voltage (V_{PN} = 250 V) and inductor current (I_{L1} = 2.6 A) which is equal to the input current (I_{in}). During the ST interval, all the switches of the inverters' legs are ON at the same time. Therefore, the switch node voltage V_{PN} = 0 V and inductors L_1 and L_2 store the energy. However, during power interval, inductors L_1 and L_2 release the energy and switch node voltage becomes V_{PN} = 250 V. Figure 3.17(b) shows input voltage, voltage across capacitor C_1 (V_{c1}), voltage across C_2 (V_{c2}) and diode voltage (V_D = 250 V) in the impedance network of the proposed inverters. The value of V_{c1} = 75 V and V_{c2} = 175 V are same as the theoretical values obtained from (3.13). It can be observed that the diode is forward biased during the power interval and reverse biased during the ST interval. Figures 3.17(c) and (d) show input voltage and phase voltages of all three-phases of inverter units 1 and 2, respectively. The magnitude of all the three voltages are 70 V (peak-peak), which is equal to the theoretical values.



(a)



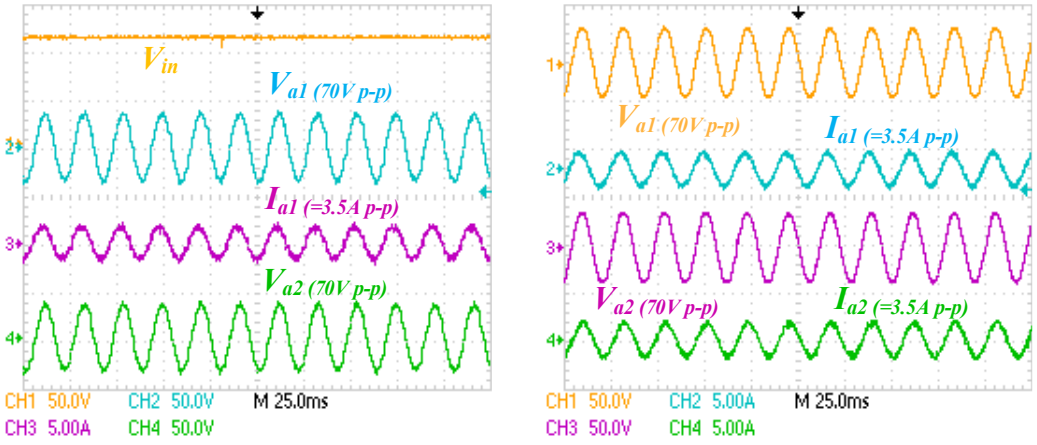
(b)



(c) (d)

Figure 3.17: Steady-state response of proposed topology during series operation (a) V_{in}, switch node voltage (V_{PN}) and inductor current I_{L1}, (b) V_{in}, capacitor voltage V_{c1} and V_{c2} and voltage switching waveform of the diode (V_d), (c) and (d) V_{in}, three-phase voltages of inverter unit 1 and 2 at V_{ref} = 35 V.

Figure 3.18(a) shows input voltage, phase *a* voltage, phase *a* current of inverter unit 1 and phase *a* voltage of unit 2. The peak-peak phase voltage of both units is 70 V and current is 3.5 A (peak-peak), which is equal to their theoretical counterparts. Figure 3.18(b) shows the phase *a* voltage, phase *a* current of units 1 and 2. Phase voltage (V_{a1}), phase current (I_{a1}) of unit 1 and V_{a2}, I_{a2} of unit 2 have same amplitude and phase angle. Therefore, the power of unit 1 and 2 are equal.

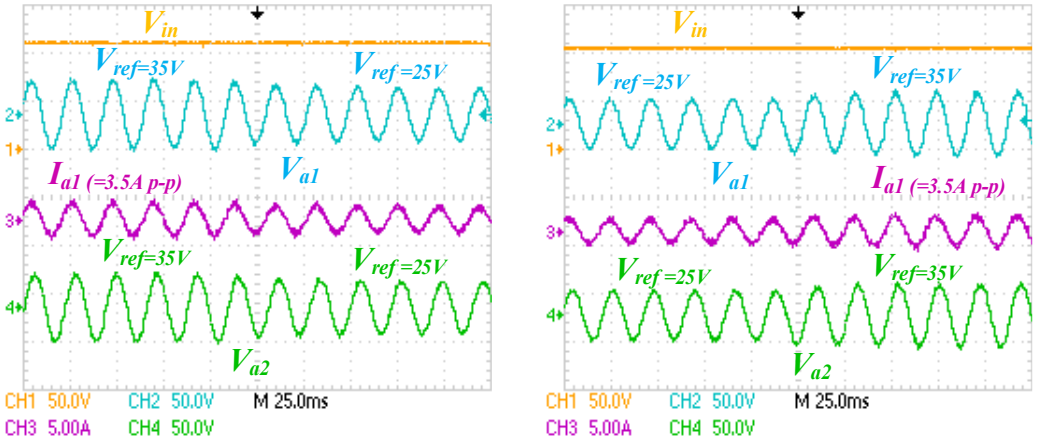


(a) (b)

Figure 3.18: Steady-state response of proposed topology during series operation (a) V_{in}, V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) and V_{a2} (phase voltage of inverter unit 2), (b) V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) and V_{a2} (phase voltage) I_{a2} (phase current of inverter unit 2) at V_{ref} = 35 V.

3.9.1 Dynamic Response of Proposed Series Mode Inverters

Figure 3.19 shows the dynamic behaviour during series operation with input voltage V_{in} = 100 V, load resistance = 20 Ω and D = 0.3, where reference voltage (V_{ref}) of both the units are varied. Figure 3.19(a) shows the response, when V_{ref} is decreased from 35 to 25 V. The peak-peak voltages of phase *a* of both the units change from 70 to 50 V, consequently the phase *a* peak-peak current changes from 3.5 to 2.5 A. Similarly, Figure 3.19(b) shows the response, where V_{ref} is increased from 25 to 35 V. The phase voltages of both the units track the reference voltage and becomes equal to 35 V and the current becomes 3.5 A accordingly. The system settles to new reference value in a short time (within two cycles), showing good dynamic behaviour of the series mode proposed inverter with closed loop control.



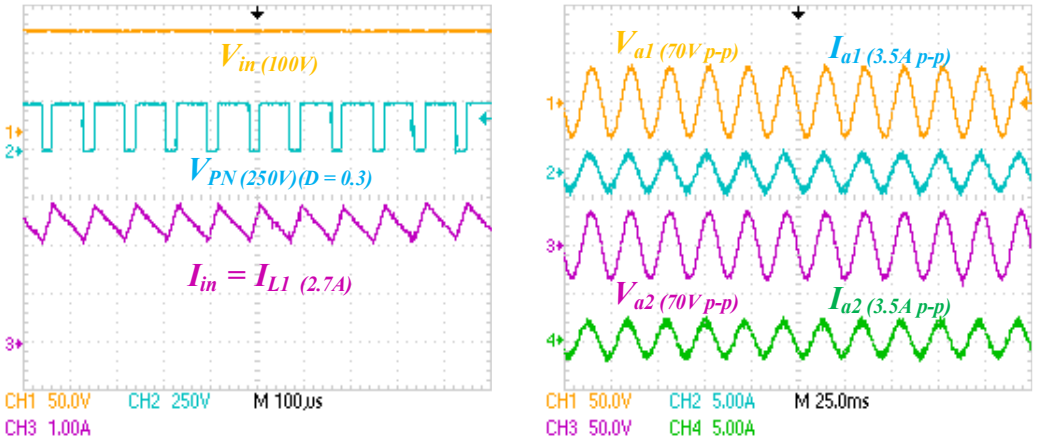
(a) (b)

Figure 3.19: Dynamic response of proposed series mode inverters, (a) and (b) dynamics during series operation for increase and decrease in voltage reference, respectively.

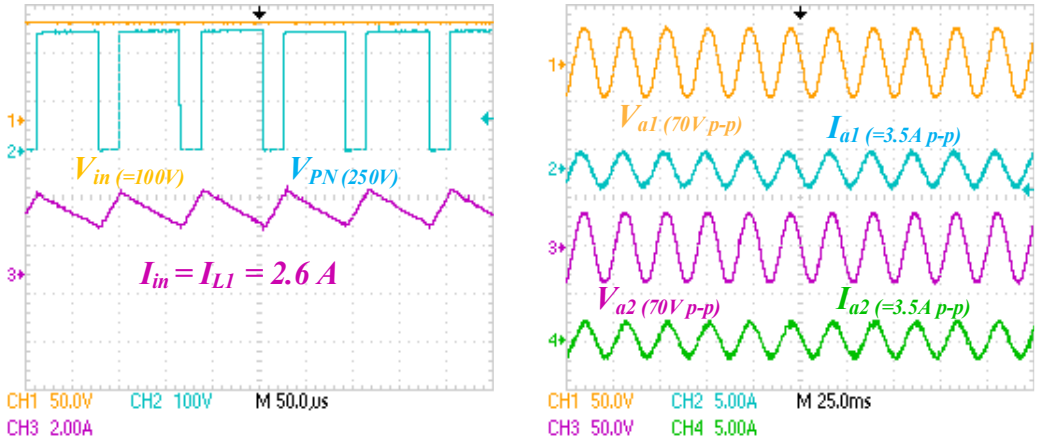
3.10 Efficiency Analysis of the Proposed Inverters

Figure 3.20 shows the results for the topology with two output units for same V_{in} =100 V, D and three-phase output voltage (35 V Peak/24.75 V rms) and load (load resistance of 15.32 Ω for peak load operation) for both parallel and series mode of operation. The peak power for the designed prototype is 240 W. Based on the values of the input and output voltages and currents, the efficiencies for the both modes of operation are calculated. Figures 3.20(a) and

(b) show the input and output voltages and currents for parallel mode of operation. Figures 3.20(c) and (d) show the input and output voltages and currents for series mode of operation. The output power is 240 W for both the modes of operation. Input currents (I_{in}) for these conditions for parallel and series mode are 2.65 A and 2.59 A, respectively. Thus input power P_{in} for parallel and series modes are 265 W and 259 W, respectively. The power efficiency ($i.e.\eta = \frac{P_{(3-\emptyset)out}}{P_{in}} * 100\ \%$) of the proposed inverters for parallel and series mode are equal to 90.6% and 92.45%, respectively. It can be observed that the input current in parallel mode (2.65 A) is more than that of the series mode (2.59 A). It is because the currents of two units are added in parallel mode, unlike the series mode. Thus, the efficiency in series mode of operation is more than that of parallel mode. Figure 3.21 shows the variation of efficiency with D and load resistance for parallel and series mode of operations with peak load of 240 W. It is observed that the efficiency for series mode operation is more than that of parallel mode as already discussed before. For Figure 3.21(a), it is clear that the efficiency in both modes decreases as the D is increased. Furthermore, in Figure 3.21(b), the efficiency in both the modes decreases as the load resistance is increased.

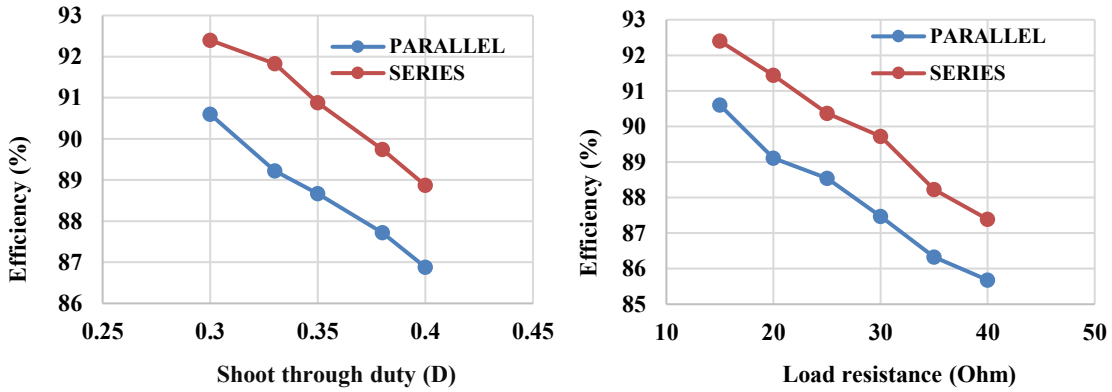


(a) (b)



(c) (d)

Figure 3.20: Steady-state response of proposed topology during parallel mode operation for equal V_{ref} for both units (a) Input voltage V_{in}, switch node voltage (V_{PN}) and input current $I_{in} = I_{L1}$, (b) V_{a1} (phase voltage), I_{a1} (phase current of inverter unit 1) and V_{a2} (phase voltage) I_{a2} (phase current of inverter unit 2) at V_{ref} = 35 V in parallel mode of inverter unit 1 and 2.



(a) (b)

Figure 3.21: Efficiency curve for peak load (240 W output) in parallel and series mode (a) Efficiency *Vs* Shoot-through duty ratio (*D*) and (b) Efficiency *Vs* load resistance.

3.11 Conclusion

This chapter proposes two topologies of three-phase quasi-z-source series-parallel multi-output (QSPMO) inverter with parallel and series mode operations. The proposed inverters are capable of supplying *n*-number of controlled three-phase AC voltage outputs simultaneously. The inverter topology with *n*-parallel connected three-phase inverters are capable of giving *n* numbers of different AC output voltages and variable load currents. The series mode of the proposed inverter gives *n*-number of AC outputs with same output voltages and load currents. The proposed 3-phase QSPMO inverters are capable of providing more than

one three-phase AC supply for microgrid applications or residential loads without connecting additional regulator or adaptor. The switching signals for the inverters are generated using hybrid modulation technique. As the proposed three-phase QSPMO inverters are based on impedance source network, they inherit the advantages such as shoot-through protection and both buck-boost output capability. Detailed mathematical modelling, steady-state and dynamic performance analyses are carried out in order to bring out the properties of the proposed inverters. A 240 W laboratory prototype has been developed to verify the performance of the proposed topologies.