"GATE INTERFACE STUDY FOR THE IMPROVEMENT OF ION-CONDUCTING DIELECTRIC BASED LOW OPERATING VOLTAGE THIN FILM TRANSISTOR"

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by

Nila Pal

SCHOOL OF MATERIALS SCIENCE AND TECHNOLOGY

INDIAN INSTITUTE OF TECHNOLOGY

(BANARAS HINDU UNIVERSITY)

VARANASI - 221005

Roll no- 17111502

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7.1 Conclusions

The emphasis of PhD work is on the synthesis of materials and their successful implementation in thin film transistors (TFTs) utilizing a low-cost solution method, as well as the development of low-operating-voltage high performance TFT devices using high-κ ion-conducting dielectrics. The presence of considerable charge trapping states at the dielectric/semiconductor interface due to the high polarisation of the high-κ ion-conducting dielectrics is one of the main challenges addressed here as the presence of interfacial trap states effectively degrades the TFT performances. So, the key objective of the thesis is to achieve better performance of the TFTs via different interfacial engineering thus reducing the effect of interfacial trap states. At the same time, the thermal budget of dielectric layer preparation has lowered up to 500°C to get an amorphous phase of the Li-Al_2O_3 gate dielectric and that significantly improves the surface smoothness and reduced probability of the leakage current through the grain boundaries. Also, ferroelectric field effect transistors have been fabricated using solution processed $LiNbO_3$ ferroelectric material as a gate dielectric and enhanced FEFETs performance by sandwiching $LiNbO_3$ in between high-κ ion-conducting dielectric.

In those goals, initially a SnO_2 TFT has been fabricated on p^{++}-Si substrates using a high-κ Li-Al_2O_3 dielectric. The outcomes of the TFT device were poor in terms of higher threshold voltage and subthreshold swing and which was mainly attributed to presence of higher amount of trap state density. After that a TiO_2 interfacial layer in between gate dielectric and gate electrode has been placed, and the comparative studies of two types of device with and without TiO_2 interface

has been carried out. In the material characterization part the X-ray diffraction pattern of three materials reveals the polycrystalline nature of TiO_2 interfacial layer with a tetragonal crystal structure, and SnO_2 semiconducting layer with a cubic crystal structure, whereas the Li-Al_2O_3 dielectric shows an amorphous nature when all films are annealed at 500°C. The surface micrographs of the single layer Li-Al_2O_3 shows a lower root-mean-square surface roughness than bilayer TiO_2/Li-Al_2O_3 but both the values are below 1 nm, quite applicable for TFT device fabrication. In contrast, the surface morphology of SnO_2 film on top of bilayer TiO_2/Li-Al_2O_3 shows a lower roughness compared to the film on the top of single Li-Al_2O_3 dielectric which indicates lower dielectric/semiconductor interface trap formation on bilayer TiO_2/Li-Al_2O_3 and may exhibit good device performance. Most interestingly, the dielectric characterization in metal-insulator-metal structure with both dielectric combinations shows that the areal capacitance is increased and the current density is reduced significantly with the bilayer TiO_2/Li-Al_2O_3 dielectric. A comparative study of two sets of SnO_2 TFTs with and without TiO_2 interface has been demonstrated. The Schottky junction formation between p^{++}-Si and n-type TiO_2 help to accumulate extra electrons at the Li-Al_2O_3/SnO_2 interface, which essentially fills up the interface trap-states significantly and reduces the sub-threshold swing (SS), threshold voltage (V_T) and enhance the carrier mobility of the device with compared to the device without TiO_2 interface. The high-κ value of TiO_2 improves the capacitance of the TiO_2/Li-Al_2O_3 stack dielectric. At the same time the leakage current is also reduced compared to single layered Li-Al_2O_3 dielectric. The better device performance has been achieved with higher carrier mobility (μ) of 16.4 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio of 7.2×10^3, and lower SS of 250 $mV.decade^{-1}$, V_T of 0.73 V in TiO_2/Li-Al_2O_3 stack dielectric based TFT.

In the second section, Mn_2O_3 thin film has been used in the gate electrode/gate dielectric interface in place of TiO_2 of earlier work. A comparison of device characterization of two distinct TFTs with and without Mn_2O_3 gate interface demonstrates that Mn_2O_3 induces more electrons to the semiconductor/dielectric interface trap states, reducing the threshold voltage and subthreshold swing of the device significantly. Furthermore, the depletion layer of the ITO/Mn_2O_3 interface suppresses gate leakage current largely, which helps to enhance the ON/OFF ratio of the device. A high capacitance of the dielectric film has been obtained by adding a high-κ Mn_2O_3 layer between the Li-Al_2O_3 gate dielectric and the gate electrode. This helps to achieve current saturation at a lower gate bias. The electron mobility of such a sub-volt TFT with an extra Mn_2O_3 layer in the gate dielectric was 17 $cm^2.V^{-1}.s^{-1}$, the ON/OFF ratio was 3.3×10^4, and the sub-threshold swing was 124 $mV.decade^{-1}$.

In the third section, a ferroelectric field effect transistor (FEFET) is fabricated for the first time with solution processed $LiNbO_3$ as a ferroelectric gate layer. The main drawback of the FEFET based memory devices is its short retention time due to presence of a depolarization field into the ferroelectric layer. A device model has been introduced with a sandwiched Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 dielectric structure to reduce the depolarization field and leakage current. A comparison investigation of FEFETs has been conducted with single layer $LiNbO_3$ ferroelectric and Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. The better device performance has been achieved in terms of high ON/OFF ratio of 1.6×10^4, carrier mobility of 1.9 $cm^2.V^{-1}.s^{-1}$, and SS of 167 $mV.decade^{-1}$ with the Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. The device also has a longer retention time than the earlier reports based on solution processed ferroelectric layer. It is proposed that the intervening of high bandgap Li-Al_2O_3 interfacial layers on both sides of $LiNbO_3$ results in complete charge compensation as well as prevents charge carrier injection

from p^{++}-Si and SnO_2. These phenomena support the better operation of the FEFET device with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric.

Lastly, a microwave irradiated ultra smooth a-C layer is processed via a low cost solution route and successfully implemented as an interface modification layer in between gate dielectric and semiconductor. A comparison of SnO_2 TFTs fabricated on top of high- κ Li-Al_2O_3 dielectric with and without an a-C layer has been performed. Very significant improvement has been observed in terms of high ON/OFF ratio of 7×10^4, carrier mobility of 21.1 $cm^2.V^{-1}.s^{-1}$, and SS of 147 $mV.decade^{-1}$ with the optimized a-C passivated TFT. The device is also showing better stability in the cyclic test with a very less hysteresis behavior.

Overall, my PhD work reveals a new avenue to select different materials for interfacial layers with high-κ dielectrics and different combinations of stack dielectric to enhance the TFT device performance.

7.2 Future perspectives

In this thesis work, I have developed a low operating voltage thin-film-transistor using high-κ ion-conducting gate dielectric via cost-effective solution route. Further, the device performance has been upgraded in terms of improvement of carrier mobility and ON/OFF ratio and lowering of threshold voltage and subthreshold swing by introducing different interfacial engineering. Still there is a room for this work to be developed further. The annealing temperatures of various thin films used here are ≤ 550°C, so they are not compatible for flexible electronics applications. So, some investigation can be done to lower the curing temperature maintaining the same device performances. Also, the retention time achieved by the FEFETs based on Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric is too far from demand of 10 years retention time. Hence, more studies

are needed to increase the retention time as well as lower the operating voltage further. As, in the Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric based FEFET Li^+ are associated to the charge compensation phenomena and in Li-Al_2O_3 the concentration of Li^+ is quite lower so another material with higher Li^+ concentration can facilitate the charge compensation more easily, hence can improve the device performance further. In addition, the low cost, low operating voltage interface modified high performance TFTs can be used to fabricate high performance optoelectronic devices (like photo detector, light emitting transistor etc.) and sensors. Moreover, ferroelectric FETs can be integrated into synaptic devices for possible development of artificial neurons.