Chapter 6:

Application of Microwave Synthesized Ultra-smooth a-C Thin

Film for the Reduction of Dielectric/Semiconductor Interface

Trap States of an Oxide TFT

6.1 Introduction

High dielectric constant (κ) materials are of great interest for the various applications in microelectronics.[185] Particularly for thin film transistor (TFT) application, a large number of high-κ dielectrics are developed which are used as gate insulators.[12, 41, 185] These high-κ dielectrics primarily reduce the operating voltage of TFTs with improved carrier mobility of the devices which can be useful for various portable electronics.[41] However, for the development of high performance TFT by using these high-κ gates dielectric, semiconductor/dielectric interface trap states play a crucial role.[186] Particularly for high-κ dielectric-based metal-oxide thin-film transistors, device performance highly affected from the scattering of carriers at the interface due to the surface roughness and high polarity constituents.[186, 187] Furthermore, the imperfect interface of dielectric/semiconductors creates a significant amount of charge trapping that effectively reduces the carrier mobility of the device. To resolve this critical issue, varieties of interface modification methods have been implemented to eliminate these shortcomings like the use of bilayer and multilayer dielectric stacks[76, 77], use of electron injecting layer in between gate dielectric/gate electrode interface[81, 101, 125, 188, 189], utilization of self-assembled monolayer (SAM) for interface modification[79, 190] and so on. In this chapter, an ultra-smooth amorphous carbon (a-C) layer has been used as a dielectric/semiconductor interface modification layer to enhance the device performance.

Amorphous carbon (a-C) is primarily a network of carbon atoms with a small to medium range of order and various hybridizations (sp, sp^2, sp^3).[191] The a-C doped with additional

components like H, N, O etc. can create numerous unique features.[192] As an example; chemical inertness, optical transparency, mechanical flexibility, ultra-smoothness and low friction coefficient are the unique features of hydrogenated amorphous carbon (a-C: H).[193] The application of a-C synthesized by various processes is extended to be an interface modifier in Li-ion battery[194], Dual-ion batteries[195], etc. Another class of sp^3 hybridized ultra-nanocrystalline diamond (UNCD) film which is a promising candidate for AFM tips and NEMS/MEMS devices due to their low friction and low wears resistance.[196-199] Also, some reports of source-drain and semiconductor contact modification of IGZO thin-film transistors (TFTs) with amorphous carbon nano-film shown a significant improvement in device performance[200]

In this chapter, I have particularly focused on a nitrogen-doped a-C film which has been implemented as an interface modification layer between metal-oxide (MO) semiconductor and high-κ ion-conducting gate dielectric for high-performance thin-film transistor fabrication. Herein, a unique thin-film fabrication method of a-C has been applied by using a low-cost solution process technique.[201, 202] In this process, microwave has been irradiated on a precursor film at room temperature by using a household microwave oven that can form an a-C thin film with ultra-low surface roughness (< 1 nm). For my PhD thesis work, I have used this a-C film as a gate dielectric/semiconductor interface layer. For that study, two sets of TFTs have been fabricated by using and without using a-C thin film. Their comparative study shows a remarkable improvement of device performance with a-C interface layer device which is due to the introduction of the ultra-smooth a-C interface layer. In addition, the high smoothness of the a-C layer helps reduce the interface trap state densities by the passivation of dangling bonds and defects of high-κ $Li-Al_2O_3$ dielectric. Also, the nitrogen dopant presented in the a-C forms an

excellent bonding with SnO_2 semiconductor which also improves dielectric/semiconductor interface. These phenomena essentially result in the enhancement of device performance and stability. A detailed description of this study has been given in this chapter.

6.2 Results and discussions

6.2.1 Surface Morphology and Chemical State Study

The surface morphology of films determines the interface property of the film with an adjacent layer. In the case of TFTs fabrication, the surface topography of dielectric thin film is very crucial issue to avoid unwanted carrier scattering, trapping and generation by the trap states of rough semiconductor/dielectric interface and charge trapping at the interface trap state.[203] Higher semiconductor/dielectric interface trap density of TFT increase the probability of leakage current and lower effective carrier mobility of the device. Here, a microwave synthesized carbon layer has been utilized as a passivation layer of gate dielectric of a TFT to reduce the surface roughness thus diminishing the interface trap state density and leakage current. Therefore, prior to TFT fabrication, the surface morphologies of Li-Al_2O_3 dielectric and a-C passivated Li-Al_2O_3 dielectric have been studied by atomic force microscopy (as shown in figure 6.1). The 2-dimensional (2D) and 3-dimensional (3D) views of the surface of Li-Al_2O_3 dielectric are shown in figures 6.1 a) and c) respectively whereas 2D and 3D surface morphology of a-C passivated Li-Al_2O_3 dielectric are shown in figures 6.1 b) and d) respectively. This study reveals that the surface micrographs of a-C passivated Li-Al_2O_3 has a much smoother surface with a root mean square surface roughness (R_{RMS}) of 0.24 nm compared to single layer Li-Al_2O_3 film surface (R_{RMS} = 0.93 nm).
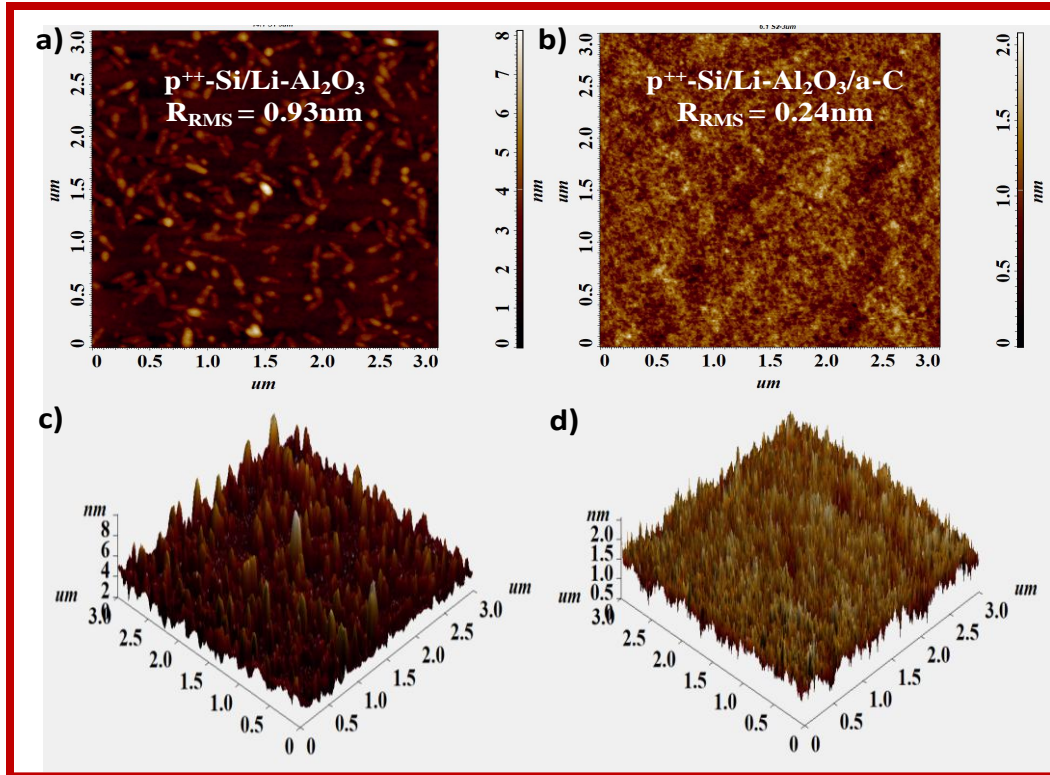
Figure 6.1 *Surface microstructures of bare Li-Al$_2$O$_3$ dielectric a) 2D, b) 3D on the top of p^{++}-Si substrates; and b) 2D, d) 3D micrographs after a-C layer passivation.*

The lower roughness of the a-C film can be attributed to the nitrogen doping in the film.[204] The presence of N atom in the a-C layer can also be confirmed from the XPS data. It is previously reported that the passivation of the electronic defects[205] and stress relief[206] of a-C film can be possible by N-doping, which effectively helps to enhance the surface smoothness. Further, the smoother surface of the a-C passivated Li-Al$_2$O$_3$ layer would positively impact on the interface formation with the above lying semiconducting layer in the case of TFT fabrication. From the XPS study, it is found that the Sn peak of SnO$_2$ semiconductor layer with amorphous carbon (a-C) film and without a-C film has a shift in Sn 3d$_{5/2}$ of 0.12 eV, and Sn 3d$_{3/2}$ of 0.17 eV (figure 6.2 a)). Whereas in the N 1s peak of a-C thin film with and without adjacent SnO$_2$ layer has a shift of 0.72 eV (figure 6.2 b)), that indicate the formation of coordination bond between

Sn and N atom.[207] Thus, a-C film act as a binder for better growth of SnO_2.[208] The presence of pyridinic N in a-C film interacts with Sn of the SnO_2 layer.[209] Further, the donor ability of N is better than O and being a Lewis acid, Sn^{4+} interacts more strongly with N of a-C film which improves the electron flow of the device. Thus, low interface trap states in the semiconductor/dielectric interface are attainable with this a-C passivated Li-Al_2O_3 dielectric with lower roughness, significantly minimizing the device's subthreshold swing. Moreover, a dielectric with a lower roughness decreases carrier scattering, improving the device's effective carrier mobility. Consequently, a lower-roughness a-C passivated Li-Al_2O_3 dielectric may indeed be advantageous for the construction of high-performance low-operating-voltage TFTs.
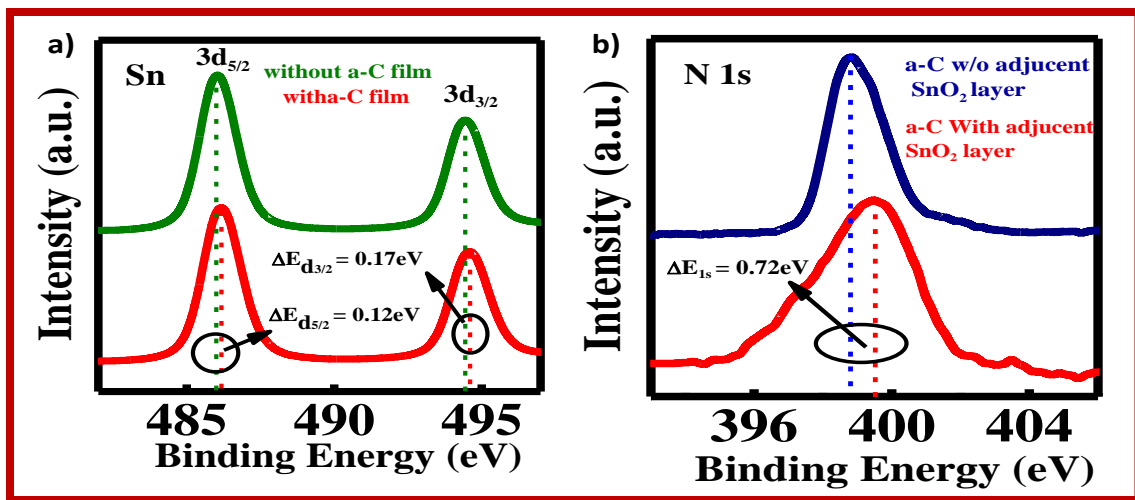

Figure 6.2 *XPS spectra of a) Sn 3d from SnO_2 with (red color online) and without (green color online) underlying a-C layer; b) N 1s from a-C with (red color online) and without (navy blue color online) adjacent SnO_2 layer at high resolution.*

6.2.2 Dielectric and Electronic characterization of MIM Devices

Frequency-dependent capacitance (C_i–f) and current-voltage (I–V) measurements are performed in a metal-insulator-metal (MIM) device architecture to demonstrate the dielectric properties of the as-deposited Li-Al_2O_3 and Li-Al_2O_3/a-C films (the schematics of MIM devices are shown in figure 6.3 a) and b), respectively). The variation of the areal capacitance with frequency for both the MIM devices has been shown in figure 6.3 c). It is observed from the capacitance dispersion relation that the single layer Li-Al_2O_3 based MIM device shows higher areal capacitance (C_i) over the bilayer Li-Al_2O_3/a-C MIM device throughout the frequency range. At 50 Hz frequency, the single-layer dielectric exhibits a C_i value of 390 nF.cm^{-2}. In contrast, the value for bilayer a-C/Li-Al_2O_3 dielectric is 65 nF.cm^{-2}; about six times lower than the single-layer dielectric-based MIM device. The areal capacitance values at the lower frequency range have been considered for mobility calculation to avoid overestimation of carrier mobility. The higher value of capacitance in single layer Li-Al_2O_3 is feasible due to its high-κ nature, caused by Li-ion movement in the alumina matrix.[75] But the drastic change in capacitance value by incorporating a-C layer on the top of Li-Al_2O_3 dielectric may be attributed to the series combination formation of two different dielectric materials that are well established, mathematically represented by equation 6.1. Also, it is essential to note that the a-C layer has considerably lower relative permittivity that may significantly lower the areal capacitance value of the a-C/Li-Al_2O_3 stack.[210]

$$\frac{1}{C_{effective}} = \frac{1}{C_{a-C}} + \frac{1}{C_{Li-Al_2O_3}} \dots \dots \dots \dots \dots (6.1)$$
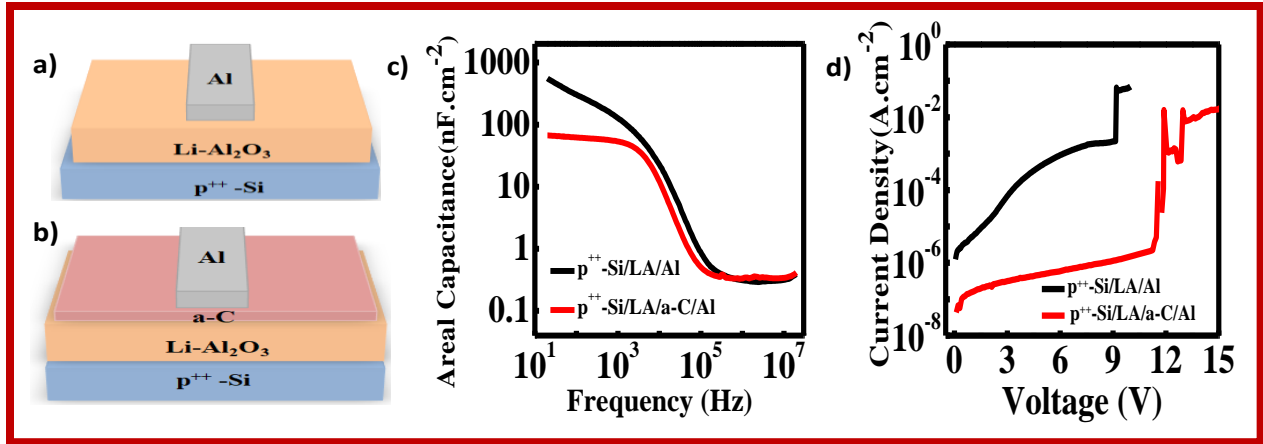
Figure 6.3 *Schematic diagrams of metal-insulator-metal (MIM) device structures with a) only Li-Al$_2$O$_3$, b) a-C passivated Li-Al$_2$O$_3$, c) areal capacitance vs. frequency, and d) current density vs. voltage relationship of both MIM devices.*

Leakage current through the dielectric layer plays a crucial role in TFT performance. In an ideal case, the leakage should be as less as possible, and the higher gate leakage current introduces a high off current in the TFT device, hence reducing the current ON/OFF ratio. So, the current densities also have been measured with the same set of MIM devices with the applied voltage, as illustrated in figure 6.3 d). Most interestingly, the current density with the a-C is around two order lower (3×10^{-7} A.cm^{-2} at the applied voltage of 3 V) with respect to the single-layer Li-Al$_2$O$_3$ based MIM (7×10^{-5} A.cm^{-2} at 3.0 V) device within the voltage range of 3-9 V. The spikes have been originated due to the dielectric breakdown which is associated to different intrinsic mechanism. Due to the ultra-smooth, defect-free film formation of the insulating a-C layer on the top of the Li-Al$_2$O$_3$ dielectric restricts the carrier drifting through the dielectric film, which constructively reduces the current density in the case of Li-Al$_2$O$_3$/a-C based MIM device significantly. This lower current density will be maintained in the TFT geometry when this a-C layer will be introduced as a semiconductor/dialectic interface layer and will be reflected as gate

leakage current of the device. Therefore, this study indicates that addition of a-C layer on top of Li-Al$_2$O$_3$ dielectric can reduce the OFF current value of TFT and can enhance the ON/OFF ratio of the device. All the key parameters extracted from the MIM devices have been enlisted in Table 6.1

Table 6.1 *Summary of key parameters extracted from MIM devices*

MIM Device	C [nF.cm^{-2}] (at 50 Hz)	Current Density [A.cm^{-2}] (at 3 V)
p^{++}-Si/Li-Al$_2$O$_3$/Al	390	7×10^{-5}
p^{++}-Si/Li-Al$_2$O$_3$/a-C /Al	65	3×10^{-7}

6.2.3 Electronic Measurements of TFTs

To investigate the impact of the a-C passivation layer on TFT performance, two sets of TFTs have been prepared with bottom gate -top contact geometry, and an n-type SnO$_2$ semiconductor is used as an active channel layer. In one set, a reference device of single layer Li-Al$_2$O$_3$ dielectric-based TFT is fabricated and named device-1. On the other hand, the second set of devices is prepared called device-2 by introducing an ultra-smooth a-C passivation layer between the gate dielectric and semiconductor. The schematic diagrams of device-1 and 2 have been illustrated in figures 6.4 a) and b), respectively. Electronic characterization of all the TFTs has been carried out in an ambient atmosphere. To avoid exaggeration of carrier mobility (μ) due to the grain boundary effect, which is significantly dominant below 25 μm channel width with a W/L ratio below 10, we have taken all TFTs having a channel width (200 μm) that is sufficiently greater with a high W/L ratio (118).[102, 103] The typical sets of output and transfer characteristics of the as-prepared devices are illustrated in figure 6.4. The I$_D$-V$_D$ curves of device-1 and device-2 are shown in figures 6.4 c) and e), respectively. During I$_D$ vs. V$_D$

measurement, the drain voltage is swept from 0 to 2 V while varying gate voltage from -0.5 to 3 V for device-1 and -1.5V to 3 V for device-2 with a step of 0.5V. This comparative study indicates a superior output characteristic with a good ON current has been achieved with device-2, while device-1 reveals a poor ON current level at the same applied V_G.

Further, a decrease in ON current in a higher V_D range instead of saturation has been observed in device-1, mainly attributed to high impedance in the accumulation mode of operation of the semiconducting channel due to larger interface defect formation. Figures 6.4 d) and f) show the I_D-V_G plot of device-1 and device-2, respectively, where the gate voltage is swept from -0.5 to 3 V for device-1 and -1.5 to 3 V for device-2, V_D is kept constant at 1 V for both cases All the critical parameters of TFTs have been extracted from the transfer characteristics, and the values are enlisted in Table 6.2. For the calculation of subthreshold swing (SS) and carrier mobility slopes are derived from log (I_D) vs. V_G (shown in figures 6.4 g) and i) for device-1 and device-2, respectively) and (I_D) $^{1/2}$ vs. V_G (shown in figures 6.4 h) and j) for device-1 and device-2, respectively) curves by linear fitting for both devices. Carrier mobility, SS, and interface trap state density have been calculated using equations 6.2, 6.3 and 6.4, respectively.

$$\mu = \frac{(\frac{\partial \sqrt{I_D}}{\partial V_G})^2}{\frac{1}{2} \times \frac{W}{L} \times C} \dots\dots\dots\dots\dots.. (6.2)$$

$$SS = \left[\frac{\partial(\log I_D)}{\partial V_G}\right]^{-1} \dots\dots\dots\dots\dots. (6.3)$$

$$N_{SS}^{Max} = \left[\frac{SS \times \log e}{\frac{kT}{q}} - 1\right]\frac{C}{q} \dots. (6.4)$$
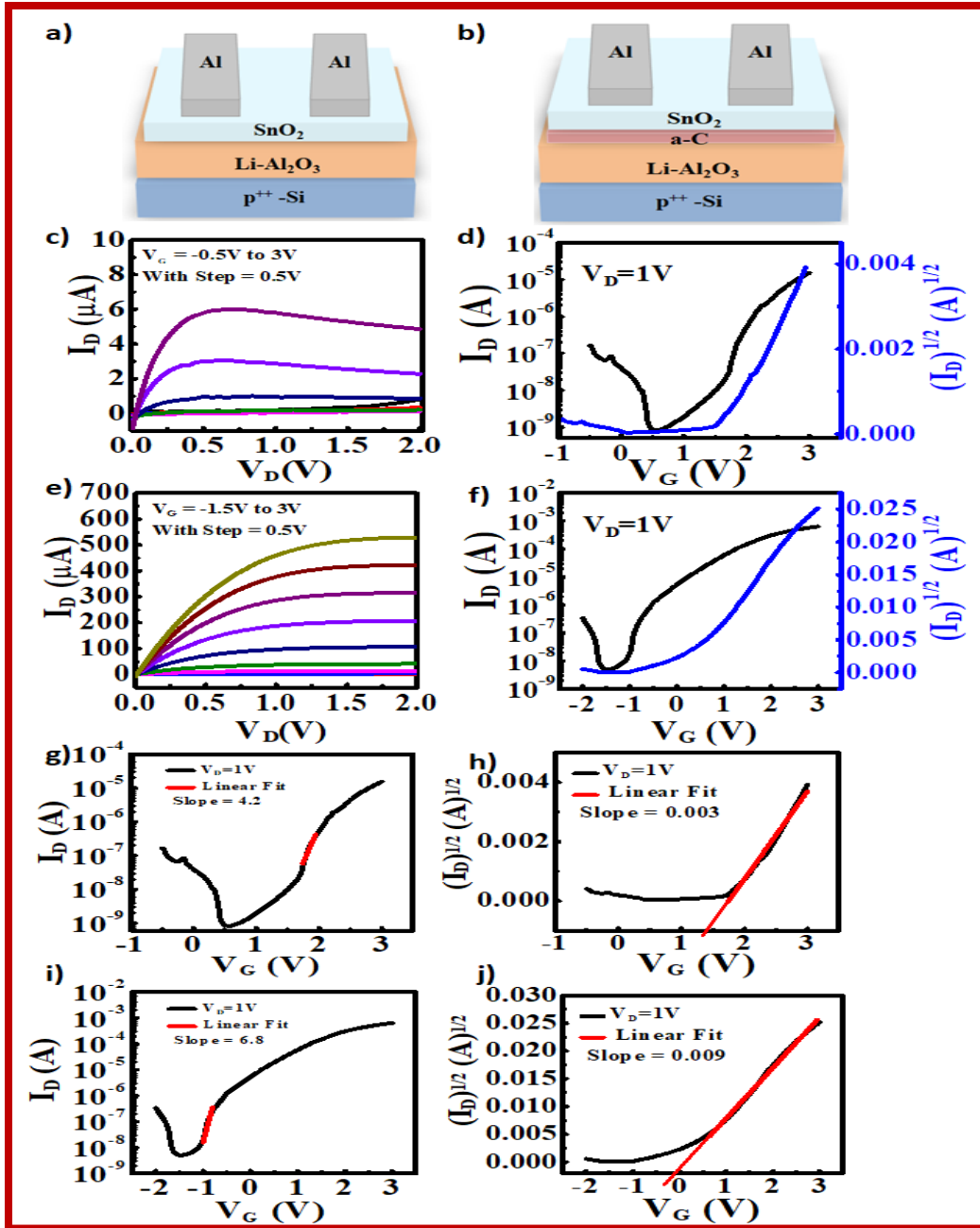
Figure 6.4 *Representative device configuration of TFTs a) without (device-1), b) with (device-2) a-C layer. The output characteristics of c) device-1, and e) device-2. Transfer characteristics of d) device-1 and f) device-2 at constant V_D=1 V. Linear fitting at lower region of log (I_D) vs. V_G curves of g) device-1, i) device-2 for Subthreshold Swing value calculation. Linear fitting of (I_D)$^{1/2}$ vs. V_G curve of h) device-1, and j) device-2 to extract the slope for mobility calculation.*

where C, I_D, V_G, W, L, V_T, k, T, e stands for the areal capacitance of the dielectric, saturation drain current, gate voltage, width and length of the device channel, threshold voltage, Boltzmann constant, room temperature in Kelvin scale, and electronic charge, respectively. The comparative study between two TFTs demonstrates that the mobility value has increased drastically, whereas the threshold voltage (V_T) decreases significantly by introducing an amorphous-carbon (a-C) passivation layer. Device-2 exhibits carrier mobility of 21.1 $cm^2.V^{-1}.s^{-1}$ and V_T of -0.09 V, and device-1 has values of 0.36 $cm^2.V^{-1}.s^{-1}$ and 1.40 V, respectively. Here, the negative value of V_T in the case of device-2 indicates that the device is working in the accumulation mode even under zero applied gate bias. Besides that, device-2 displays one order higher ON/OFF ratio of 7.0×10^4 and a relatively lower SS of 147 $mV.decade^{-1}$ than device-1 (ON/OFF ratio 9.9×10^3 and SS of 238 mV. $decade^{-1}$). The possible reason behind the lowering of V_T and SS in device-2 is reducing the interfacial trap state after the intervention of the ultra-smooth a-C layer. The calculated interfacial trap state density for device-2 is 6.0×10^{11} cm^{-2} which is one order lower than device-1 (7.0×10^{12} cm^{-2}), essentially supporting the reduction of SS and V_T value of device-2.

Table 6.2 *Summary of the TFT parameters*

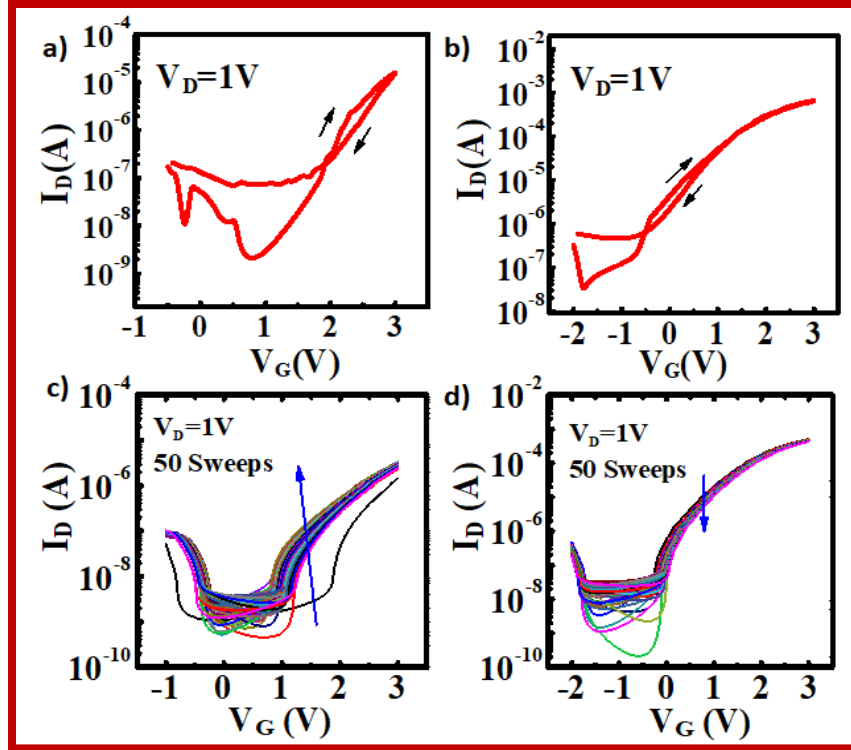| Device	Threshold Voltage (V)	ON/OFF ratio	Subthreshold Swing (mV.decade^{-1})	Carrier Mobility (cm^2.V^{-1}.s^{-1})	Interface trap-state density (cm^{-2})
p^{++}-Si/Li-Al$_2$O$_3$/SnO$_2$/Al	1.40	9.9×10^3	238	0.36	7.3×10^{12}
p^{++}-Si/ Li-Al$_2$O$_3$/a-C /SnO$_2$/Al	-0.09	7.0×10^4	147	21.1	6.0×10^{11}

Figure 6.5 *The to and fro sweep of gate voltage at constant $V_D = 1$ V for a) device-1 and b) device-2 to check the hysteresis nature of the devices. Cyclic stability test of c) device-1 and d) device-2 with 50 sweep cycles.*

Furthermore, the hysteresis behavior and cyclic stability test for both the devices have been conducted to check the stability performances, as illustrated in figure 6.5. The hysteresis behavior in the transfer curve has been depicted in figures 6.5 a) and b) for device-1 and device-2, respectively. The figures clearly illustrate that device-2 has negligible clockwise hysteresis during the to and fro sweep of V_G, but device-1 has a substantially more significant value. Also, the clockwise hysteresis nature of the I_D-V_G plot is the indication of charge trapping-releasing at the interface.[211] In addition, the cyclic test of 50 sweeps with an interval of 1 second is carried out for both devices (figure 6.5 c) for device-1 and d) for device-2). From figure 6.5 d), a minimal change can be noticed in the case of device-2 after a 50-time sweep, but a notable shift

in the transfer characteristics has been observed in figure 6.5 c) for device-1. The distinction of hysteresis behavior of these two TFTs reflect the more stable nature of device-2, which is also the signature of lower interfacial trap state density of device-2.

6.3 Conclusions

In summary, a SnO_2 thin film transistor has been fabricated successfully using sol-gel-derived Li-Al_2O_3 as a gate dielectric. A remarkable improvement in the device performance has been realized by inserting a microwave synthesized ultra-smooth a-C layer between gate dielectric and semiconductor as a passivation layer. The coordination bond formation between N and Sn atom helps for better growth of SnO_2 on the top of a-C layer. In addition, the high smoothness of the a-C layer essentially reduces the interface trap state densities by passivation of dangling bonds and defects of high-κ Li-Al_2O_3 dielectric. These phenomena effectively enhance the device performance and stability with a-C layer. Therefore, we have achieved a better device performance in terms of higher carrier mobility of 21.1 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio of 7.0×10^4, and lower SS value of 147 $mV.decade^{-1}$ in device-2, with the a-C passivation layer. Also, this device exhibits lower hysteresis and better stability under cyclic sweep test over device-1. This state of the art study demonstrates the application of a microwave grown ultra-smooth a-C thin film as an interface modification layer to improve TFT device performance.