Chapter-5

5.1 Introduction

Metal oxide based ferroelectric materials are of great scientific and technological significance owing to their numerous implementations as sensors[144, 145], photovoltaics[146-148], energy harvesting devices[149, 150], memory devices[151, 152], synaptic devices[153-155], and so forth. Among different ferroelectric oxides like, HfO_2[156, 157], ZrO_2[158], $BaTiO_3$ (BTO)[159], $SrTiO_3$(STO)[160] etc. are well-studied materials which are widely used for memory applications. Beside these examples, lithium niobate ($LiNbO_3$, LN) is an interesting material that reveals excellent chemical and physical properties such as ferroelectric[161], piezoelectric[162], pyroelectric[163], electro-optical[164], photorefractive[165] and nonlinear properties[166]. Because of these features, it has a large range of applications, including waveguides, surface acoustic wave devices, and nonvolatile memory components[167, 168]. Nowadays, the hierarchical memory system of devices with varying speed, density, and cost has been adopted to optimize the performance-cost tradeoff. As the CMOS scaling is approaching fundamental limits, some new nonvolatile memory (NVM) concepts have been proposed and made significant progress in recent years.[169] Among them, ferroelectric field-effect transistors (FEFET) are paid massive attention as nonvolatile memories due to their fascinating features like non-destructive read-out, high-density integration possibility, and the high switching speed of reading and writing, and low power consumption.[170, 171] Instead of having number of advantages of FEFET, there is a critical issue of low retention time that needs to be addressed for realistic application. The reasons behind the comparatively short retention time are mainly based

on a depolarization field of inside ferroelectric thin film and gate leakage followed by trapping.[172] This depolarization field of FEFET develops due to the uncompensated charge accumulation in the semiconductor channel resulting from the low carrier density of semiconductor channel. Therefore, number of efforts has been taken to minimize these effects, by insertion of an interfacial buffer layer along with the ferroelectric gate dielectric.[173-176] Instead of extensive study of ferroelectric features of $LiNbO_3$, till now there are no reports on $LiNbO_3$-based FEFET fabrication so far.

In this chapter, I have tried to identify the critical issue for fabrication of $LiNbO_3$-based FEFET devices. Primarily, my goal was to reduce the depolarization field that originated in the $LiNbO_3$-based FEFET. For this purpose, I proposed a model of sandwiched stacked dielectric of $LiNbO_3$ instead of single layer $LiNbO_3$. According to this model, $LiNbO_3$ has been sandwiched with two Li-Al_2O_3 which provided free Li^+ that polarized easily, preventing the depolarization field generated inside $LiNbO_3$ thin film. Based on this model, I have fabricated solution-processed SnO_2 ferroelectric field-effect transistors with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 gate dielectric. A clear improvement has been observed in the retention time of this Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 based FEFET which is due to the improvement of ON/OFF ratio, carrier mobility and reduction of subthreshold swing (SS) of the device with respect to the $LiNbO_3$ only device.

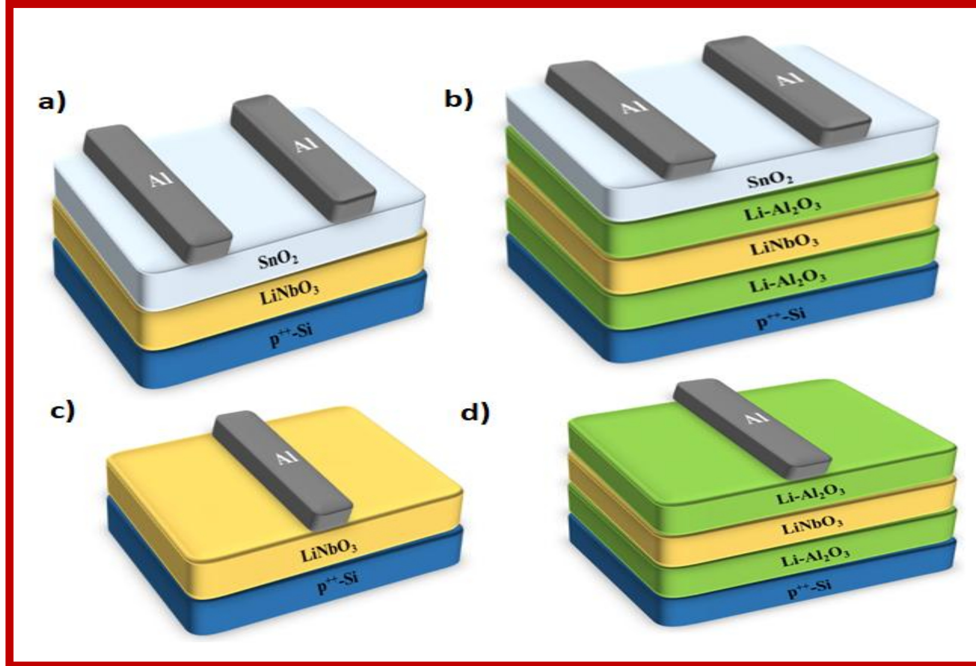

Figure 5.1 *Schematic configuration of SnO_2 FEFET with a) only $LiNbO_3$ (LN) ferroelectric (device-1) and b) Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 (LA/LN/LA) stack dielectric layer (device-2) as the gate material. Metal-insulator-metal (MIM) devices have been illustrated with c) only ferroelectric and d) stacked dielectric layer, respectively.*

5.2 Results and discussions

5.2.1 XRD Analysis

The proper distinction of the crystallographic phases of the materials is very crucial for their device application. Therefore, the X-ray Diffraction measurement of the dielectric $LiNbO_3$ thin film has been done to check its crystallographic phase. Figures 5.2 a) and b) show the GIXRD patterns obtained from films annealed at 400°C and 500°C respectively, deposited on p^{++}-Si (111) substrates. The diffraction pattern of $LiNbO_3$ film annealed at 400°C for 1 hour shows crystalline nature with a sharp peak at $2\theta = 56.14^{\circ}$, corresponding to the plane (122), indicating a

single-phase rhombohedral (trigonal) structure. In contrast, the other precursor $LiNbO_3$ film which was annealed at 500°C for 30 minutes shows multiple peaks in GIXRD data (Figure 5.2 b), indicating its polycrystalline nature. Crystallographic indexation was obtained using JCP: 00-074-2238 for trigonal (R3c) indicating (012), (104), (110), (113), (024), (116), (122), (214) and (226) as principal directions.[177] No impurity phase has been found in both cases. GIXRD data of these two different temperature annealing conditions indicated that the polycrystalline nature increased with increasing temperature of annealing condition. Besides, the sample with 400°C gives a unidirectional growth of $LiNbO_3$ in the direction of (122) plane which can be beneficial for FEFET fabrication. Therefore, for FEFET application, an annealing temperature of 400°C has been used to facilitate the ferroelectric property of gate dielectric. Li-Al_2O_3 is the another component of stacked dielectric which forms an amorphous phase under 400°C annealing and the SnO_2 thin film forms a polycrystalline phase under same annealing condition which has been reported in our earlier publication.[125]

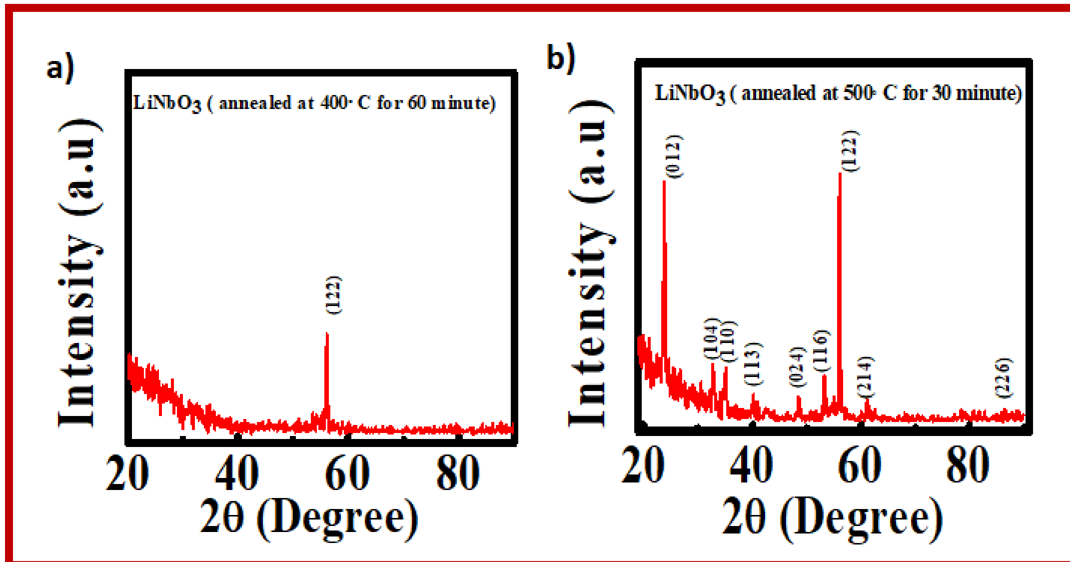

Figure 5.2 *GIXRD patterns of $LiNbO_3$ thin film a) annealed at 400°C for 1 hour, b) annealed at 500°C for 30 minutes.*

5.2.2 UV-Vis Spectra Study

The $LiNbO_3$ (LN) thin film has been prepared on quartz substrates by following the same condition of FEFET fabrication for UV-Vis spectra measurement. Here, both the absorbance and transmittance data have been shown in figure 5.3 a) for LN thin film. This study indicates that the $LiNbO_3$ thin film has nearly 100 % transparency in the UV region (350 nm) and about 95 % in the visible-NIR regions (400-800 nm). The optical band gap of LN has been extracted from absorption coefficient data. According to the theory, the relation between optical absorption, absorption coefficient (α), photon energy (hν) are given by the equation 5.1

$$\boldsymbol{\alpha = \frac{A\left(h\nu - E_g\right)^n}{h\nu}} \ldots\ldots\ldots\ldots\ldots..(\mathbf{5.1})$$

where A and n are constants. For direct allowed transition, n=1/2, and for the indirect allowed transition, n=2.32. Figure 5.3 b) shows the variation of $(\alpha h\nu)^2$ with photon energy (hν) (Tauc plot). The straight-line nature of the graph indicates the direct bandgap of the material. The optical band gap of LN has been calculated by extrapolating the straight line from Tauc plot, yielding the direct band gap value of 4.33 eV. This optical band gap is consistent with the earlier reports.[167, 178, 179]

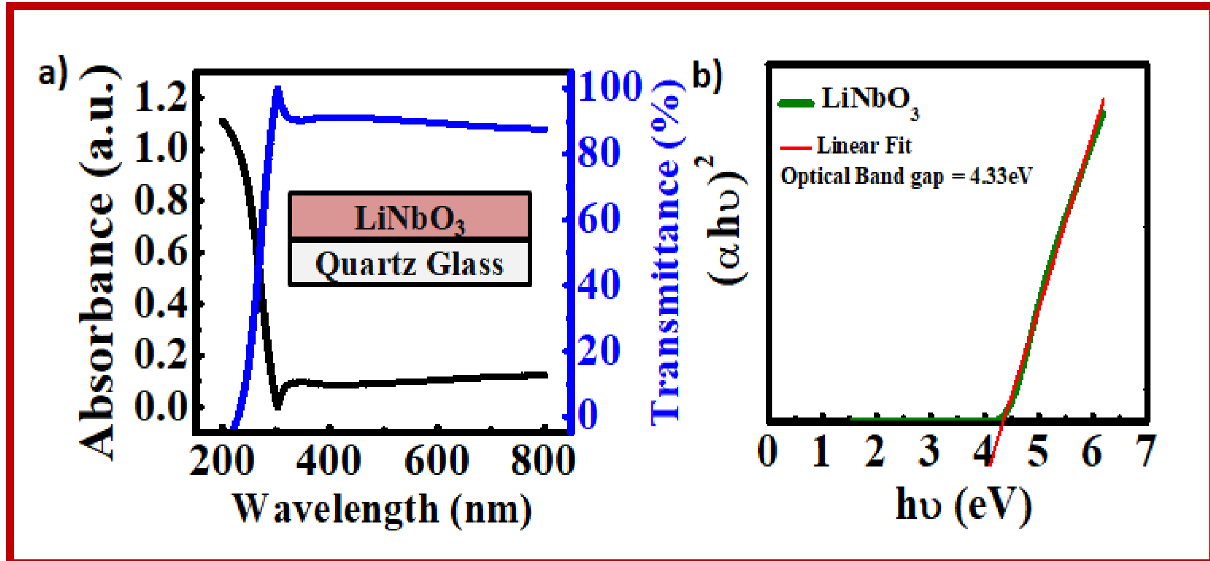

Figure 5.3 *The a) UV-Vis Spectra of $LiNbO_3$ thin film deposited on quartz glass, b) Tauc plot using the absorbance data to obtain optical band gap of $LiNbO_3$ thin film annealed at 400°C.*

5.2.3 Surface Morphology

The quality of surface morphology of both LN and stacked LA/LN/LA layer after thermal annealing has been examined by root mean square (RMS) roughness measurement using atomic force microscopy (AFM) as illustrated in figure 5.4. The surface topography in 2-D and 3-D of LN and LA/LN/LA thin films which are annealed at 400°C are shown in figures 5.4 a) and b) and figures 5.4 c) and d) respectively. This study indicates the surface RMS roughness of single and tri-layer stacked dielectric are 5.9 nm and 4.6 nm respectively. The decrease in surface roughness with the stacked device can be beneficial for overall improvement of FEFET behavior due to lower dielectric/semiconductor interface trap states with respect to the single layer device. To support the above statement, SnO_2 semiconductor film has been deposited on top of those two dielectric thin films under the same condition that followed for FEFET fabrication and the surface morphologies of the single-layer LN (figure 5.4 e) and f)) and stacked dielectric (figure

5.4 g) and h)) have been studied. From this study, it clear that the SnO_2 film on stacked LA/LN/LA dielectric has significantly lower surface roughness (R_{RMS} = 2.5 nm) than SnO_2 film on single layer LN film (R_{RMS} = 5.5 nm).

5.2.4 Dielectric properties

The capacitance dispersion relation with frequency (range 20-10^7 Hz) has been measured and depicted in figure 5.5 a) for both the MIM devices having the geometry of p^{++}-Si/LN/Al (figure 5.1 c)) and p^{++}-Si/LA/LN/LA/Al (figure 5.1 d)), respectively. Areal Capacitance values of 625.6 $nF.cm^{-2}$ and 378.7 $nF.cm^{-2}$ for the p^{++}-Si/LN/Al and p^{++}-Si/LA/LN/LA/Al devices, respectively, have been obtained at 50 Hz frequency. These values are utilized to calculate the saturation field-effect mobility of the respective FEFET devices. The areal capacitance values at the lower frequency region have been chosen to avoid the overestimation of mobility calculation. The capacitance value of p^{++}-Si/LA/LN/LA/Al has been observed to be lower than p^{++}-Si/LN/Al. This is mainly attributed to the formation of the series combination of three dielectric layers in the case of stacked dielectric, following equation 5.2[92]

$$\frac{1}{C_{effective}} = \frac{1}{C_{Li-Al_2O_3}} + \frac{1}{C_{LiNbO_3}} + \frac{1}{C_{Li-Al_2O_3}} \dots\dots (5.2)$$

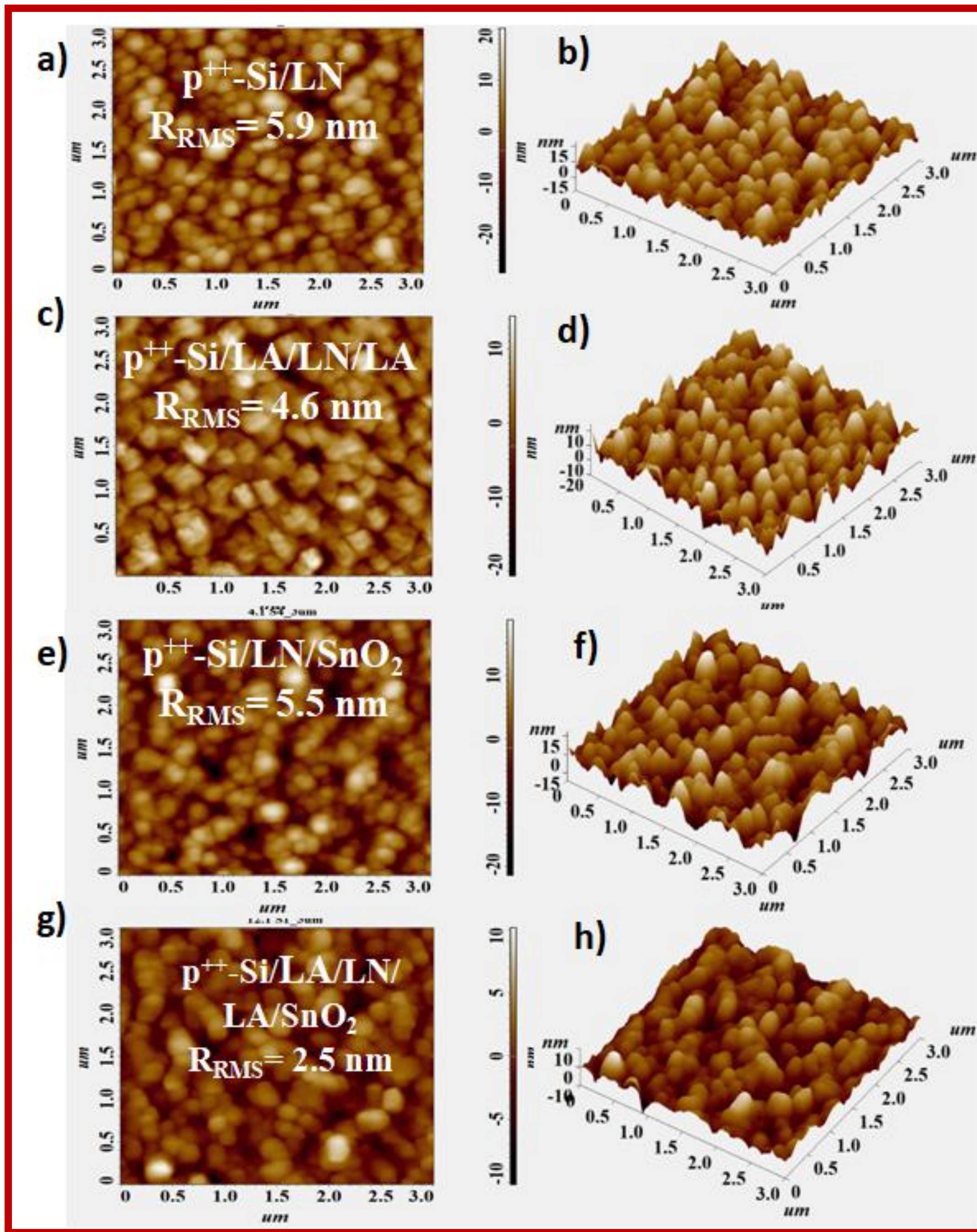

Figure 5.4 *Surface topography of p^{++}-Si/LN a)2D and, b) 3D; p^{++}-Si/LA/LN/LA/Al c) 2D and, d) 3D; p^{++}-Si/LN/SnO_2 e) 2D and, f) 3D; p^{++}-Si/LA/LN/LA/SnO_2 g) 2D and h) 3D, respectively.*

The same devices have been used for current measurement with respect to applied voltage for both the dielectric films illustrated in figure 5.5 b). It is observed that the current density of p^{++}-

Si/LA/LN/LA/Al and p^{++}-Si/LN/Al are 2.5×10^{-6} and 4.7×10^{-5} $A.cm^{-2}$ at an applied gate voltage of 4 V respectively. This indicates that the additional Li-Al_2O_3 layer is reducing DC conductivity of dielectric film by ~19 times. The lower DC conductivity of stacked ferroelectric MIM devices indicates high potential barrier formation by the Li-Al_2O_3 layer, preventing charge carrier injection. These ranges of current densities of the dielectric films are considerably low for low operating voltage tin film transistor (TFT) applications.

The most important and unique properties of a ferroelectric film for memory applications are its remnant polarization in the absence of an externally applied field and the reversibility of the polarization direction by applying an electric field of sufficient magnitude called the coercive field.[180] Figures 5.5 c) and d) show the ferroelectric performances of all solution-processed LN ferroelectric capacitors as well as of LA/LN/LA stacked dielectric capacitors with the same MIM devices. The room temperature polarization-electric field (P-E) loop reveals the lossy natured ferroelectric behavior as shown in figure 5.5 c) for LN films annealed at 400°C. The observed lossy nature in LN is due to the oxygen vacancies created during synthesis. The oxygen vacancies may suppress the dipole formation due to the deficiency in the charge densities, i.e., unequal amounts of positive and negative charges. This leads to low resistivity and high leakage current in the presence of the applied field leading to lossy nature.[181] On the other hand, the stacked ferroelectric shows better results (figure 5.5 d)). Ferroelectric capacitors show remnant polarization (P_r) of 0.463 $\mu C.cm^{-2}$ and 0.029 $\mu C.cm^{-2}$ for stacked ferroelectric and single LN layer, respectively. The P_r value of single layer $LiNbO_3$ is quite similar to the earlier report.[182] All the MIM device outcomes are enlisted in Table 5.1.

Table 5.1 *Summary of the MIM device parameters*

Device	Areal Capacitance ($nF.cm^{-2}$)	Current Density ($A.cm^{-2}$)		Remnant Polarization ($\mu C.cm^{-2}$)
		At 4V	At 10V	
p^{++}-Si/LN/Al	625.6	4.7×10^{-5}	7.8×10^{-4}	0.029
p^{++}-Si/LA/LN/LA/Al	378.7	2.5×10^{-6}	7.3×10^{-5}	0.463

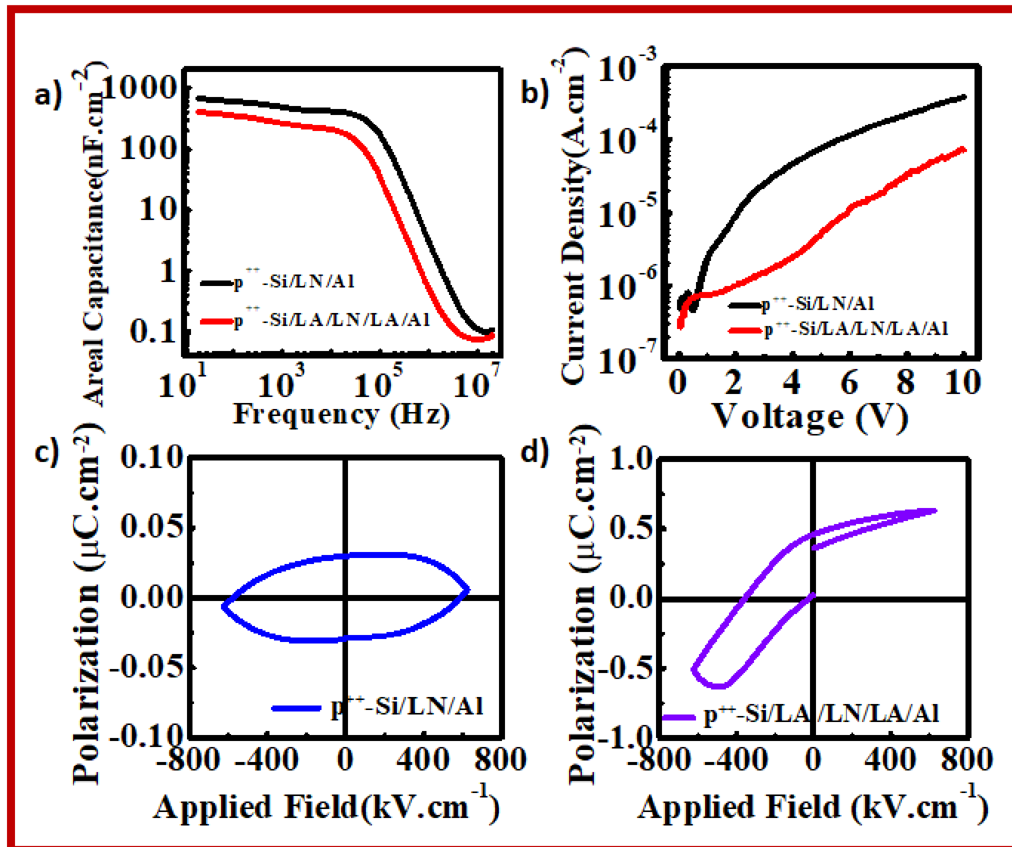

Figure 5.5 *a) Capacitance dispersion relation with frequency and b) leakage current density vs. voltage measurement; polarization vs. applied field measurement of c) p^{++}-Si/LN/Al and d) p^{++}-Si/LA/LN/LA/Al MIM device, respectively.*

5.2.5 Electronic characteristics of Transistors

Two types of ferroelectric field-effect transistors (FEFET) have been fabricated on heavily boron-doped Si substrates, which act as gate electrodes. Here, a single layer of $LiNbO_3$ (LN) ferroelectric and Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 (LA/LN/LA) stacked dielectric layer have been incorporated as gate insulators for two different types of FEFET device fabrication, termed as device-1 (figure 5.1 a)) and device-2 (figure 5.1 b)), respectively. In addition, the n-type SnO_2 semiconductor plays the role of an active channel layer and Aluminum as source-drain electrodes for both FEFETs. The measured drain current (I_D) vs. drain voltage (V_D) characteristics of the fabricated SnO_2 FEFETs have been demonstrated in figure 5.6 a) for device-1 and c) for device-2, maintaining the same channel width to length ratio (W/L) of 118 (23.6 mm /0.2 mm) for all the devices. During output characteristics measurement, the drain voltage (V_D) has been swept to

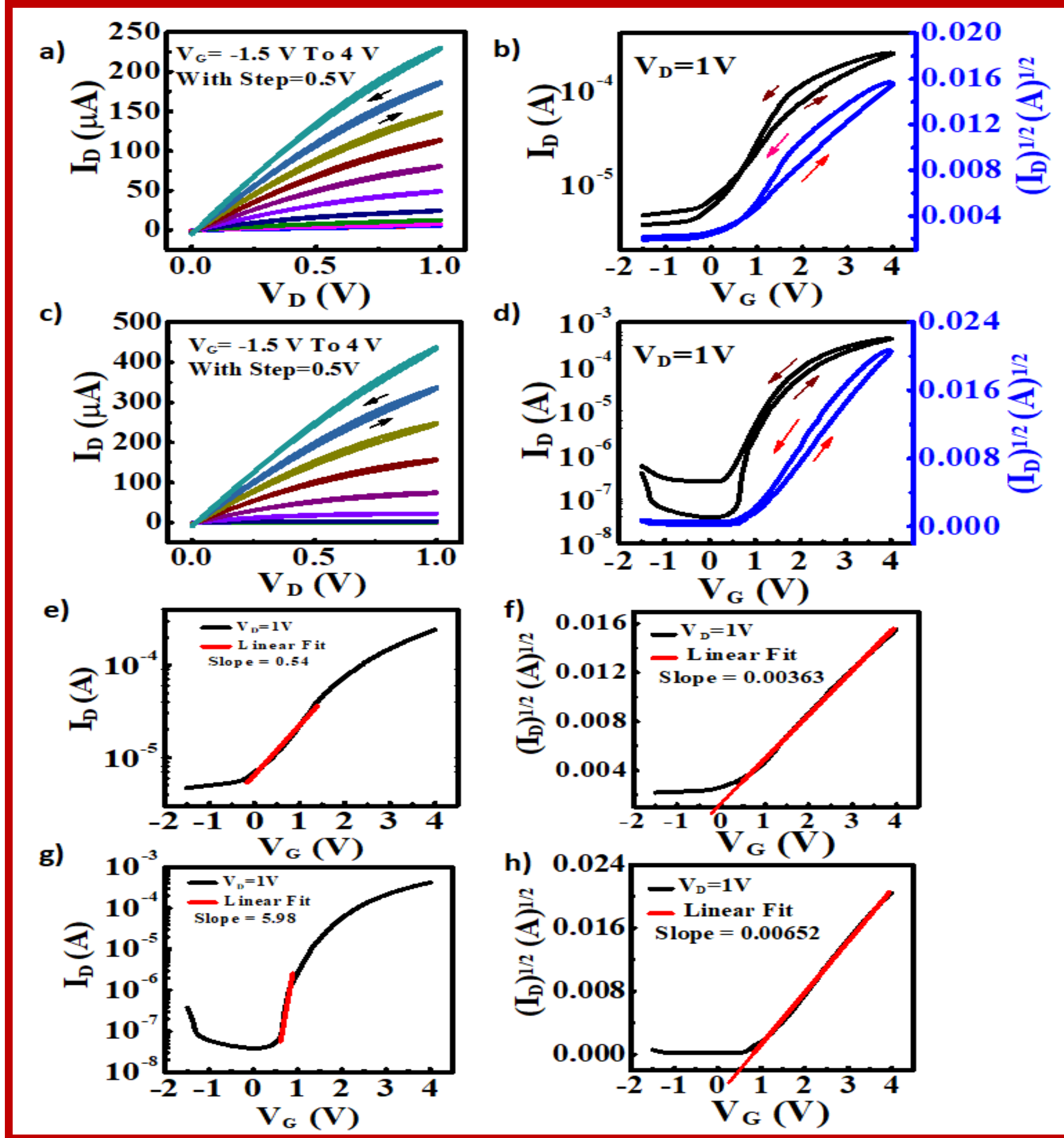

Figure 5.6 *Output (I_D-V_D) characteristics of an n-channel SnO_2 FEFETs with a) LN and c) LA/LN/LA stacked dielectrics, having devices' channel width to length ratio (W/L)=118. Transfer characteristics (I_D-V_G) of the FEFET devices with b) LN and d) LA/LN/LA stacked dielectrics, respectively, measured at constant V_D = 1 V. Linear fit of I_D vs. V_G curves at lower V_G region of FEFETs with e) LN and, g) LA/LN/LA stacked dielectric for SS value calculation. Linear fit of $(I_D)^{1/2}$ vs. V_G curves of devices with f) LN and, h) LA/LN/LA stacked dielectric, respectively for carrier mobility calculation.*

and fro in the voltage range of 0 to 1 V, while the constant gate voltages (V_G) have been increased from -1.5 to 4 V with a step of 0.5 V. The I_D value of device-2 at V_D=1V, with constant V_G = 4V is 438 µA which is higher than device-1 (230 µA). As shown in figures 5.6 a) and c), typical n-channel transistor characteristics have been obtained, having counterclockwise hysteresis. Further, the transfer characteristics (I_D-V_G) of the devices have been illustrated in figure 5.6 b) for device-1 and d) for device-2, respectively. The gate voltage is swept from -1.5 V to 4 V and then returned back to -1.5V at a constant drain voltage of 1V. The counterclockwise hysteresis of the output and transfer characteristics are attributed to the ferroelectric nature of $LiNbO_3$ and LA/LN/LA stacked gate-insulator. All the device parameters like carrier mobility, subthreshold swing (SS), threshold voltage and current ON/OFF ratio of the devices have been extracted from the transfer characteristics. The carrier mobility has been calculated using equation 5.3,

$$\boldsymbol{\mu} = \frac{\left(\frac{\partial\sqrt{\mathbf{I_D}}}{\partial\mathbf{V_G}}\right)^2}{\frac{1}{2}\times\frac{\mathbf{W}}{\mathbf{L}}\times\mathbf{C}} \ldots\ldots\ldots\ldots\ldots..(\mathbf{5.3})$$

where C, I_D, V_G, W, L are areal capacitance of the dielectric, saturation drain current, gate voltage, width and length of the device channel, respectively. The slope of the $(I_D)^{1/2}$ vs. V_G curves has been obtained by linear fitting in straight line regions as shown in figure 5.6 f) for device-1 and h) for device-2. Here, device-2 displays superior carrier mobility of 1.9 $cm^2.V^{-1}.s^{-1}$ over device-1 (0.35 $cm^2.V^{-1}.s^{-1}$). Furthermore, device-2 has a significantly higher current ON/OFF ratio of 1.6×10^4 than device-1 (51). Subthreshold Swing (SS) of TFT device is defined by the equation 5.4

$$\mathbf{SS} = \left[\frac{\partial(\log \mathbf{I_D})}{\partial\,\mathbf{V_G}}\right]^{-1} \dots\dots\dots\dots..(5.4)$$

To calculate the SS value, the slope of the lower region of log (I_D) vs. V_G curve (shown in figure 5.6 e) for device-1 and g) device-2) is selected. The SS value achieved from device-2 is 167 mV.decade^{-1} which is remarkably lower than device-1 (1869 mV.decade^{-1}). Dielectric/semiconductor interface trap state densities of both devices are derived from the SS values using equation 5.5,

$$\mathbf{N_{SS}^{Max}} = \left[\frac{\mathbf{SS} \times \log \mathbf{e}}{\frac{\mathbf{kT}}{\mathbf{q}}} - \mathbf{1}\right]\frac{\mathbf{C}}{\mathbf{q}} \dots.(5.5)$$

where e, k, T, q, C is exponential constant, Boltzmann constant, room temperature, electronic charge, and areal capacitance of the dielectric layer, respectively. The N_{SS}^{Max} value of device-2 is 4.3×10^{12} cm^{-2} and that of device-1 is 1.2×10^{14} cm^{-2}. Additionally, device-1 shows a negative threshold voltage of -0.008 V, where device-2 has a positive threshold value of 0.43 V. All the device parameters are summarized in Table 5.2

Table 5.2 *Summary of the TFT parameters*

Device	Threshold Voltage (V)	ON/OFF ratio	Subthreshold Swing (mV.decade^{-1})	Carrier Mobility (cm^2.V^{-1}.s^{-1})	Interface trap-state density (cm^{-2})
p^{++}-Si/LN/SnO_2/Al	-0.008	51	1869	0.35	1.2×10^{14}
p^{++}-Si/LA/LN/LASnO_2/Al	0.43	1.6×10^{4}	167	1.9	4.3×10^{12}

The log (I_D) vs. V_G plots of the devices with multiple gate voltage ranges have been measured and represented in figure 5.7 a) and d) for device-1 and device-2, respectively. The individual plots of two different voltage ranges have been shown in figure 5.7 b), c), e), and f). It has been

noticed that with the increase of gate voltage range, the OFF current of device-1 increases gradually, thus diminishing the current ON/OFF ratio. As compared to device-1, the OFF current increment of device-2 is much lower, maintaining more or less the same ON current which effectively enhances ON/OFF ratio of the device.

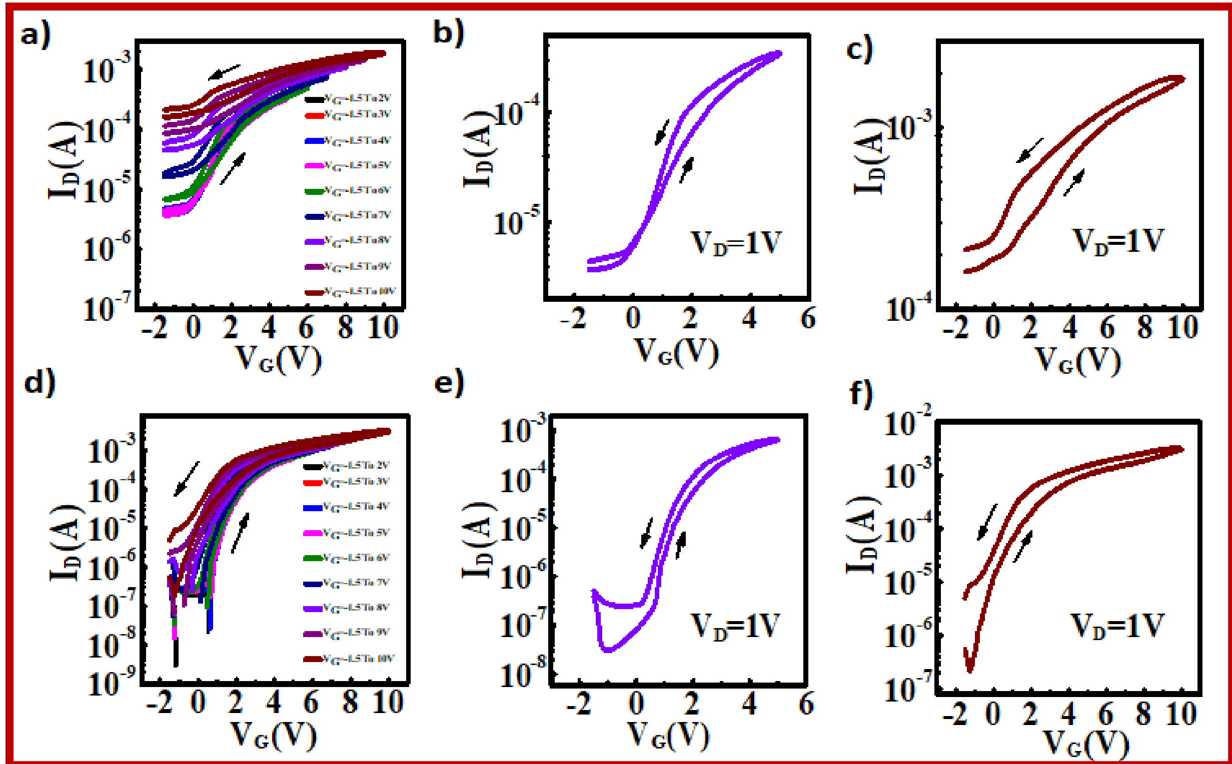

Figure 5.7 *Transfer characteristics of both devices with different gate voltage range keeping constant gate voltage at 1 V. Gate voltage range -1.5 V to various volts for a) LN, d) LA/LN/LA based FEFETs; -1.5 V to 5 V for b) LN, e) LA/LN/LA based FEFETs; -1.5 V to 10 V for c) LN, f) LA/LN/LA based FEFETs, respectively.*

5.2.6 Retention Time

Memory retention characteristics of device-1 and device-2 have been examined by a measurement of the remnant drain current as a function of time shown in figure 5.8 keeping V_D at a constant value of 1 V. The ON and OFF states were generated by applying gate voltage sweep from 0 to7 V and 0 to-2 V, respectively. During retention measurement, $V_G = V_{Hold}$ was kept constant at 0 V. The memory retention with the current ON/OFF ratio of two orders was obtained for device-2 (figure 5.8 a)) and one order for device-1 (figure 5.8 c)) up to 10 minutes. The ON current gradually decreased with time whereas the OFF current maintained the same state for both the devices, but the ON state current change in device-1 is higher compared to device-2. After 2 hours, ON/OFF ratio of device-2 reached about the value of 3 (figure 5.8 b)) while for device-1 the two current states are merged with each other (figure 5.8 d)). In general, semiconductors in contact with ferroelectrics lead to a larger depolarization field than metal because of a weaker screening effect caused by their lower free charge densities and larger dielectric constants.[183] Hence device-1 with only $LiNbO_3$ dielectric is showing poor retention behavior with respect to device-2 with LA/LN/LA sandwiched dielectric.

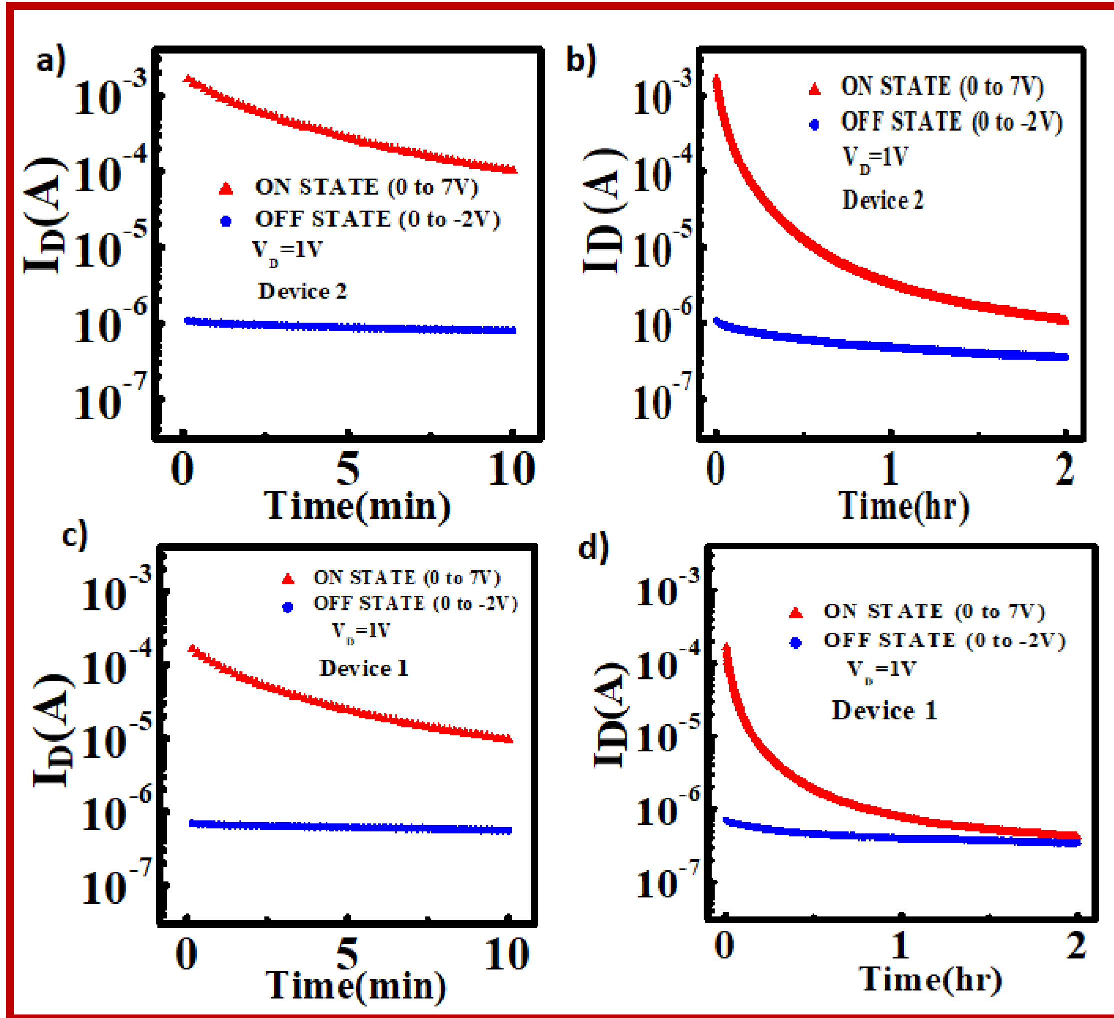

Figure 5.8 *Retention characteristics of FEFET with LA/LN/LA stacked (device-2) and single layer LN (device-1) dielectric, measured by keeping V_G = 0V and V_D = 1 V with time range a) device-2 and c) device-1 for 10 minutes and b) device-2 and d) device-1 for 2 hours . The gate voltage of 7 V and -2 V are applied to achieve the ON and OFF states, respectively.*

The noticeable improvement in the device performance in case of stacked ferroelectric-based TFT (device-2) over device-1 with a single LN ferroelectric layer is mainly because of two reasons. Primarily, with the addition of Li-Al_2O_3 layers sandwiching $LiNbO_3$ ferroelectric, a significant reduction in surface roughness has been achieved which also upgraded the surface

smoothness of the semiconductor layer in TFT, indicating a lower defect formation at the dielectric/semiconductor interface and the bulk film. That reduces carrier scattering during TFT operation which effectively enhances the device performance.

The second factor that comes into play is the reduction of depolarization field and gate leakage current in a stacked dielectric based FEFET. Generally, in a Metal-Ferroelectric-Metal (MFM) geometry, complete charge compensation occurs during the charge polarization of ferroelectric thin film from neighboring metal electrodes. Therefore, no depolarization field exists after inducing polarization in the ferroelectric layer. But, the situation can be different, in case one side of the ferroelectric thin film forms a heterojunction with a semiconductor. Due to less carrier concentration of semiconductor, after charge polarization of ferroelectric thin film, less number of charge accumulate in the semiconductor side that result an incomplete charge compensation.[184] Hence, a depolarization field always appears in a FEFET device where one side of ferroelectric dielectric forms a heterojunction with channel semiconductor, bringing down the device's retention time.[172] Another dominant reason is the gate leakage current. On that account, the intervention of a buffer dielectric layer improves the device performance which can be explained by a band structure model as shown in figure 5.9. Herein, figure 5.9 a) shows the band diagram model of the p^{++}-Si/$LiNbO_3$/SnO_2 device, where $LiNbO_3$ is sandwiched between p^{++}-Si and SnO_2. The carrier concentration of p^{++}-Si is close to metal, whereas semiconducting SnO_2 has a much lower free charge carrier density. This carrier density mismatch creates incomplete charge compensation, thus enhancing the depolarization field within the $LiNbO_3$ layer. At the same time due to the lower bandgap of $LiNbO_3$ ferroelectric, band offset of wide bandgap SnO_2 semiconductor might be less; that leads to significant gate leakage current at applied positive bias. So, device-1 with only $LiNbO_3$ ferroelectric shows poor device

performance and retention time. To the contrary, figure 5.9 b) shows the band diagram model of the p^{++}-Si/Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3/SnO_2 device, where $LiNbO_3$ is sandwiched between two interfacial Li-Al_2O_3 layers. For this case, when a positive gate voltage is applied due to the capacitive effect adjacent Li-Al_2O_3 layer gets polarized by Li^+ movement and induces polarization in the next layers. Here, sandwiched $LiNbO_3$ layer experiences equal charge densities on both sides, resulting in complete charge compensation. Thus, the depolarization effect inside $LiNbO_3$ layer can be reduced largely. Similarly, a larger band offset of Li-Al_2O_3 and SnO_2 ensures fewer charge injections into the ferroelectric layer. Also, the band offset of Li-Al_2O_3 with p^{++}-Si is notably high, which prevents the charge carrier injection from p^{++}-Si to $LiNbO_3$. Subsequently, leakage current is minimized in the case of device-2, boosting overall device performance.

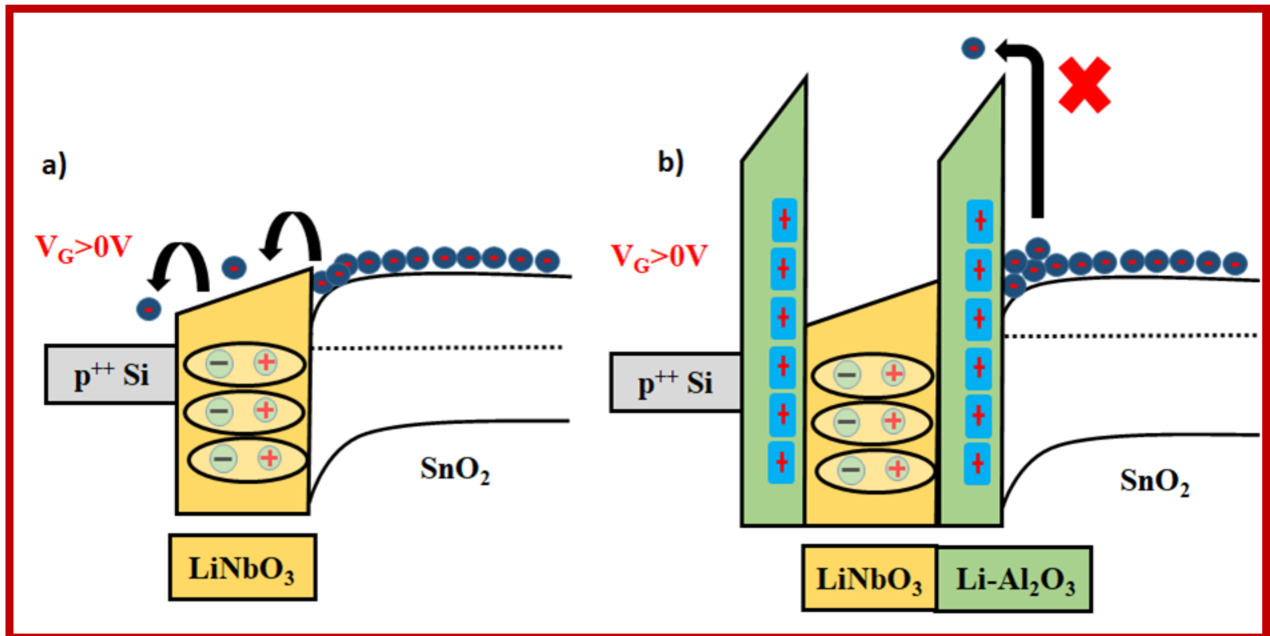

Figure 5.9 *Schematic configurations of Energy Band diagrams for a) p^{++}-Si/$LiNbO_3$/SnO_2 and b) p^{++}-Si/Li-Al_2O_3/ $LiNbO_3$/Li-Al_2O_3/SnO_2 at positive applied gate voltage.*

5.3 Conclusions

In summary, a SnO_2 ferroelectric field-effect transistor (FEFET) has been fabricated with two types of gate dielectric layers. One is single layer $LiNbO_3$ ferroelectric based; another is based on Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. The better device performance has been achieved in terms of high ON/OFF ratio of 1.6×10^4, carrier mobility of 1.9 $cm^2.V^{-1}.s^{-1}$, and SS of 167 $mV.decade^{-1}$ with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric based FEFET. The device also has a longer retention time. The better performance of this device is explained by using a band model of stacked gate dielectric. It is proposed that the intervening of high bandgap ionic Li-Al_2O_3 interfacial layer on both sides of $LiNbO_3$ results complete charge compensation as well as prevents charge carrier injection from p^{++}-Si to SnO_2. These phenomena support the better operation of the FEFET device with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. These findings pave a new avenue for the development of better quality FEFETs with higher retention time.