Chapter 4:

Gate Interface Engineering for Sub-volt Metal-oxide Transistor

Fabrication by Using Ion- conducting Dielectric with Mn_2O_3

Gate Interface

4.1 Introduction

High dielectric constant (κ) thin-film offers high capacitance, which is capable of accumulating a large amount of mobile charge carrier in the dielectric/semiconductor interface of the channel of a thin film transistor (TFT) at a very low gate voltage.[41, 71, 107] This effect lowers the threshold voltage and subthreshold swing of a TFT enabling the device to operate at a lower voltage. Additionally, higher-κ dielectric allows to deposit of a relatively thicker gate dielectric film which reduces gate leakage significantly even after maintaining the high capacitance properties. Such kind of high capacitance gate dielectric enables the reduction of transistor size by avoiding the short channel effect.[107-109] Again, this shortened length allows us to fabricate a higher areal density of logic elements by increasing the TFT density.[107-109] In this competition, conventional SiO_2 dielectric reaches its limit of the shortest channel length suggesting a new search for reliable high-κ dielectric. Different dielectric materials have been developed to replace SiO_2 including inorganic, polymer, and electrolyte materials. Among inorganic materials, Al_2O_3, HfO_2, ZrO_2, TiO_2, $ZrTiO_x$, $SrTiO_3$, etc., have been widely investigated.[107-110] Besides these inorganic oxide materials, ultrathin dielectric and several electrolytes, including ion-gel, liquid electrolytes, and solid inorganic electrolytes, have been utilized as high-κ dielectric of TFT.[109, 111-114] Both gas-phase and solution processes have been employed to grow high-κ dielectric thin films. The most utilized gas-phase methodologies are chemical vapor deposition (CVD), atomic layer deposition (ALD), sputtering, pulsed laser deposition (PLD), and e-beam evaporation.[107, 115, 116] However, for large area/roll-to-roll

fabrication, low-cost deposition techniques like spin-coating, spray coating, inkjet printing, and gravure printing have been investigated. Among them, solution-processed electrolyte materials take advantage of mobile ions to fabricate extraordinarily high capacitive thin film, which is required to develop low operating voltage TFT.[117-123] Such electrolytes, including ion-gel, liquid electrolyte, and solid inorganic electrolyte, have been successfully utilized for different classes of low voltage TFT.[91, 101, 114, 117-125] However, most of these approaches can reduce operating voltage up to 2.0 V. To develop a sub-volt operating voltage TFT, further modification of device architecture is required to reduce the density of dielectric/semiconductor interface states significantly. Technically, it is possible to reduce the sub-threshold swing (SS) of a TFT significantly by keeping the threshold voltage closer to zero.

In this chapter, a high-performance and sub-volt (< 1 V) operating voltage oxide TFT fabrication has been described. Transistor has been fabricated using ITO substrate combined with a sol-gel derived ion-conducting dielectric and tin oxide (SnO_2) semiconductor. One of the key findings of this work is the enhances of the carrier mobility and lowers the operation of TFT by utilization of sol-gel derived high permittivity manganese (III) oxide (Mn_2O_3) as an interface layer between the gate electrode and gate dielectric Throughout this chapter, entire sol-gel processes have been performed at or below 550°C, which is compatible with any glass substrate. The role of the Mn_2O_3 gate interface in lowering the operating voltage of TFT and improving device performance with possible mechanisms has been discussed in the following section. To the best of my knowledge, fabrication of sub-volt metal oxide TFT by solution-processed technique is not reported earlier.
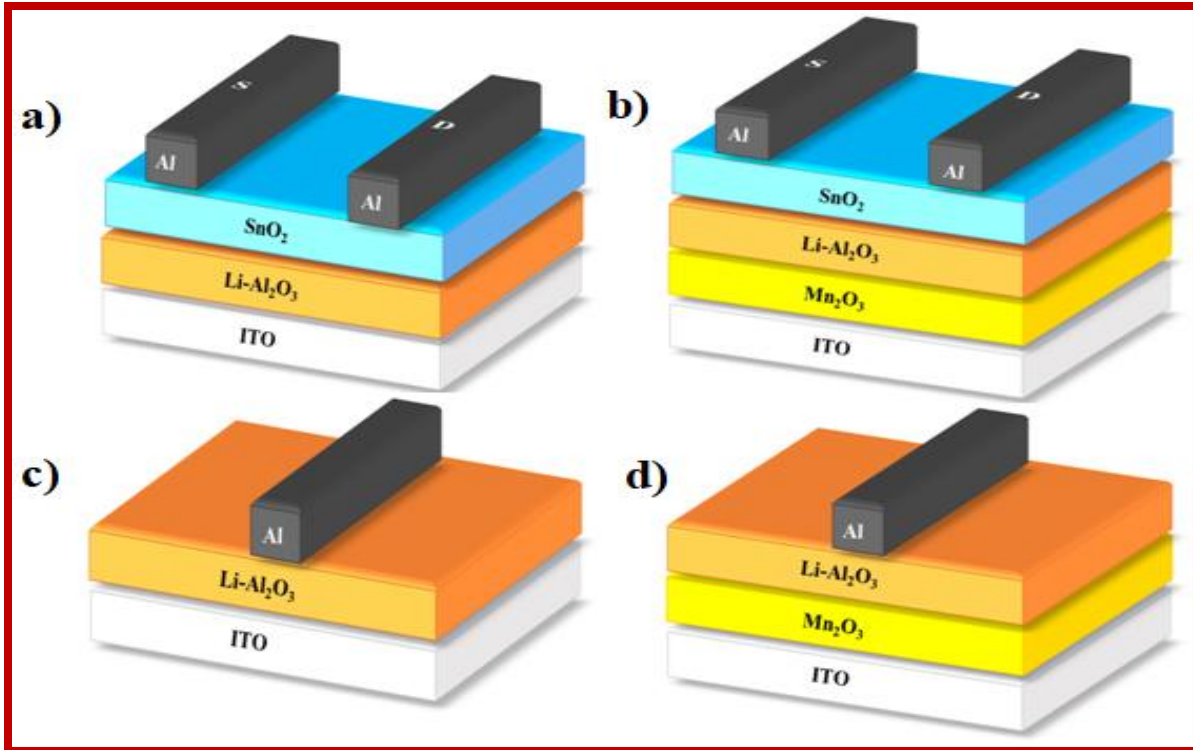
Figure 4.1 *Schematic diagram of the device structures of a) device-1 (without Mn_2O_3 gate interface), b) device-2 (with Mn_2O_3 gate interface), c) MIM device without Mn_2O_3, d) MIM device with Mn_2O_3.*

4.2 Result and discussions

4.2.1 Powder XRD and GIXRD characterizations of Mn_2O_3

For X-ray powder diffraction analysis, the sample was prepared by annealing the powder precursor samples. In contrast, for the grazing incidence XRD (GIXRD) study, samples were prepared on a p^{++}-Si substrate in identical conditions used for TFT fabrication. Figure 4.2 a) shows the powder XRD pattern of manganese oxide. The major reflection peaks are indexed as the crystal planes of (211), (222), (400), (332), (431), (440), (611), (541), (622), (631), and (721) of Mn_2O_3.[126] This data indicates that the annealing at 550°C in an ambient environment forms the Mn_2O_3 phase only. Annealing at 550°C for 30 minutes shows thermo-chemical changes in

the peak positions. Although, the GIXRD study shows (figure 4.2 b)) only the two most intense

peaks that are indexed as the crystal planes of (222) and (440) of Mn_2O_3[127, 128].
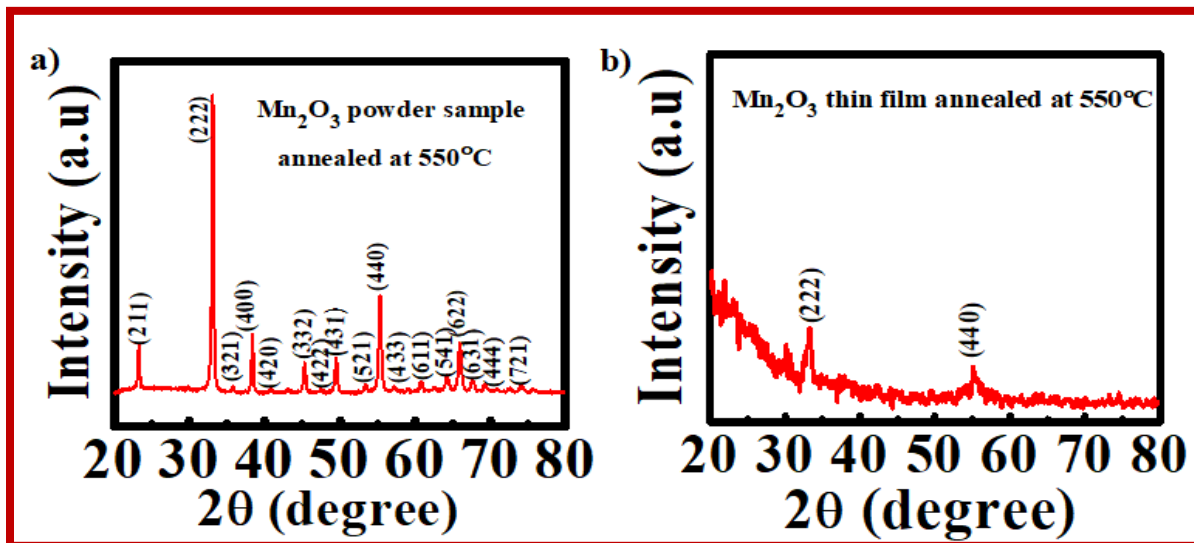

Figure 4.2 a) XRD patterns of Mn₂O₃ powder sample, and b) GIXRD patterns of Mn₂O₃ thin film annealed at 550°C.

4.2.2   X-ray photoemission spectroscopy (XPS) of Mn_2O_3

X-ray photoemission spectroscopy (XPS) study was conducted to investigate the chemical

oxidation state of the elements present in Mn_2O_3 thin film. A survey scan of the Mn_2O_3 film

annealed at 550°C is shown in figure 4.3 a) within the binding energy range of 0 – 1400 eV

revealed the absence of any impurity except carbon contamination. The binding energy levels of

Mn 3p, Mn 3s, Mn 2p, O 1s, C 1s, and auger peaks are shown in figure 4.3 a) agree well with

previously reported values[129, 130]. Figure 4.3 b) and c) shows the binding energy spectra of

Mn 3s and Mn 2p respectively. These Mn 2p and Mn 3s peaks are broad due to multiple

splitting. The multiple splitting energies of the Mn 3s spectra are 89.44 eV and 83.89 eV with a

separation of 5.55 eV. This peak splitting is caused by the coupling of non-ionized 3s electrons with 3d valence-band electrons. This splitting of spectra is proportional to the remaining electron in the 3s orbital and the other unpaired electrons, which have parallel spins. The energy difference of this spitting indicates the particular oxidation state of Mn. In this case, it originated due to the Mn^{3+} state that confirms the formation of the Mn_2O_3 phase.[131] A Satellite peak is present in Mn 2p spectra at a binding energy of 664.13 eV which is 10.59 eV higher than that of $2p_{1/2,}$ reconfirming the presence of the Mn^{3+} oxidation state [131]. In addition, the purity of Mn_2O_3 is further analyzed by considering the binding energy of O 1s spectra located at 529.81 eV (figure 4.3 d)). This binding energy value is also in good agreement with the literature data[126]. Peaks appearing at a binding energy of 529.81 eV and 531.58 eV in O 1s spectra correspond to Mn-O-Mn and Mn-OH. The presence of the –OH group in O 1s XPS spectra stems from the absorption of moisture by Mn_2O_3.

4.2.3   UV-Vis absorption studies of thin films

For transmittance study, thin films of Mn_2O_3 and $Li-Al_2O_3$ were fabricated on quartz substrate under the same conditions followed in TFT dielectric fabrication. The Mn_2O_3 thin film shows the transparency (figure 4.4 a)) of 70 to 75% in the visible range and relatively higher transparency of 85% in the NIR region (900 nm). Comparatively, $Li-Al_2O_3$ thin film is more transparent, with transparency of over 85% in the entire visible and NIR region (figure 4.4 b)). Optical band gaps of Mn_2O_3 and $Li-Al_2O_3$ have been extracted from absorption coefficient data. According to the theory, the relation between optical absorption, the absorption coefficient (α), and photon energy (hν) are given by

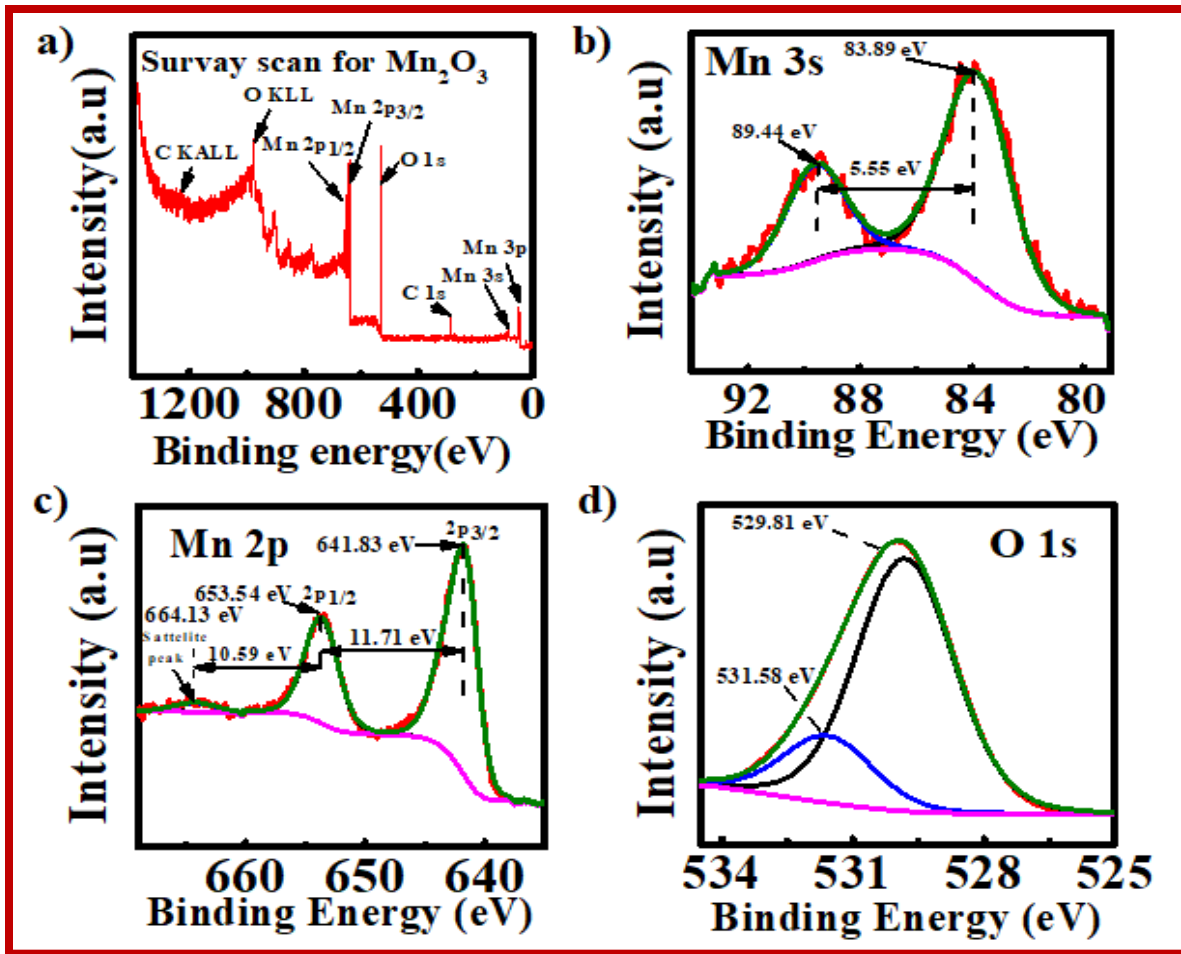$$\alpha = \frac{A(h\nu - E_g)^n}{h\nu} \quad .... \quad (4.1)$$

Figure 4.3 *XPS spectra of the different elements present in Mn₂O₃ thin film a) survey scan b) Mn 3s and c) Mn 2p states and d) O 1s allocated to Mn-O-Mn (~ 529.81 eV) and Mn-O-H (~ 531.58 eV) of Mn₂O₃ thin film sample annealed at 500°C.*

where A and n are constants, for direct allowed transition n =1/2 and indirect allowed transition n=2.[132] Figures 4.4 c) and 4.4 d) show the variation of $(\alpha h v)^2$ with photon energy (hv). The straight-line nature of both graphs (figures 4.4 c) and d)) indicates the direct band gaps of the two materials. The optical band gap of Mn_2O_3 and $Li-Al_2O_3$ has been extracted by extrapolating the straight line of $(\alpha h v)^2$ vs. hv plot yielding the values of 3.36 eV and 5.70 eV, respectively. These optical band gaps of Mn_2O_3 and $Li-Al_2O_3$ are consistent with the earlier reports.[133-135]
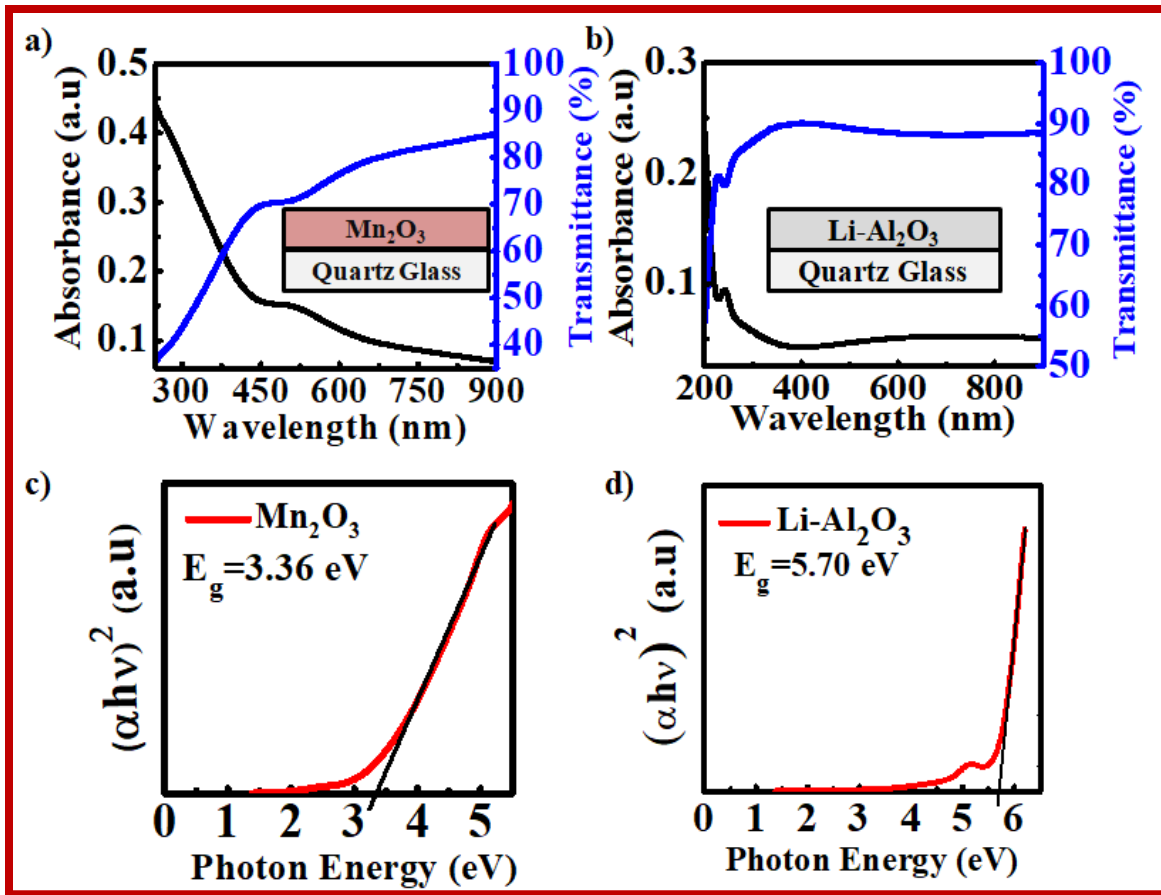
Figure 4.4 Optical absorption and transmittance spectra of the solution-processed a) Mn_2O_3 and b) $Li-Al_2O_3$ thin films annealed at 550°C and 500°C, respectively. Tauc plot ($(\alpha h\nu)^2$ vs. h\nu) of c) Mn_2O_3 and d) $Li-Al_2O_3$ show direct allowed transition with optical band gap 3.36 eV and 5.70 eV, respectively.

4.2.4 Surface morphologies of different thin films

The surface morphologies of $Li-Al_2O_3$ and $Mn_2O_3/Li-Al_2O_3$ bilayer dielectric thin films have been studied by atomic force microscopy (AFM) and micrographs of different dielectrics have been shown in figure 4.5. All these thin films have been deposited on an ITO-coated glass substrate precisely under the exact condition of TFT fabrication. The study indicates that the deposited Mn_2O_3 thin film is relatively smooth with a root mean square roughness (R_{rms}) of 0.56

nm (figures 4.5 a) and d)), which is slightly higher than that of Li-Al$_2$O$_3$ thin films (R$_{rms}$ = 0.28

nm), as displayed in figures 4.5 b) and e). The AFM image of Mn$_2$O$_3$/Li-Al$_2$O$_3$ (figures 4.5 c)

and f)) indicates that the R$_{rms}$ roughness of this film is 0.74 nm which is a bit higher than that of

the individual films. However, the roughness of all these films is below 1.0 nm, which is a good

indication of forming a lower amount of trap state dielectric/semiconductor interface.
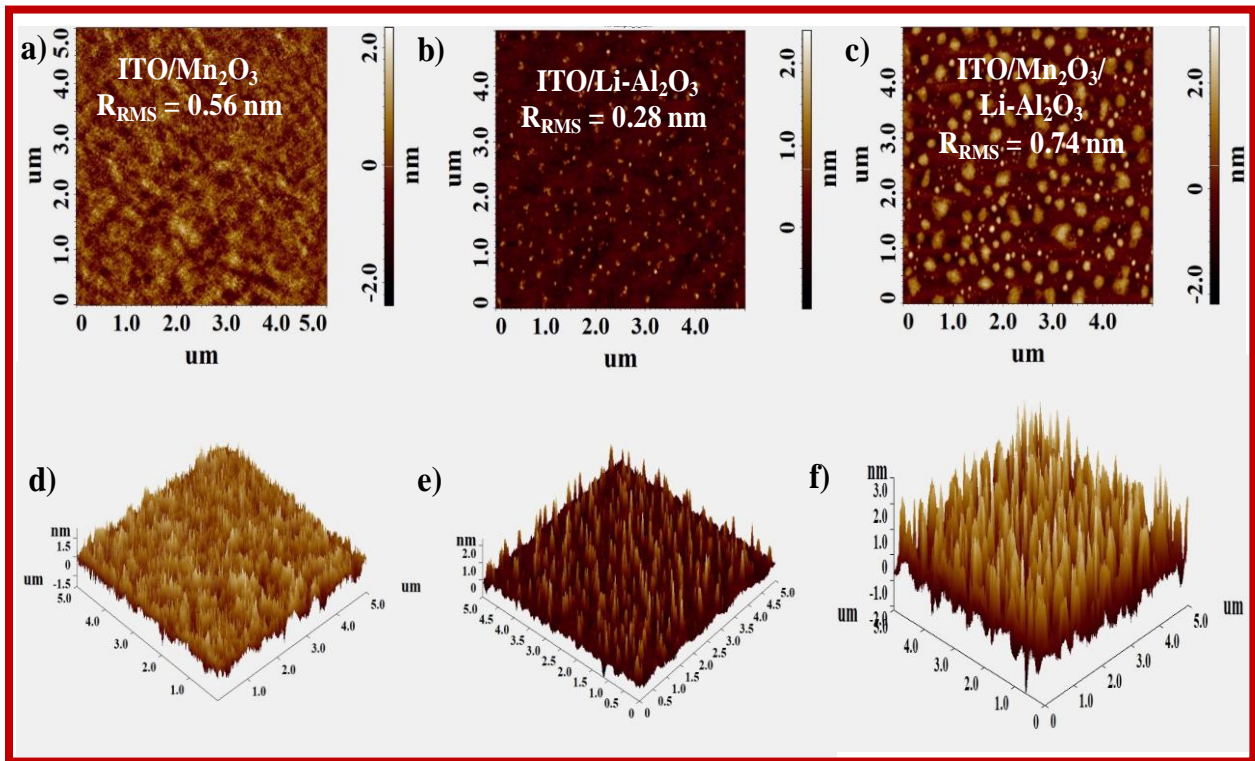

Figure 4.5 Two dimensional AFM images of a) Mn$_2$O$_3$, b) Li-Al$_2$O$_3$, and c) Mn$_2$O$_3$/Li-Al$_2$O$_3$ thin

film on ITO. Three dimensional AFM images of d) Mn$_2$O$_3$ (R$_{rms}$ ~ 0.56 nm), e) Li-Al$_2$O$_3$ (Rrms ~

0.28 nm), and f) Mn$_2$O$_3$/Li-Al$_2$O$_3$ (R$_{rms}$ ~ 0.74 nm) thin film on ITO.

4.2.5   Cross-sectional SEM of TFT device

Figure 4.6 shows the cross-sectional image of device-2 on an ITO-coated glass substrate. The average thickness of Mn_2O_3 dielectric and SnO_2 semiconductor layers are 20 nm, 94 nm, and 18 nm, respectively.
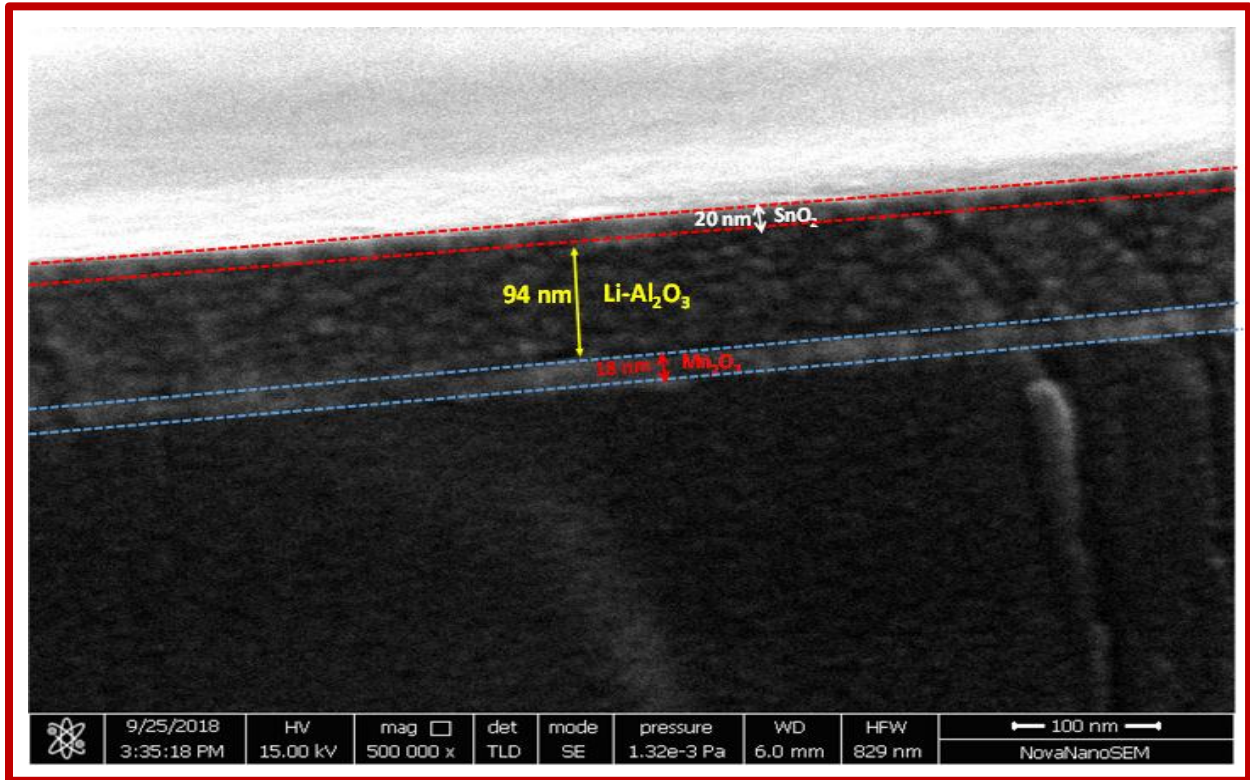

Figure 4.6 *Cross-sectional SEM image of device-2 with a device structure of ITO/Mn_2O_3/Li-Al_2O_3/SnO_2/Al.*

4.2.6   Variation of capacitance with frequency and current density with applied field (or voltage) of different dielectric films

The capacitance and current density of various gate dielectric thin films have been measured with the geometry of ITO/dielectric/Al. Schematics of those devices without and with Mn_2O_3 layer are shown in figures 4.1 c) (MIM device-1) and d) (MIM device-2), respectively. Dielectric

thin films have been deposited under the same conditions followed in the TFT fabrication. The capacitance behavior of those dielectric thin films in different frequencies (20 Hz -10^5 Hz) has been shown in figure 4.7 a). The capacitances of the dielectric with and without Mn_2O_3 are 611.4 nF.cm^{-2} and 327 nF.cm^{-2} at 50 Hz, respectively. Capacitance values of these two dielectric thin films decrease with frequency, attributed to the lack of surface polarization due to Li$^+$ at a higher frequency. Still, the change in capacitance with frequency in MIM device-2 is more significant concerning MIM device-1. Mn_2O_3 has a high intrinsic dielectric constant (> 2500 below 1 kHz), which is much higher than Li-Al_2O_3.[136] Therefore, by including the Mn_2O_3 layer, the overall capacitance value increases in the lower frequency range.[137] However, there are two opposing sides to Mn_2O_3. One of them is its very high frequency-dependent dielectric constant which decreases with frequency rapidly. On the other hand, Mn_2O_3 is not an excellent insulator to use as a gate dielectric of TFT. Therefore, using the Mn_2O_3 layer, overall capacitance increases at lower frequencies, but it decreases rapidly at higher frequencies which are not suitable for the high-frequency application. Although, it helps us very significantly to lower the operating voltage of the device by improving other device parameters of TFT. Considering the film separation (d) of Mn_2O_3/Li-Al_2O_3 and Li-Al_2O_3 thin film as 114 nm and 94 nm respectively, the dielectric constant (κ) of these films has been calculated from the following equation

$$C = \frac{C}{A} = \frac{k\epsilon_0}{d} \dots \dots \dots \dots \dots \dots (4.2)$$

where ϵ_0 is the dielectric constant of the vacuum. Using the thickness data of dielectric thin film, equation 4.2 gives the effective dielectric constants of Mn_2O_3/Li-Al_2O_3 and Li-Al_2O_3 thin film of 79 and 35, respectively.

The same set of devices has been used to measure current density vs. applied field (or voltage) characteristics. The current density vs. electric field plot has been demonstrated in figure 4.7 b), which indicates that the bilayer dielectric is stable up to the field of $\sim$ 2.2 MV.cm^{-1} and is high enough for the safe application of this TFT. Figure 4.7 c) shows the variation of current density with the applied voltage for two different dielectric thin films. It is observed from figure 4.7 c) that the current density of Mn_2O_3/Li-Al_2O_3 thin film is $\sim$ 50 times lower than that of the Li-Al_2O_3 only dielectric. The current density of Mn_2O_3/Li-Al_2O_3 bilayer dielectric is 0.15 μA.cm^{-2} at 10 V, which is good enough for low voltage TFT fabrication. The capacitance per unit area, dielectric constant, and current density of these films have been summarized in Table 4.1.
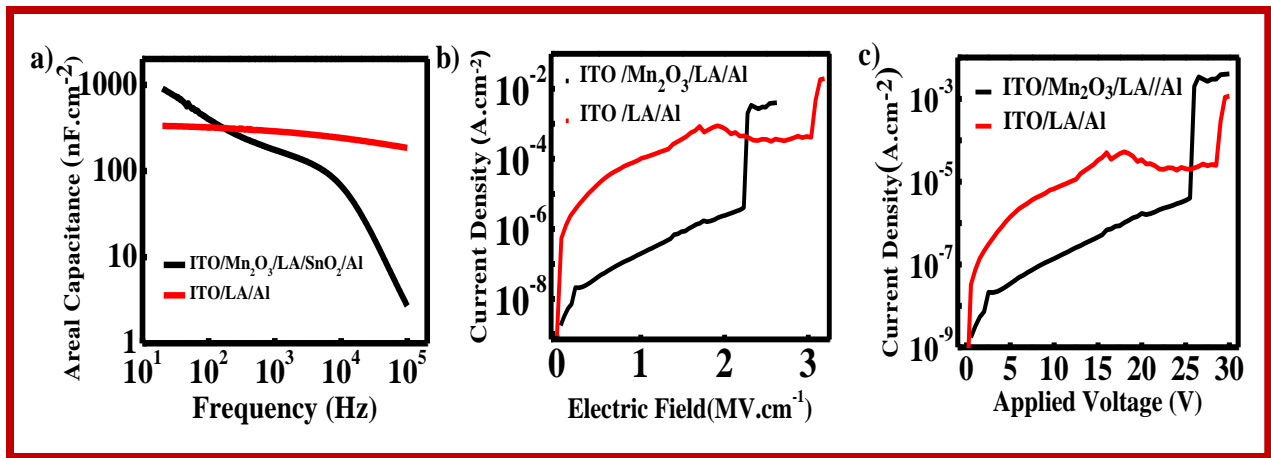

Figure 4.7 *Variation of a) capacitance vs. frequency, b) current density vs. the applied field, c) current density vs. applied voltage of Li-Al$_2$O$_3$ and Mn$_2$O$_3$/Li-Al$_2$O$_3$ gate dielectric with MIM device architecture.*

Table 4.1 *Current densities, areal capacitance, and dielectric constants of dielectric films.*

Dielectric	C (nF.cm^{-2}) (at 50 Hz)	Dielectric constant (at 50 Hz)	Current density (μA.cm^{-2})
Li-Al$_2$O$_3$	327.7	35	7.12
Mn$_2$O$_3$/Li-Al$_2$O$_3$	611.4	79	0.15

70

4.2.7 TFT device characterization:

The TFT characteristics have been investigated using SnO_2 n-channel active semiconductor layer with two different types of dielectrics as shown in figures 4.1 a) and b). Figure 4.8 a) shows the output characteristics of SnO_2 transistor with Li-Al_2O_3 only gate dielectric. This comparative study indicates the linear and saturation region within a drain voltage range of 2.0 V, where the gate voltage was varied from -0.5 V to 4.5 V. However, this TFT shows a very high threshold voltage (V_T) with a value of 2.5 V and an ON/OFF ratio of 3×10^3 as shown in figure 4.8 c). In contrast, a remarkable improvement of this TFT has been made using the Mn_2O_3 interface. The output (I_D-V_D) and transfer (I_D-V_G) characteristics of this TFT is shown in figure 4.8 b) and d). Figure 4.8 b) shows that the device requires a drain voltage (V_D) of $\sim$ 0.6 V to saturate the drain current when V_G is varied from -0.2 to 1.0 V. The threshold voltage is reduced to 0.28 V which is one order lower than that of the device-1, and ON/OFF ratio increases to 3.5×10^4 as shown in figure 4.8 d). Comparing the characteristics of device-1 and 2, it can be noted that device-1 has a relatively higher gate leakage current. However, Mn_2O_3/Li-Al_2O_3 bilayer stacked dielectric shows a lower leakage current, which is due to the very different grain size and conductivity of Li-Al_2O_3 and Mn_2O_3. Lowering leakage current by using bilayer stack dielectric has been studied earlier in several literatures.[138, 139] Carrier mobility (μ), sub-threshold swing (SS), and dielectric/semiconductor interface trap sate of these TFTs are calculated from the following equations respectively[6]

$$I_D = \mu C \frac{W}{2L} (V_G - V_T)^2 \ldots\ldots\ldots\ldots (4.3)$$

$$SS = \left[\frac{\partial(\log I_D)}{\partial V_G} \right]^{-1} \ldots\ldots\ldots\ldots\ldots\ldots\ . (4.4)$$

$$N_{SS}^{Max} = \left[\frac{SS \times \log e}{\frac{kT}{q}} - 1 \right] \frac{C}{q} \quad \ldots\ldots (4.5)$$

where I_D, C, V_G, and V_T are saturation drain current, capacitance per unit area, gate voltage, and threshold voltage, respectively. Since the TFT operation was performed in direct voltage, the capacitance at a low frequency (50 Hz) is considered for mobility calculation to avoid overestimation. The channel length and width of these TFTs are 23.6 mm and 0.2 mm, respectively, with a W/L ratio of 118 used to calculate saturation mobilities of charge carriers in the devices. The field effect mobility of charge carriers of both devices is extracted using equation 4.3. To prevent overestimation of the mobility value due to non-ideal transfer characteristics of practical thin film transistor, we derived the slope from the fitting of experimental data in the linear regime of the square root of I_D vs. V_G according to the earlier report (shown in figures 4.8 e) for device-1 and f) device-2)).[140] The higher electron mobility of 17 $cm^2.V^{-1}.s^{-1}$ has been achieved for the device with Mn_2O_3 interfaced dielectric. This value is higher than that of the $Li-Al_2O_3$-only gate dielectric TFT that shows the mobility of 15 $cm^2.V^{-1}.s^{-1}$. However, the key improvement of the Mn_2O_3 interfaced device is the operating voltage of less than 1.0 V compared to the 2.0 V of other devices. This improvement became possible due to the low SS (defined by equation 4.4) value of device-2. For calculation of SS value, the slopes are determined from log (I_D) vs. V_G graphs shown in figure 4.8 g) and h) for device-1 and device-2, respectively. The estimated SS values that are extracted from the transfer characteristics of device-1 and device-2 are 413 $mV.decade^{-1}$ and 124 $mV.decade^{-1}$, respectively. Using these SS

values, dielectric/semiconductor interface-states-density has been calculated from equation 4.5. The extracted interface-state-density (N_{ss}^{max}) of device-2 is 4.1×10^{12} cm^{-2} which is around three times lower than that of device-1. The device parameters of both transistors have been summarized in Table 4.2.

Table 4.2 Key parameters of SnO$_2$ TFTs with and without Mn$_2$O$_3$ gate interface

Device	Dielectric	Carrier mobility [cm^2.V^{-1}.s^{-1}]	ON/OFF ratio	Threshold voltage [V]	Subthreshold Swing [mV.decade^{-1}]	Trap state Density [cm^{-2}]
Device-1	Li-Al$_2$O$_3$	15	3.0×10^3	2.55	413	1.2×10^{13}
Device-2	Mn$_2$O$_3$/Li-Al$_2$O$_3$	17	3.3×10^4	0.28	124	4.1×10^{12}

Such distinguishable improvement of TFT with the Mn$_2$O$_3$ interface may have two possible reasons. One can be the very low surface roughness of Mn$_2$O$_3$/Li-Al$_2$O$_3$ dielectric film. Since higher roughness in the dielectric/semiconductor interface causes considerable carrier scattering in the channel layer and creates interfacial trap states.[141-143] However, comparative AFM studies of both dielectric surfaces indicate that both dielectrics have similar roughness with a root-mean-square value below 1 nm and should not give a big difference between them. Therefore, there are certainly some other reasons behind this distinct improvement which can be attributed to the interface trap density of dielectric/semiconductor interfaces. To identify the origin of the advancement of lowering the operating voltage and device performance due to the additional Mn$_2$O$_3$ gate interface layer, a model has been proposed based on the relative energy band of the device, which is illustrated in figure 4.9.
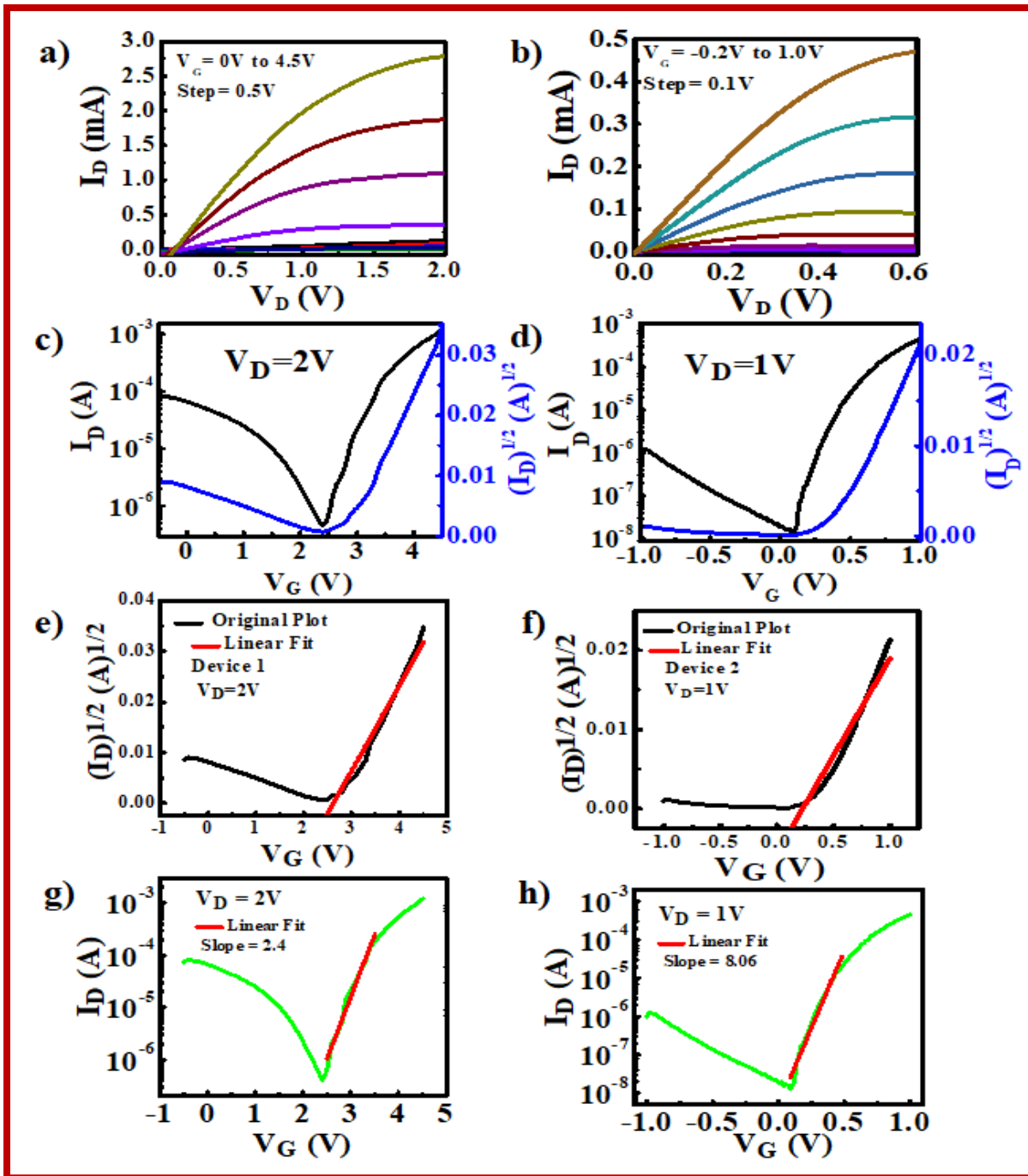
Figure 4.8 *Typical a) output, c) transfer characteristics of device-1 and b) output, d) transfer characteristics of device-2. Linear fit of $(I_D)^{1/2}$ vs. V_G plot for e) device-1 and f) device-2 to extract the slope for charge carrier mobility calculation. Log (I_D) vs. V_G plot for g) device 1 and h) device 2 to determine the slope for subthreshold swing (SS) calculation.*

Due to the presence of the Mn_2O_3 interface in device-2, charge carriers can be induced to the interface of the channel that can fill the interface states and can effectively enhance the charge accumulation at a specific positive gate voltage. This phenomenon can be realized in figure 4.9 a), which depicts ITO/Mn_2O_3 interface as a Schottky junction. Therefore, at zero gate bias, electrons get transferred to the gate electrode (ITO), leaving a positive charge layer in Mn_2O_3 film (black arrow). Under accumulation mode operation, Mn_2O_3 film accumulates more positive charge resulting in the accumulation of the additional electrons in the channel and consequently high drain current under accumulation mode operation (figure 4.9 b)). In contrast, the case of device-1 has a relatively higher density of interface trap states in the $Li-Al_2O_3/SnO_2$ interface that originated from the free-drifting of Li^+ on the dielectric surface. The trap-states are not filled up at zero applied bias due to the absence of earlier phenomena that appeared in the case of the ITO/Mn_2O_3 interface (figure 4.9 c)). Under accumulation mode operation, initially, electrons fill all those trap states (figure 4.9 d)). They require a relatively higher voltage to accumulate mobile charges in the channel, effectively introducing a large threshold voltage for the device. Moreover, this higher density of interface states introduces a more significant subthreshold swing of the device (equation 4.4). Therefore, drain current (I_D) requires more drain voltage (V_D) to saturate. Thus, an additional Mn_2O_3 layer on ITO induces extra electrons to accumulate in the dielectric/semiconductor interface, effectively inducing additional electrons to the accumulation layer of the channel, enabling us to fabricate high-performance sub-volt TFT.[81]
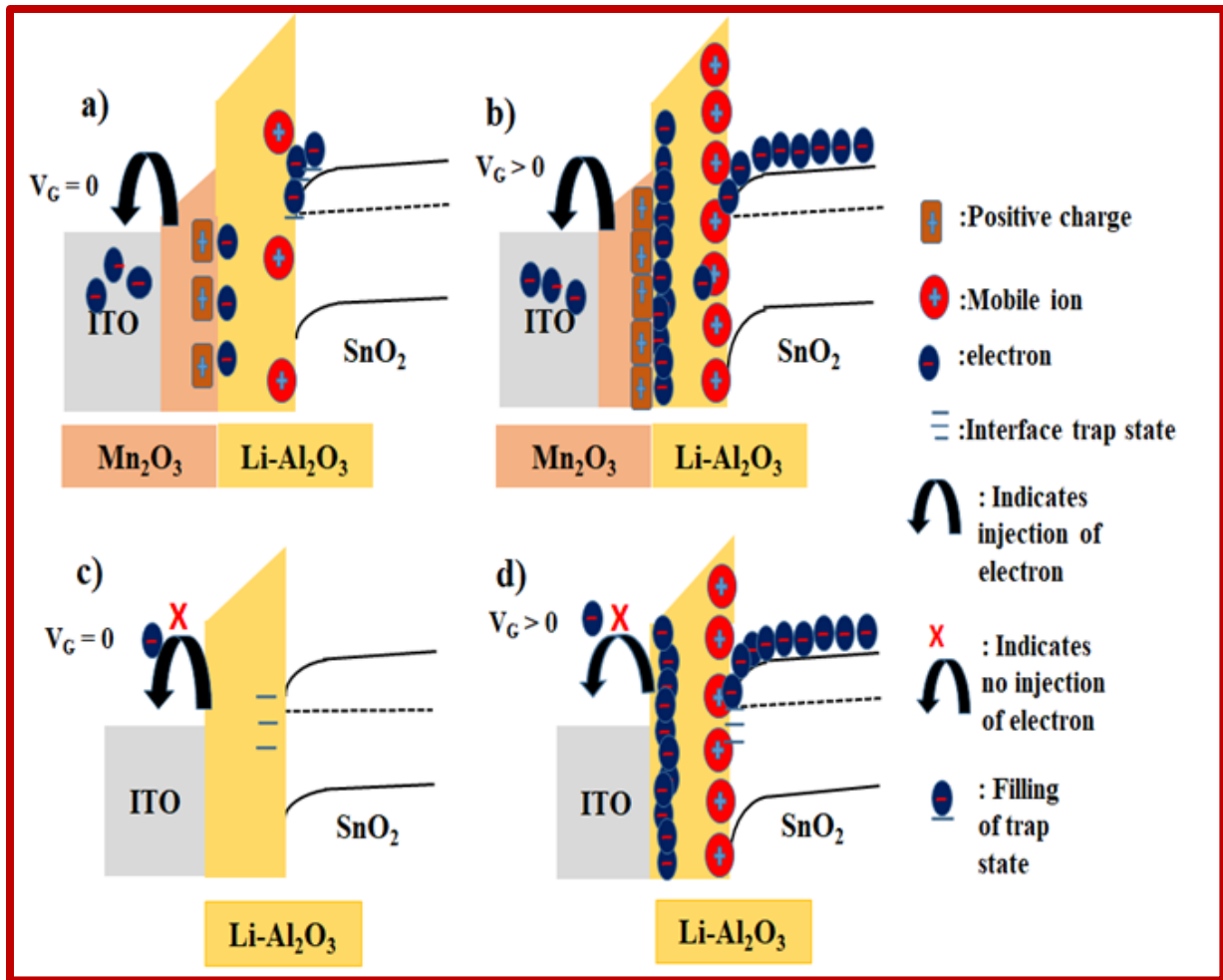
Figure 4.9 *Energy band diagram of the Mn_2O_3/Li-Al$_2$O$_3$ dielectric film a) under zero and b) positive gate bias. Energy band diagram of Li-Al$_2$O$_3$ dielectric film c) under zero gate bias d) under positive gate bias.*

4.3 Conclusions

In conclusion, a high-performance solution-processed sub-volt tin oxide thin-film transistor (TFT) has been fabricated onto a sol-gel derived ion-conducting gate dielectric by utilizing a Mn_2O_3 gate interface. A comparative device characterization of two different TFTs with and without Mn_2O_3 gate interface reveals that Mn_2O_3 induces additional electrons to the

dielectric/semiconductor interface trap states that essentially reduce the threshold voltage and subthreshold swing of the device. Moreover, the depletion layer of the ITO/Mn$_2$O$_3$ interface reduces gate leakage current significantly, which helps to improve the ON/OFF ratio of the device. Again, by inserting a high-κ Mn$_2$O$_3$ layer between the Li-Al$_2$O$_3$ gate dielectric and the gate electrode, a high capacitance of the dielectric film has been achieved that helps to get current saturation at lower gate bias. Such sub-volt TFT with an additional Mn$_2$O$_3$ layer in gate dielectric exhibited electron mobility of 17 cm^2.V^{-1}.s^{-1}, ON/OFF ratio of 3.3×10^4, and sub-threshold swing of 124 mV.decade^{-1}. This investigation suggests a new feasible direction for developing high-performance, sub-volt TFT fabrication by selecting proper material combinations for gate dielectrics.