Chapter 3:

Solution Processed Low Voltage Metal-Oxide Transistor by using TiO_2/Li-Al_2O_3 stacked Gate Dielectric

Chapter-3

3.1 Introduction

The charge carrier conduction of the channel of a thin film transistor (TFT) typically occurs within < 10 nm thickness of the semiconductor film next to the gate-dielectric.[89] Therefore, the field-effect charge transport phenomena of a TFT is not only dependent on the microstructures of the semiconductor but is also strongly affected by the surface properties of the gate-insulator.[90] Conventional silicon dioxide gate dielectric (SiO_2) commonly offers smooth surface morphology capable of minimizing the defect density of the semiconductor-insulator interface. However, the dielectric constant of SiO_2 is very low (3.9). Therefore, to reduce the operating voltage of a TFT below 2 V for portable electronics applications, it requires a very low thickness of SiO_2 (< 10 nm) which sometimes becomes very leaky.[12] Employment of high-κ dielectric materials instead of SiO_2 is the best alternative which allows us to deposit thicker dielectric film by maintaining the advantage of low operating voltage TFT fabrication.[41, 73, 91-93] However, ionic bonds in high-κ dielectrics result in high defect concentrations with oxygen vacancies (V_O) being the primary source of traps. These can be sources of fixed charges or act as electron traps that decrease the effective carrier mobility of the device. Moreover, these trap states change the threshold voltage (V_T) of the device and increase the gate-leakage current,[94] decreasing device performance and stability. To overcome these problems different approaches such as inorganic-organic hybrid dielectrics,[95] multicomponent dielectric,[96] bilayer-dielectric stack,[81, 97, 98] composite solid polymer electrolyte (CSPE),[99] have been used. Many of these dielectrics are solution-

processable and can be printed by different printing techniques.[100] To reduce the semiconductor/dielectric interface trap states, recently, a new method has been developed by implying n-type TiO_2 as an interface layer between highly doped silicon (p^{++}-Si) substrate and high-κ ion conducting Li_5AlO_4 dielectric, which drastically enhance the TFT device performance due to the formation of Schottky junction of p^{++}-Si/TiO_2. However, capacitance of that Li_5AlO_4/TiO_2 stacked dielectric reduces rapidly above the frequency 10^4 Hz.[101] To enhance the frequency range and overall performance of TFT, more detailed study is required for different combinations of the stacked dielectric.

In this chapter, Li-doped alumina (Li-Al_2O_3) thin film has been synthesized by the sol-gel method and used this ionic dielectric to fabricate TiO_2/Li-Al_2O_3 stacked gate dielectric. The variation of areal capacitance of this bilayer stacked gate dielectric reduces only by 20% up to the frequency of 10^5 Hz. To realize the overall improvement of TFT performance and the mechanism of this development, two sets of solution-processed SnO_2 TFT were fabricated; one with a TiO_2 gate interface and another without a gate interface. Comparative studies of these two TFTs reveal a significant improvement in device performance in the TiO_2 interface device. A schematic presentation of the energy band gap of multilayer thin films and related charge transfer of p^{++}-Si/TiO_2 Schottky junction explains the probable reason for enhancing device performance.

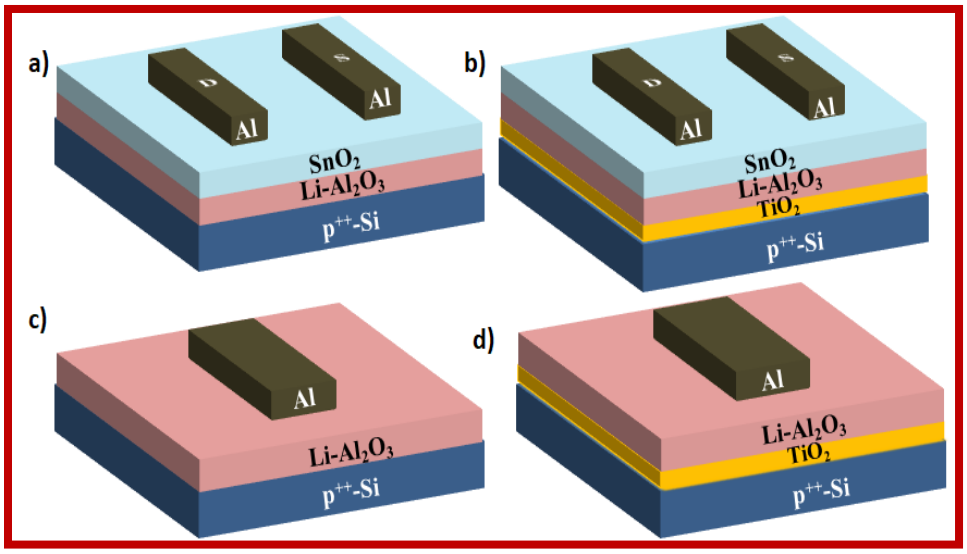

Figure 3.1 *Schematic diagrams of TFT devices, a) device-1 with single layer Li-Al_2O_3 gate-dielectric, b) device-2 with bilayer TiO_2/Li-Al_2O_3 gate-dielectric. MIM devices with c) Li-Al_2O_3 gate-dielectric and d) TiO_2/Li-Al_2O_3 gate-dielectric.*

3.2 Results and discussions

3.2.1 Grazing Incidence X-Ray Diffraction Pattern of Thin Films

To analyze the structural properties of spin-coated TiO_2, Li-Al_2O_3, and SnO_2 thin film, individually, all these thin films were deposited on the p^{++}-Si substrate under the same condition of TFT fabrication. Figure 3.2 a) shows the GIXRD patterns of TiO_2 thin film which indicates a crystalline peak at $2\theta \sim 25.28°$, which corresponds to the (101) plane of the stable anatase phase of TiO_2. The GIXRD patterns of Li-Al_2O_3 dielectric which is shown in figure 3.2 b), did not show any diffraction peak, indicating the amorphous nature of Li-Al_2O_3 dielectric.

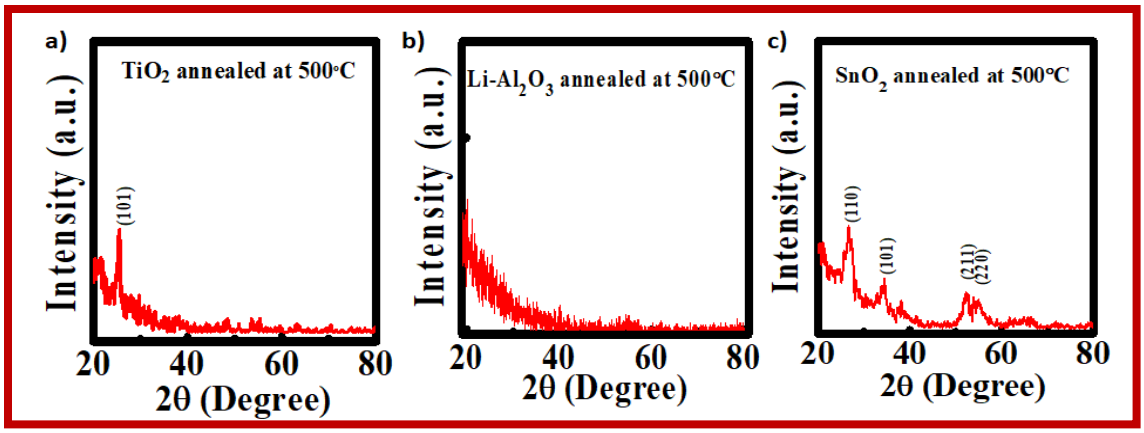

Figure 3.2 *The GIXRD patterns of a) TiO_2, b) Li-Al_2O_3 dielectric, and c) SnO_2 semiconductor layer annealed at 500°C.*

The GIXRD pattern of SnO_2 thin film has been shown in figure 3.2 c) that identified diffraction peaks at the 2θ angle 26.6°, 34.2°, 52.7°, and 54.7°, which correspond to the reflection planes of (110), (101), (211) and (220) respectively; justify the tetragonal phase of SnO_2 (JCPDS 88-0287).

3.2.2 Surface Morphologies of Thin Films

The surface morphologies of single layer Li-Al_2O_3 and bilayer TiO_2/Li-Al_2O_3 dielectrics were studied by atomic force microscopy (AFM). All these dielectric layers were deposited on p^{++}-Si substrates with the same conditions as TFT fabrication. The 2-D and 3-D morphologies of these two dielectric thin films are shown in figures 3.3 a), b), e), and f). Figure 3.3 a) and e) represent the AFM images of Li-Al_2O_3 dielectric whereas; figure 3.3 b) and f) are AFM pictures of TiO_2/Li-Al_2O_3 dielectrics. This study shows that the RMS roughness of both dielectric thin films is < 1 nm which is suitable for high-performance TFT fabrication. However, compared to the bilayer TiO_2/Li-Al_2O_3 surface (0.46 nm); the single-layer Li-Al_2O_3 surface (0.26 nm) is

smoother. Similarly, an AFM study has been performed on SnO_2 thin film deposited on single and bilayer dielectrics shown in figure 3.3 c), d), g), h), indicating their roughness below 1 nm.

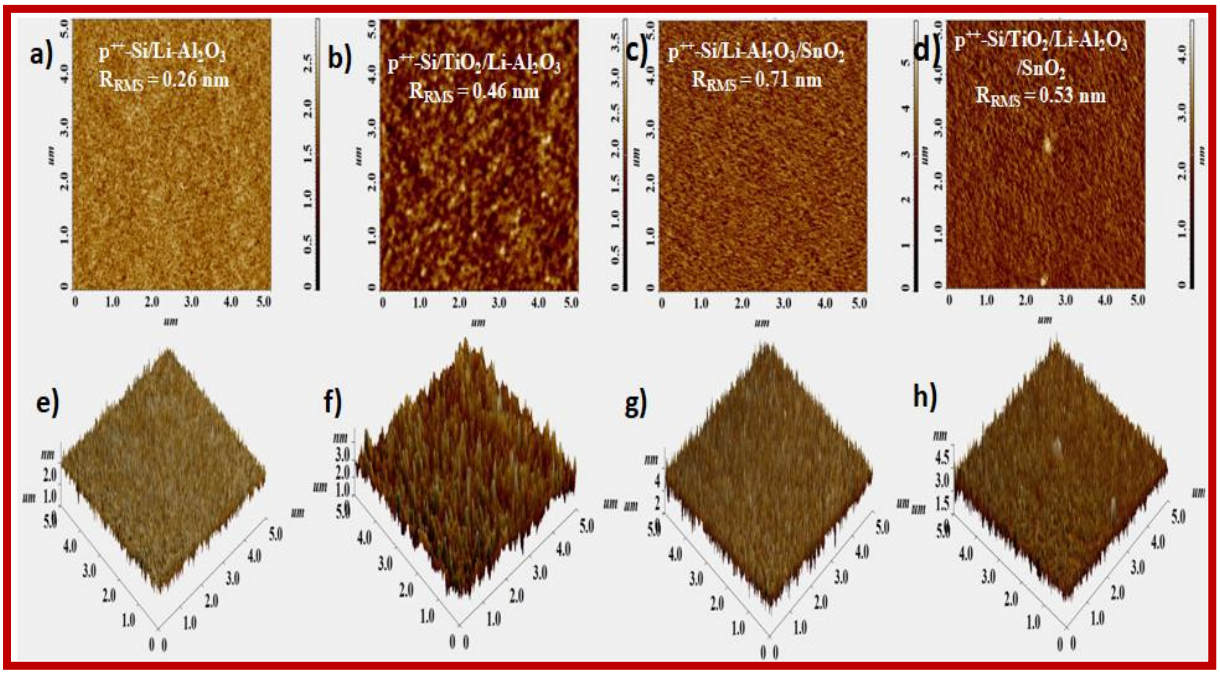

Figure 3.3 *2D AFM images of a) Li-Al_2O_3 and b) TiO_2/Li-Al_2O_3 dielectric. 3D AFM images of e) Li-Al_2O_3 and f) TiO_2/Li-Al_2O_3 dielectric. 2D AFM image of SnO_2 thin film on c) Li-Al_2O_3 and d) TiO_2/Li-Al_2O_3 dielectric. 3D AFM image of SnO_2 thin film on g) Li-Al_2O_3 and h) TiO_2/Li-Al_2O_3 dielectric.*

3.2.3 Dielectric and Electrical characterization

The leakage current density and areal capacitance of single-layer and bilayer dielectric are measured with metal-insulator-metal (MIM) architecture (figures 3.1 c) and d)) which is shown in figure 3.4. The variation of capacitance per unit area of the same set of MIM devices with frequencies (20 to 10^5 Hz) at room temperature is represented in figure 3.4 a). It is well known that the capacitance decreases with frequency due to the different relaxation times originating from different types of polarization contribution.[41] Similar behavior is observed in both types

of MIM devices that reduce significantly > 10^3 Hz. However, the capacitance of the single-layer p^{++}-Si/Li-Al_2O_3/Al device changes more rapidly compared to the bilayer p^{++}-Si/TiO_2/Li-Al_2O_3/Al MIM device. The measured areal capacitance (C) values of single and bilayer MIM devices are 55 nF.cm^{-2} and 66 nF.cm^{-2} at 50 Hz frequency, respectively. This study is the indication of the higher areal capacitance value with a broader frequency range of a bilayer stacked dielectric thin film which originated from an additional TiO_2 layer. The high-κ value of the TiO_2 layer increases the capacitance of TiO_2/Li-Al_2O_3 dielectric with respect to the Li-Al_2O_3 single layer.

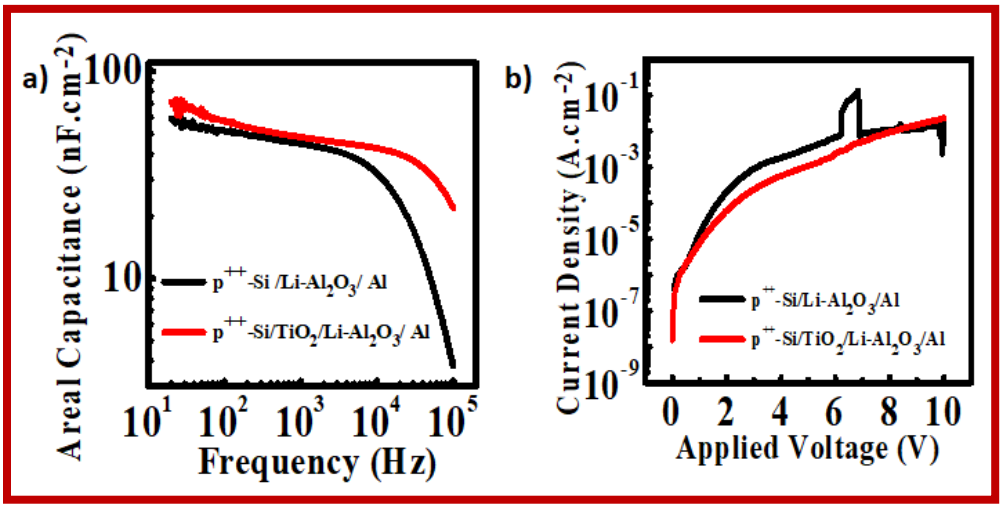

Figure 3.4 *Variation of a) areal capacitance with frequency and b) current density with applied voltage for p^{++}-Si/Li-Al_2O_3/Al and p^{++}-Si/TiO_2/Li-Al_2O_3/Al MIM devices.*

Figure 3.4 b) shows the current density vs. applied voltage graphs of both dielectric thin films. This data indicates that the stacked dielectric of the p^{++}-Si/TiO_2/Li-Al_2O_3/Al device has one order lower current density than the p^{++}-Si/Li-Al_2O_3/Al device at applied voltage 2 V with a current density of 6.2×10^{-5} A.cm^{-2} whereas single layer dielectric MIM device shows a current density of 2.0×10^{-4} A.cm^{-2} at 2.0 V. The dielectric-DC conductivity of bilayer film is reasonably

low for TFT fabrication that operates within 2.0 V operating voltage. The reduction of dielectric-DC conductivity in the case of bilayer dielectric may result from the lattice mismatch of two different materials with different grain shapes at the interfaces, which is well understood from the earlier multilayered dielectric studies.[98]

3.2.4 Electrical Characterization of Single and Bilayer Dielectric Thin Film Transistor

To realize the performance of these dielectric layers for the application of gate dielectric of TFTs, two sets of devices have been fabricated. Device-1 is the reference TFT without a TiO_2 gate interface (figure 3.1 a)) and device-2 is TFT with a TiO_2 gate interface (figure 3.1 b)) in between the gate electrode and Li-Al_2O_3 gate-dielectric. A higher channel length of 200 μm with a W/L (W=23.6 mm, L= 0.2 mm) ratio of 118 is chosen to avoid overestimating carrier mobility value due to grain boundary effect, which is highly dominating below 25 μm channel length and W/L ratio of 10.[102, 103] Additionally, high-performance TFT with a larger device area demands good dielectric quality with pinhole-free uniform thin film with very low defect states. Figure 3.5 shows transistor characteristics of two types of devices and are measured at ambient conditions. The I_D-V_D characteristics of device-1 and device-2 are shown in figures 3.5 a) and b), respectively. The applied V_D is swept from 0 to 1V with different constant gate voltages ranging from -0.2 to 2.0V with a step of 0.2V. The linear and saturation region of the output characteristics are clearly shown in figures 3.5 a) and b) for both sets of devices.

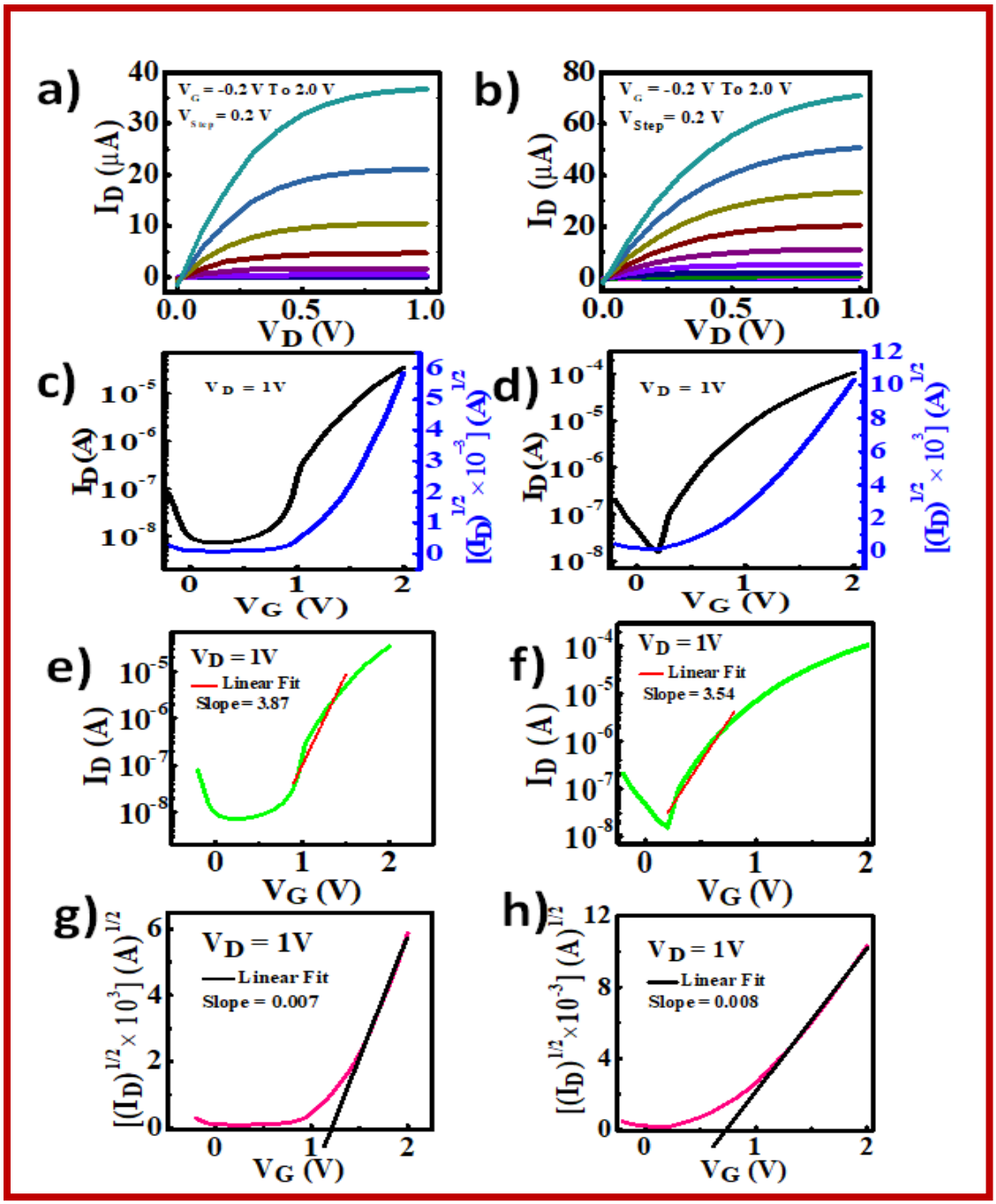

Figure 3.5 *Transistor characterizations of single-layer and bilayer gate-dielectric SnO_2 TFT. a) and b) output characteristics; c) and d) transfer characteristics; e) and d) linear fit of log (I_D) vs. V_G curve to extract SS value; g) and h) linear fit of $(I_D)^{1/2}$ vs. V_G to extract carrier mobility of device-1 and device-2, respectively.*

The Transfer characteristics of SnO_2 TFT without and with TiO_2 interface are shown in figures 3.5 c) and d). The gate to source voltages is swept from -0.2 to 2 V, keeping V_D constant at 1 V for both devices. All the measurement conditions and parameters are kept the same for all devices. From comparative data of transfer characteristics (figure 3.5 e) and f)), it is observed that the threshold voltage of device-2 (0.73 V) is sufficiently lower than device-1 (1.2 V). Besides, the calculated value of the ON/OFF ratio for device-2 is 7.2×10^3 which is higher than device-1 (i.e., 3.6×10^3). The carrier mobility (μ), subthreshold swing (SS) and dielectric/semiconductor interface trap-states (N_{SS}^{Max}) of TFT have been calculated by using the following equations[6]

$$\mathbf{I_D = \mu C \frac{W}{2L}(V_G - V_T)^2} \quad \ldots\ldots\ldots\ldots\ldots (\mathbf{3.1})$$

$$\mathbf{SS = \left[\frac{\partial(\log I_D)}{\partial V_G}\right]^{-1}} \quad \ldots\ldots\ldots\ldots\ldots (\mathbf{3.2})$$

$$\mathbf{N_{SS}^{Max} = \left[\frac{SS \times \log e}{\frac{kT}{q}} - 1\right]\frac{C}{q}} \ldots\ldots (\mathbf{3.3})$$

where k, T, and q are the Boltzmann constant, the temperature in absolute scale, and the charge of an electron, respectively. The saturation carrier mobility of both devices is calculated by using equation 3.1 and extracted from the linear fitting of $(I_D)^{1/2}$ vs. V_G plot (figure 3.5 g) and h)). From the comparison of both devices, it is observed that device-2 shows better performance having electron mobility of 16.4 $cm^2.V^{-1}.s^{-1}$ than device-1 that shows electron mobility of 16.1 $cm^2.V^{-1}.s^{-1}$. The subthreshold swing (SS) values of both devices are extracted from the slope at the lower gate-voltage regime of the log (I_D) vs. V_G graphs (shown in figures 3.5 e) and f)) and

by using equation 3.2. Device-2 has lower SS value (250 mV.decade^{-1}) than device-1 (280 mV.decade^{-1}). The dielectric-semiconductor interface trap-state densities have been derived from equation 3.3. Device-1 has a 1.5 times higher interface trap-state density than device-2. The lower N_{SS}^{Max} leads to less trapping of charge carriers in the dielectric-semiconductor interface, resulting in improved effective mobility and higher drain current.[104] All the TFT parameters are summarized in Table 3.1.

Table 3.1 *Summary of the TFT parameters of SnO_2 transistors with single-layer and bilayer stack gate-dielectrics.*

Device	**Threshold Voltage (V)**	**ON/OFF ratio**	**Subthreshold Swing (mV.decade^{-1})**	**Carrier Mobility (cm^2.V^{-1}.s^{-1})**	**Interface trap-state density (cm^{-2})**
Si^{++}/Li-Al_2O_3/SnO_2/Al	1.2	3.6×10^3	280	16.1	1.6×10^{12}
Si^{++}/TiO_2/Li-Al_2O_3/SnO_2/Al	0.73	7.2×10^3	250	16.4	1.1×10^{12}

To understand the reason behind the higher performance of device-2 with TiO_2/Li-Al_2O_3 stack dielectric, a schematic diagram of energy bands of two types of SnO_2 TFTs has been illustrated in figure 3.6. Since p^{++}-Si (111)/TiO_2 interface forms a Schottky junction at zero gate bias, the electron of the TiO_2 layer transferred to the p^{++}-Si gate-electrode creates a depleted layer of positive charge at the TiO_2 thin film. However, a hole cannot transfer from p^{++}-Si to the TiO_2 layer due to a large potential barrier in the p^{++}-Si (111)/TiO_2 interface.[105, 106] Hence, the layer of the positive charge of TiO_2 thin film induces electrons of the channel of TFT (SnO_2) to accumulate at the Li-Al_2O_3/SnO_2 interface, which initially fills up the electron trap-states (N_{SS}^{Max}) at the dielectric/semiconductor interface (figure 3.6 a)).

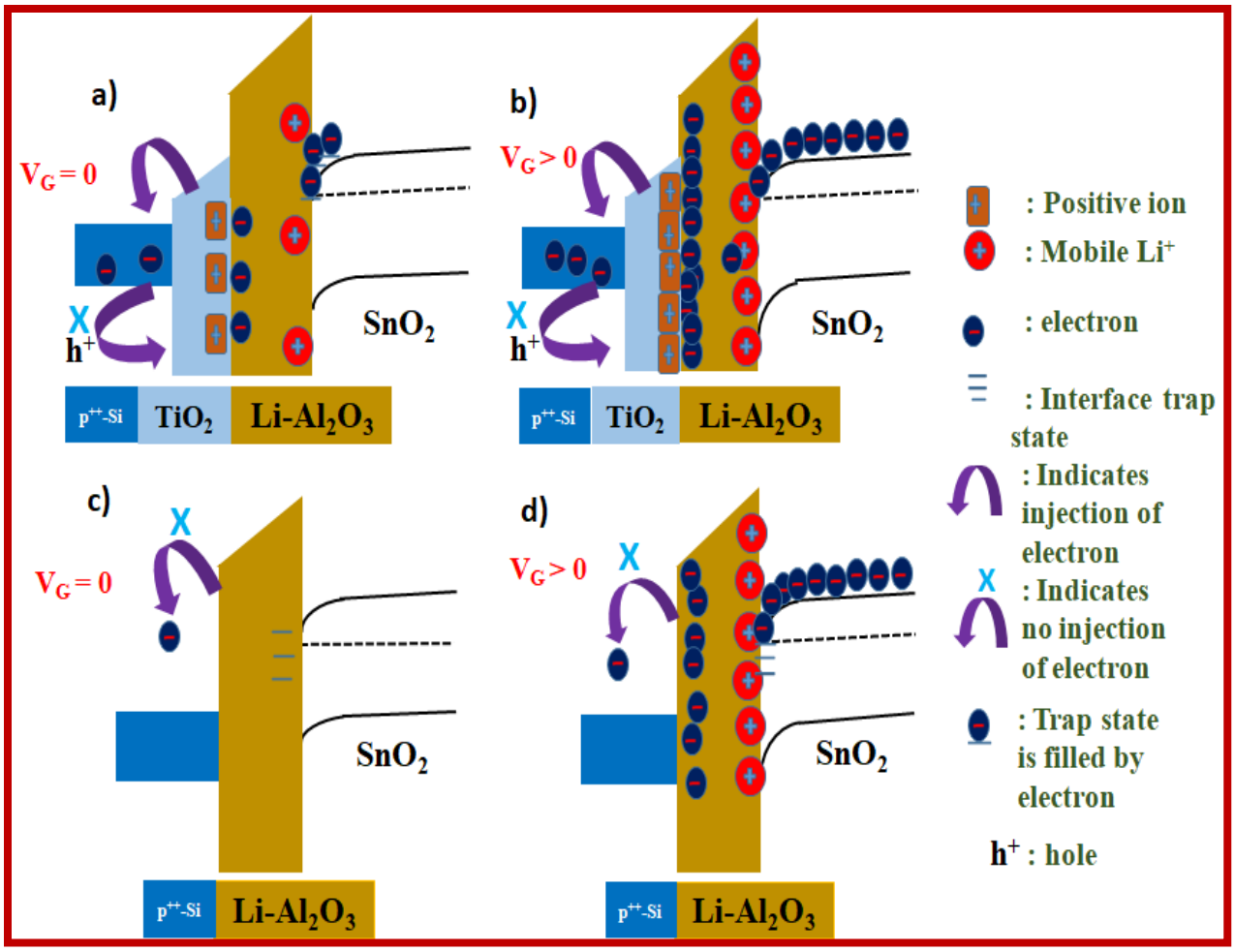

Figure 3.6 *Metal-Insulator-Semiconductor structures illustrating the mechanism of variation in transistor performances with single-layer and bilayer dielectric stack. Energy band diagram of a) and c) without applied bias, and b) and d) with an applied positive bias of device-2 with bilayer TiO_2/Li-Al_2O_3 dielectric and device-1 with single layer Li-Al_2O_3 dielectric, respectively.*

This phenomenon is happening without gate bias. Therefore, TiO_2 thin film effectively reduces the interface trap-states, resulting in a lower subthreshold swing and threshold voltage. Although, this phenomenon is not occurring in device-1 because of the high barrier height of the insulating Li-Al_2O_3 layer. Therefore, electrons cannot be ejected from Li-Al_2O_3 to the p^{++}-Si gate-electrode

(figure 3.6 c)). Under accumulation mode operation, a positive gate voltage is applied to both devices (figure 3.6 b) and d)). However, this bias does not change the depletion layer width of the p^{++}-Si (111)/TiO_2 interface due to the intermediate insulating Li-Al_2O_3 layer. This phenomenon effectively enhances the accumulation of mobile charge carriers in the channel of device-2 which improves the device performance over device-1.

3.3 Conclusions

In conclusion, high-performance solution-processed low operating voltage SnO_2 thin-film transistors have been fabricated onto sol-gel derived ion-conducting Li-Al_2O_3 dielectric by using a TiO_2 gate interface. Comparative studies of two sets of SnO_2 TFTs with and without TiO_2 interface have been demonstrated. The Schottky junction formation between p^{++}-Si and n-type TiO_2 help to accumulate extra electrons at the Li-Al_2O_3/SnO_2 interface, which essentially fills up the interface trap-states and reduces the sub-threshold swing (SS) as well as threshold voltage (V_T) and enhance the saturation carrier mobility of the device with compared to the device without TiO_2 interface. The high-κ value of TiO_2 improves the capacitance of the TiO_2 /Li-Al_2O_3 stack dielectric as well as its leakage current is also reduced compared to single-layered Li-Al_2O_3 dielectric. We have achieved carrier mobility (μ) of 16.4 $cm^2.V^{-1}.s^{-1,}$ SS of 250 $mV.decade^{-1}$, and V_T of 0.73 V in TiO_2/Li-Al_2O_3 stack TFT with an ON/OFF ratio of 7.2×10^3. This investigation opens a new path to developing high-performing TFT devices by using a suitable bilayer stack of gate-dielectrics.