Chapter 2

Experimental Part: Materials Synthesis, characterization & Device fabrication

Chapter-2

In this chapter, different methods of experimentation like materials synthesis, material characterization, device fabrication process, and electrical characterization of devices, which are used in this thesis work, have been discussed. In the material synthesis section, three types of materials synthesis methods have been described, and these materials are ion-conducting oxide dielectric, a metal oxide semiconductor, and ferroelectric oxide materials. Material characterization includes various bulk material and thin film characterizations. The device fabrication part consists of MIM and TFT fabrication. At the same time, electrical characterization includes current vs. voltage (I-V), capacitance vs. frequency (C-f), current vs. time (I-t), and polarization vs. electric field (P-E) measurement.

2.1 Materials Synthesis

In this thesis work, three different kinds of metal oxides have been synthesized via the low-cost sol-gel method. These are i) ion-conducting oxide dielectric, ii) metal-oxide-semiconductor, and iii) metal oxide ferroelectric materials. The ion-conducting oxide insulator act as a gate-dielectric in TFT fabrication. Various kinds of metal oxide semiconductors have been synthesized for different purposes. TiO_2 and Mn_2O_3 have been used for the interfacial layer between the gate dielectric and gate electrode, and the a-C layer as an interface between semiconductor and gate dielectric; well-known n-type metal-oxide-semiconductor SnO_2 has been used as the active channel layer of the TFTs. Metal oxide ferroelectric like $LiNbO_3$ has been used as a gate-dielectric in FEFET fabrication. The solution technique allows the materials to react equally on a

molecular level, resulting in a single compound amorphous/polycrystalline thin film. In most of the precursor sol preparation of synthesis we used metal salts dissolved in alcohol. Thin film of different dielectric, semiconductors and interface layers are fabricated by spin coating followed by an annealing process. A brief description of these materials synthesis is given below.

2.1.1 Synthesis of Li-Al_2O_3 ion-conducting gate-dielectric precursor solution

Li-Al_2O_3 has been synthesized via a low-cost sol-gel method and used as a gate dielectric. For the synthesis of Li-Al_2O_3 dielectric, Lithium acetate [CH_3COOLi] and Aluminum nitrate nonahydrate [Al $(NO_3)_3$, $9H_2O$] have been used as precursor salts. Initially, an alumina salt has been dissolved to make a 500 mM precursor solution in 2-methoxy ethanol and stirred for about 60 minutes with the help of a magnetic stirrer. Similarly, 500 mM Lithium acetate salt has been dissolved in a mixed solvent of 2-methoxy ethanol and water (10:1 volume ratio) and stirred for 60 minutes to get a clear solution. Then these two solutions are mixed, maintaining Li: Al volume ratio of 1:11, and half a molar amount of acetylacetone has been added as a stabilizer. The mixed solution is stirred vigorously for about 6 hours and aged at least 24 hours for proper gelation.

2.1.2 Synthesis of TiO_2 and Mn_2O_3 precursor solution

A thin layer of TiO_2 metal-oxide-semiconductor has been used as a gate-interface layer between the gate electrode and dielectric. A 100 mM precursor sol of TiO_2 has been prepared by dissolving Titanium(IV) Butoxide $[Ti(OCH_2CH_2CH_2CH_3)]_4$ in 2-methoxy ethanol (2ME), then stirring at ambient temperature for about 30 minutes with a magnetic stirrer that result a clear sol. This sol has been useed for TiO_2 thin film deposition by a spin coating method.

Similarly, a 100 mM Mn_2O_3 precursor solution has been synthesized by dissolving manganese acetate tetrahydrate [$(CH_3COO)_2Mn$, $4H_2O$] in 2-methoxy ethanol and stirred at room temperature for 10 minutes to obtain a transparent solution which was used to deposit a thin film of Mn_2O_3 by a spin coating method.

2.1.3 Synthesis of SnO_2 precursor solution

In this thesis work, SnO_2 has been used as a channel semiconductor of all TFTs. This SnO_2 has been deposited by a solution-processed technique. For different types of TFT fabrication, SnO_2 precursor solutions of concentration of 100-300 mM have been prepared by dissolving tin chloride [$SnCl_2$] (99.99 percent, Sigma Aldrich) in 2-methoxy ethanol under vigorous stirring for 30 minutes to obtain a clear solution.

2.1.4 Synthesis of ferroelectric $LiNbO_3$ precursor solution

Ferroelectric $LiNbO_3$ dielectric thin film has been fabricated by the solution method and precursor solution of 500 mM has been prepared from Niobium (V) ethoxide (99.95%, purchased from Sigma Aldrich) and Lithium chloride (98%, obtained from Avra).At first, Lithium chloride salts of the required amount have been dissolved in a widely used 2-methoxy ethanol solvent and stirred for about 60 minutes to get a transparent solution. Then in a separate solution, niobium (V) ethoxide has been mixed in 2-methoxy ethanol drop wise and stirred for about 30 minutes. After that, two solutions have been added in a 1:1 ratio and stirred for about 15 minutes to maintain the actual stoichiometry of the final product. The final solution has been stabilized for 30 minutes before use.

2.1.5 Synthesis of a-C precursor solution

An aqueous solution of branched polyethylenimine (b-PEI, MW ~ 25000) (Sigma Aldrich) (Merck Life Science Pvt. LTD) 40 mg/mL has been prepared by mixing b-PEI and distilled

water and ultrasonicated for 3 hours. An aqueous solution of 2 M D-(+) Glucose has been synthesized by mixing water and D-(+) Glucose (Merck Life Science Pvt. LTD) via vortex mixing for 10 minutes. After that, two solutions have been put together via vortex mixing with a volume ratio of 1:1 and kept overnight. The solution has been filtered with a 0.45 μm PVDF filter before spin coating.

2.2 Device fabrication

Mainly two different types of devices have been fabricated for this thesis work. One of them is metal-semiconductor-metal (MIM) and the other one is the bottom gated top contact thin film transistors (TFT). Both of these two classes of devices have been fabricated by solution processed techniques except top electrodes. Semiconductor, dielectric and interface layers have been deposited by spin coating method followed by an annealing process. The flow chart of the whole device fabrication process, including substrate cleaning, is represented in figure 2.1.

2.2.1 Substrate cleaning

For thin-film device fabrication, both highly doped Si wafer and ITO coated glass has been used as substrate as well as the bottom electrode. Before any thin film deposition on the substrates, the surface has been cleaned appropriately. In my thesis work, we have used a popular RCA cleaning process. This process includes several steps clearly shown by the flow chart in figure 2.1 a). Initially, the surfaces have been cleaned with a soap solution and then rinsed with DI water. After that, the substrates have been consequently put in a different medium (like DI water, acetone, and Isopropanol) and ultrasonicated for 20 minutes in each step. Then the substrates have been dried by blowing air and then put in a plasma cleaning chamber for 10 minutes maintaining a plasma generation power of 20W. Plasma cleaning enhances the hydrophilic

nature of the surface and removes residual organic materials that ensure pinhole-free film fabrication.

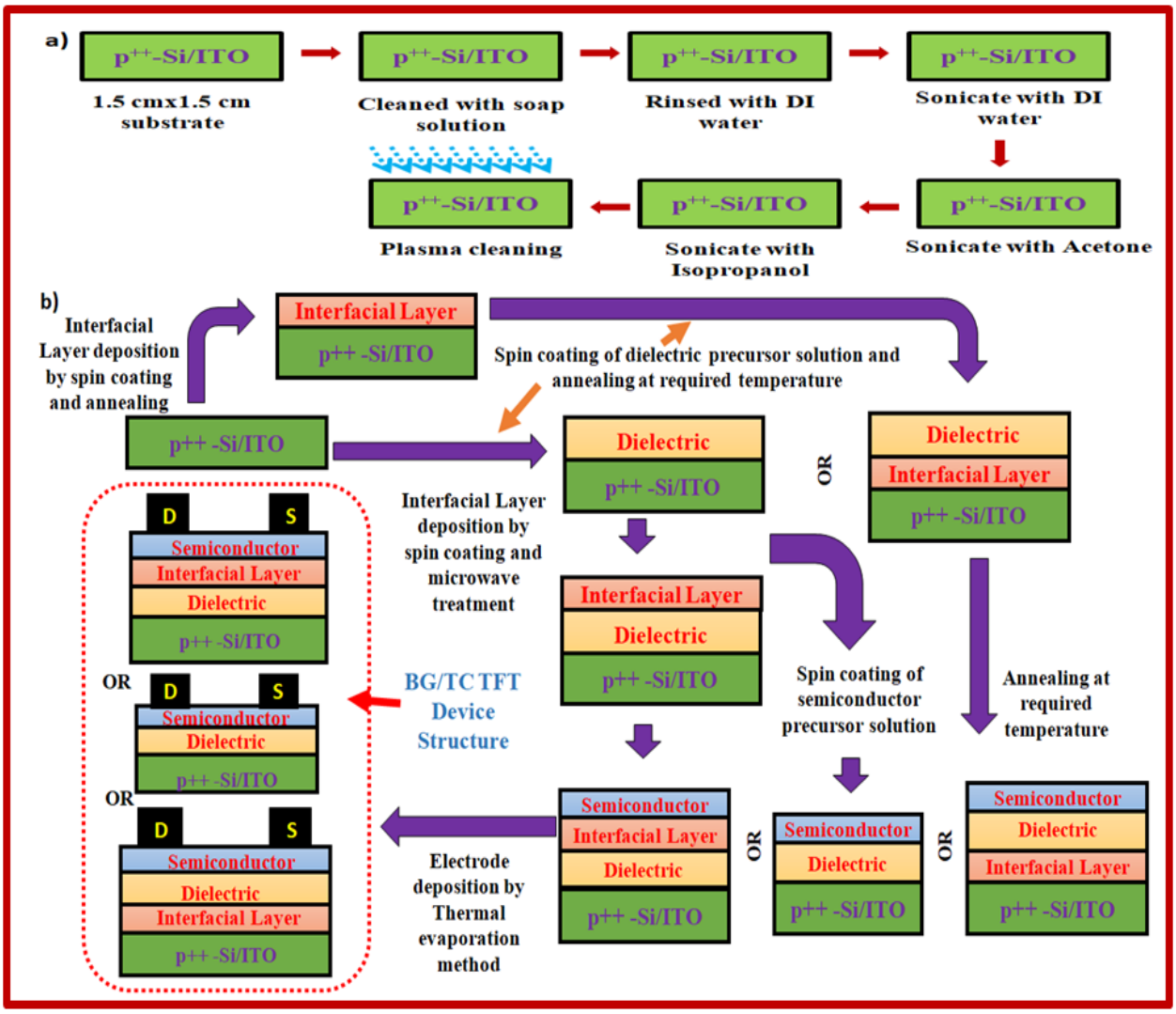

Figure 2.1 *a) Substrate cleaning steps of both types of substrates with standard RCA cleaning method following oxygen plasma treatment, and b) device fabrication steps of a single dielectric layer and the different interfacial layers containing dielectric stack-based thin-film-transistor device.*

2.2.2 Device fabrication with a single dielectric layer

By using an entirely solution-processed approach as described below, we have successfully fabricated SnO_2-based TFTs with two different gate dielectrics with single and bilayer dielectric configurations.

2.2.2.1 SnO_2 TFT with Li-Al_2O_3 gate-dielectric

SnO_2 thin film transistor (TFT) with Li-Al_2O_3 dielectric was fabricated on p^{++}-Si, and ITO coated glass substrate. Before spin coating, a 0.45μm PVDF syringe filter has been used to filter the aged Li-Al_2O_3 dielectric precursor solution. A precursor solution of 500 mM Li-Al_2O_3 has been spin-coated on the cleaned substrates at 5000 rpm for 50 seconds and immediately placed on a hotplate at a temperature of 90°C to dry the samples. These dried samples have been kept in a preheated muffle furnace at 350°C for 30 minutes. This method has been performed three times to get the requisite dielectric layer thickness, finally annealed at 500°C for 1 hour to get the proper insulating phase of Li-Al_2O_3 dielectric. Then, SnO_2 semiconductor precursor solution has been spin-coated on the top layer of the dielectric film with a spinning speed of 4000 rpm for 40 seconds. After drying, these samples have been annealed at 500°C for 30 minutes to get a polycrystalline semiconductor layer. Lastly, 100 nm of aluminum source and drain electrodes have been deposited on the semiconductor layer using the shadow-mask thermal evaporation method, maintaining the W/L ratio of 118 (W= 23.6 mm, L=0.2 mm). Metal-insulator-metal (MIM) device for dielectric properties measurement has been manufactured following the same method of TFT fabrication except for the semiconductor layer.

2.2.2.2 SnO_2 TFT with $LiNbO_3$ gate-dielectric

The SnO_2 FEFET has been prepared in a similar method as mentioned in the earlier section. A heavily Boron doped p-type Si (100) with a dimension of 15×15 mm has been used as substrate

that works as gate electrode as well. The dielectric precursor solution has been spun coat over the cleaned p^{++}-Si substrate at 3500 rpm for 40 seconds and immediately transferred to a hot plate, set at 90°C for five minutes to remove the excess solvent, then heated at 350°C for 10 minutes. This process has been repeated three times to reach the proper dielectric layer thickness. Finally, the samples have been heated at 400°C for 60 minutes to obtain the crystalline $LiNbO_3$ phase. The SnO_2 semiconductor precursor solution of 300 mM has been spun coat on the dielectric film at 3500 rpm for 40 seconds and dried at 120°C on a hot plate for five minutes and then annealed in a preheated furnace at 400°C for 60 minutes. Lastly, an Aluminum source and a drain electrode (100nm) have been deposited by the thermal evaporator by using a shadow mask process, having a channel width and length of 23.6 mm, and 0.2mm, respectively, with a W/L ratio of 118.

2.2.3 Device fabrication with bilayer dielectric stack

2.2.3.1 SnO_2 TFT with bilayer TiO_2/Li-Al_2O_3 dielectric

The TFT with TiO_2 gate interface has been fabricated in a similar way as mention in sec. 2.2.2.1 with an additional TiO_2 thin film before dielectric deposition. The TiO_2 thin film has been deposited on a p^{++}-Si wafer by spinning it at 3500 rpm for 40 seconds, then drying it with a solvent-evaporation technique on a hot plate (set at 90°C). Then this film has been annealed for 30 minutes at 350°C to generate a polycrystalline thin TiO_2 film. On the TiO_2 film, the Li-Al_2O_3 precursor solution has been spin-coated for 50 seconds at 5000 rpm, then annealed at 350°C for 30 minutes. The dielectric film coating has been performed three times to reach the appropriate thickness of the dielectric layer. Finally, a Li-Al_2O_3 thin film has been formed by annealing this film at 500°C for one hour. The precursor SnO_2 solution has been spin-coated (4000 rpm for 40

sec.) and then annealed (500°C for 30 minutes) after dielectric deposition. Finally, aluminum source/drain electrodes with a width-to-length ratio of 118 have been deposited using the thermal evaporation process. In addition to TFT production, a similar approach has been used to produce metal-insulator-metal (MIM) devices for the electrical characterization of single and bilayer dielectric thin films.

2.2.3.2 SnO_2 TFT with bilayer Mn_2O_3/Li-Al_2O_3 dielectric

The SnO_2 TFT with bilayer Mn_2O_3/Li-Al_2O_3 dielectric has been fabricated with a bottom-gate top contact structure. Except for the metallization, all thin films have been prepared by an all-solution processing approach with spin coating in an open atmosphere. Typical ITO-covered glass with a sheet resistance of 70 Ω/□ and roughness of 0.53 nm serves as the substrate (Delta technologies). A 100 mM manganese acetate precursor solution has been spin-coated on a cleaned ITO substrate for 40 seconds at 4000 rpm and then dried on a hot plate at 90°C. Then, the substrates have been annealed for 30 minutes at 350°C in a furnace. The spin coating procedure has been repeated once more, followed by final annealing in a preheated furnace at 550°C for 30 minutes. A 500 mM Li-Al_2O_3 precursor solution has been spun-coat on an ITO/ Mn_2O_3 coated substrate at 5000 rpm for 50 seconds, then annealed at 350°C for 30 minutes. This procedure has been performed thrice to acquire the appropriate thickness. Finally, dielectric coated samples have been annealed for 60 minutes at 500°C in a preheated furnace to fabricate a ~90 nm thick Li-Al_2O_3 layer. A precursor solution of $SnCl_2$ (100 mM) has been spin-coated for 40 seconds at 4000 rpm, then annealed at 500°C for 20 minutes to generate a thin crystalline layer of SnO_2. All of these annealing processes take place in a natural atmosphere. Finally, using the shadow-mask thermal evaporation process, 100 nm aluminum (Al) has been deposited, which serves as the TFT's source (S) and drain (D) electrodes. Metal-insulator-metal (MIM) devices

with Mn_2O_3/Li-Al_2O_3 bilayer have been constructed under identical conditions without the SnO_2 deposition to evaluate the capacitance and leakage current behavior of gate dielectric material.

2.2.3.3 SnO_2 TFT with multilayer Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 dielectric

The SnO_2 FEFET has been fabricated with multilayer Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. Heavily Boron doped p-type Si (100) with dimension 15×15 mm has been used both as substrate and gate electrode. At first, the Li-Al_2O_3 (LA) dielectric solution was spun coat over the cleaned substrate at 5000 rpm for 50 s and dried on a hot plate at 90°C for a few minutes then annealed at 500°C for 30 minutes. The $LiNbO_3$ (LN) gate dielectric solution has been spun coat on the cleaned substrate at 3500 rpm for 40 s and immediately transferred to a hot plate, set at 90°C for five minutes to remove the excess solvent, then annealed at 350°C for 10 minutes. This process has been repeated two times to achieve the required dielectric layer thickness. Finally, the samples have been annealed at 400°C for 1 hour to get the crystalline $LiNbO_3$ phase. Again another Li-Al_2O_3 layer was deposited on top of the $LiNbO_3$ thin film in a similar way as mentioned earlier. Then, SnO_2 precursor of concentration300 mM has been spun coat on the dielectric film at 4000 rpm for the 40 s and dried at 120°C on a hot plate for five minutes, and then annealed in a preheated furnace at 400°C for 1 hour. Lastly, the Aluminum source and drain electrodes (100 nm) have been deposited by the thermal evaporation method using a mask, having a channel width and length of 23.6 mm, and 0.2mm, respectively; W/L ratio of 118. The metal-insulator-metal (MIM) device of LA/LN/LA stack ferroelectric has been fabricated in the same manner, excluding the semiconductor layer. For the MIM device, the above Al electrode has been deposited by the thermal evaporation method having an electrode area of 0.15 cm^2 (0.5 cm×0.3 cm).

2.2.3.4 SnO_2 TFT with bilayer Li-Al_2O_3/a-C dielectric

Devices are fabricated on heavily Boron-doped (p^{++}) Si substrates with a sheet resistance of ~ 50 Ω/□. In the first step, Li-Al_2O_3 dielectric precursor solution (500 mM) has been spin-coated on clean plasma-treated substrates at 5000 rpm for 50 s and subsequently transferred to a hot plate (90°C) for a few minutes for removal of excess solvent. Then they have been processed through an intermediate heat treatment at 350°C for 30 minutes in a preheated furnace. This process has been done three times to reach the desired dielectric thickness, after which the dielectric has been annealed for one hour at 500°C. For the a-C layer deposition, the aqueous solution of branched polyethyleneimine with 2 M D-(+) Glucose has been spin-coated on the plasma-treated (30 W, 1hour) samples with 3000 rpm for the 30s, immediately transferred to the hot plate set at 90°C for about 15 minutes for curing. After that, substrates were exposed to the microwave by using a kitchen microwave oven at power of 240 W for 60 s, subsequently washed with DI water and IPA (Isopropyl alcohol) to remove un-reacted precursors and check a-C layer formation. Then SnO_2 semiconductor film has been deposited and annealed at 500°C for 30 minutes to get a polycrystalline phase. Finally, Al source-drain electrodes of 100 nm have been deposited through a patterned interdigitated mask having a channel width to length ratio of 118 (23.6 mm/0.2 mm) to complete the device fabrication. All the metal-insulator-metal (MIM) devices have been manufactured following the same method of TFT fabrication excluding the semiconductor layer.

2.3 Materials characterization and Electrical characterization

Material Characterization

2.3.1 X-ray diffraction

The structural analysis of powder samples have been carried out using a wide-angle X-ray diffractometer (Rigaku, Mini Flex 600, DTEX–ultra) equipped with a graphite monochromator

with monochromatized Cu K_α radiation (λ=0.15405 nm), the generator had a 45 kV output and a current of 200 mA. Thin films have been characterized by Grazing Incidence XRD (Rigaku, Smart lab). The samples have been placed on the sample holder, and the scans have been carried out at a rate of 3° per minute at a diffraction angle of 20° to 80°.

2.3.2 UV-visible spectroscopy

The JASCO V-650 spectrophotometer has been used to measure the UV-Vis spectroscopic characteristics of the prepared thin films in the wavelength range of 200-900 nm. We employed UV-visible spectroscopy to assess the visibility of a sol-gel coated dielectric thin film that was deposited on a quartz substrate. Also, these data have been used to calculate the optical bandgap of the materials.

2.3.3 Atomic force microscopy

The identification of surface roughness of dielectric thin film is essential because the Thin-film transistor performance is enormously influenced by the dielectric/semiconductor interface. Because the rough interface (dielectric/semiconductor) functions this works as a transport barrier and obstructs the movement of charge carriers in semiconductors that effectively reduces the carrier mobility. Therefore, it is an essential requirement to deposit a thin dielectric layer of excellent quality and low roughness. A powerful nanoscale resolution atomic force microscopy instrument has been used to investigate the surface roughness of the dielectric thin film (AFM). The distance between the cantilever tip and the sample's surface determines which mode an AFM operates. A Solver scanning microscope controller has been utilized to control the NT-MDT multimode AFM (Russia) used to scan the bulk surface morphology of the samples. The root means square roughness of a sol-gel coated dielectric thin film has been calculated using AFM's semi-contact mode. A 100 µm long, single beam cantilever has been used for the semi-contact

mode with a tip mounted with a resonant frequency range between 240 to 255 kHz and a corresponding spring constant of 11.5 Nm^{-1}.

2.3.4 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a quantitative, surface-sensitive spectroscopic technique for determining the substance's elementary composition, analytical formulation, chemical state, and electronic condition. XPS technique has been used to check element composition, chemical state, and electronic state oxide material for my thesis work. For identification of binding energy and chemical oxidation state, X-ray photoemission spectroscopy (XPS) experiments have been performed by using Al-K_α monochromatic X-ray source (1486.6eV) and a high resolution hemispherical electron analyzer (VGScienta-R4000WAL) for detection of excited photoelectrons. The base pressure of the chamber was maintained at 1×10^{-10} mbar during the experiments and resolution of the experimental measurements was ~ 600 meV. C 1s (binding energy = 285.0 eV) is taken as an internal standard for charging effect correction of the spectra. Casa XPS software has been used for analyzing XPS spectrum and the background was subtracted for each peak before fitting.

2.3.5 Scanning electron microscopy

SEM is commonly used to get a magnified image of a surface with the elemental composition and determine topographical sample features with much higher resolving capability. In this thesis work, SEM has been used for the cross-sectional study of multilayer thin films. This cross-sectional study has been carried out by breaking the thin film devices and loading in the SEM sample holder in such a way so that the electron beam of SEM can be exposed to the cross-section of sample. This study has been done by high resolution scanning electron microscopy (NOVA NANOSEM 450, FEITM).

Electrical characterization

2.3.6 Current measurement

The measurement of current density of MIM devices is a critical characterization of the dielectric thin film before TFT fabrication. Ideally, a good dielectric thin film has been sandwiched between two metal electrodes, and shouldn't show any significant current. However, due to a few traces or pinholes in the thin film, a very low-level current travels through it in practice. When the same dielectric thin film has been used in TFT fabrication, we can utilize this measurement to assess the quality of the dielectric thin film and anticipate the order of leakage current. Using an Agilent B1500A semiconductor parameter analyzer, current-voltage density characteristics of MIM devices (p^{++}-Si/dielectric/Al) have been measured in an open atmosphere. Figure 2.2 depicts the device's structural arrangement.

2.3.7 Capacitance vs. frequency measurement

Another essential criterion for determining whether a dielectric thin film may be employed as a gate dielectric in TFTs is its capacitance. For the C-f measurements, a metal plate capacitor MIM device structure has been fabricated. The area of the mask used in the metallization of the top electrode is the effective area of the capacitor. The dielectric constant of the employed dielectric layer in thin-film transistors has been calculated from the capacitance value. This C-f test has been carried out with a p^{++}-Si or ITO/dielectric/Al device using an LCR meter (Keysight LCR meter E4990A) at frequencies ranging from 100 Hz to 10 MHz and a 50 mV AC voltage. Figure 2.2 depicts the device's layout, the same as the capacitance-frequency measurements structure.

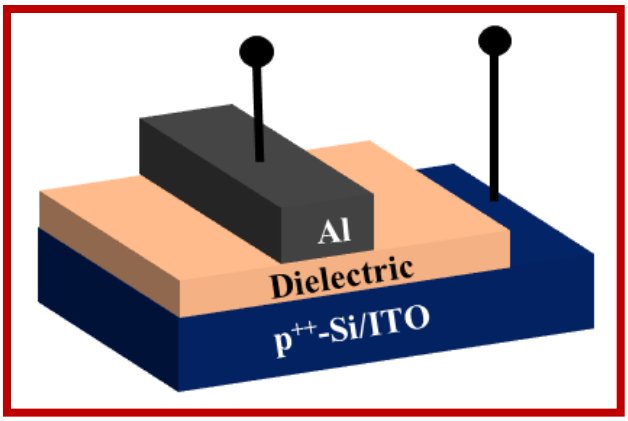

Figure 2.2 *Metal insulator metal device configurations for dielectric characterizations.*

2.3.8 Polarization vs. Electric field measurement

The polarization vs. electric field measurement of the $LiNbO_3$ thin film and Li-Al_2O_3/$LiNbO_3$/ Li-Al_2O_3 dielectric stack has been done in the same MIM devices as the C-f study with a P-E loop tracer. The ferroelectric loop has been traced using Radiant Technologies Precision 4 kV HVI instrument. Here, two-terminal are required one is the bottom p^{++}-Si, and another is the top electrode (mainly Al)

2.3.9 Thin-film transistor characterization

Electrical characterization of the TFT needed two sets of measurements because it is a three-terminal device. Figure 2.3 depicts the TFT device's layout. The characteristics are known as output characteristics when drain current (I_D) is assessed concerning variable drain voltage (V_D) under constant gate voltage (V_G) (V_D vs. I_D). When I_D is evaluated as a function of V_G variation under constant V_D, the features are referred to as transfer characteristics (I_D vs. V_G). The output characteristics are the primary electrical characterization used to ensure the quality of TFT. This characteristic specifies the device's linear and saturation regions. The transfer characteristics, on

the other hand, are more crucial since all the important TFT parameters such as mobility, ON/OFF ratio, V_T, can be extracted from this characteristic. All of these TFT characterizations have been carried out in an open atmosphere. An Agilent B1500A semiconductor parameter analyzer has been used for electrical measurements. Besides, the retention time measurement of the ferroelectric field-effect transistor (FEFET) has been studied by using the same instrument. Here, the sources to drain current of FEFET with two different polarization states of the ferroelectric layer have been collected with time known as retention time measurement. All the double sweep I-V measurements of TFT devices have been carried out by a Precision Source/Measure Unit (KeySIGHT B2912 A). A probe micromanipulator has been used to make electrical contact with the TFT. Electron mobility has been derived from transfer characteristics using the gradual channel approximation.

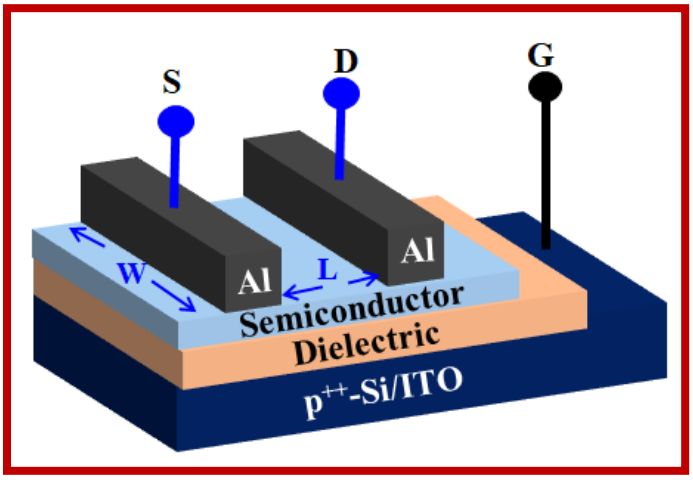

Figure 2.3 *Schematic representation of thin-film-transistor device configuration.*