Chapter 1:

Introduction

Chapter-1

1.1 Background of thin film transistor (TFT) research

Despite enormous efforts in the last several decades to design solution-processed metal-oxide-based electronic devices, their low levels of production and substandard performance have hindered their efficient industrialization so far. While comparing the reliability and electrical operations of Si-based electronic devices to those of solution-processed metal-oxide electronic devices, the latter plays admirably.[1] Nonetheless, regarding the uncomplicated and simple manufacturing, wide-area production, roll-to-roll fabrication, quick deposition, and low price, these devices outperform vacuum-based manufacturing procedures.[2] As a result, numerous research groups are paying attention on the advantages of next-generation processing industry.[3] On the other hand metal oxide-based materials, have a number of advantages, including a) chemical stability in open atmosphere, b) a wide range of electrical characteristics ranging insulating to conducting material, c) ease of connectivity with other systems and devices, and so on.[4] Simultaneously, demand for flat-panel displays (FPDs) with higher resolution, larger screen sizes, and lower power consumption is increasing, pushing existing amorphous silicon thin-film transistor (TFT) technology to its limit.[5, 6] Because of their excellent mobility, transparency, and scalability, TFTs made of metal oxide semiconductors offer massive potential for future display technology.[7, 8] Till now, physical vapor deposition (PVD) procedures are used to make commercial metal-oxide semiconductor-based TFTs,[9] although solution-based alternatives have recently attracted much interest.[2, 10] Not only the metal oxide

semiconductors but also the metal oxide-based gate insulators are playing a crucial role in enhancing TFT properties.[11] In recent years, the fast growth of complementary metal-oxide-semiconductor integrated circuits (CMOS ICs) has revolutionized consumer electronics and the microelectronic sector.[12, 13] Here, SiO_2 has traditionally been considered the more trustworthy dielectric as it produces uniform films with least defects, primarily when used as a native oxide layer to interface with single crystal silicon. In response to the increasing demand for high performance while maintaining acceptable power consumption, the core unit dimension, i.e. thin film field effect transistors (TFFET), has been substantially shrunk down. As Moore's law states that the count of field effect transistors (FETs) in integrated circuits doubles every two to three years, implying that the FET dimension and hence the SiO_2 dielectric thickness are shrinking correspondingly.[14] However, the leakage current density increases when the thickness of SiO_2 layer reaches to the atomic scale, due to direct tunneling, causing significant concerns with standby power usage and system stability.[15] Though the gate leakage problem has been solved since the late 1990s,[16] but the criteria for selecting dielectric candidates were unknown. Around 2001, the technological barrier was solved by substituting HfO_2 for SiO_2, an alternate oxide material with a high dielectric constant (high-κ). The capacitance is defined as follows

$$\mathbf{C = \frac{\epsilon_0 \kappa A}{d}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (\mathbf{1.1})$$

where ϵ_0 is the permittivity in vacuum, κ stands for relative permittivity, A is parallel plate capacitor area, and d is the depth of dielectric layer. As tunneling possibility declines exponentially with tunneling length, using high-permittivity dielectrics allows a thicker layer to offer the same capacitance, maintaining the sufficient oxide thickness (EOT, concerning SiO_2) increases correspondingly, effectively suppressing leakage current. This breakthrough has

sparked high-dielectric research in both academia and industry. A real example of a microprocessor unit (MPU) that benefits from adopting a high-dielectric material is the Intel Core-2 series microprocessor unit (MPU) built on 45 nm node technology. Use of a high-κ Hf-based gate insulator, results in a decrease the power consumption about 30% for Core-2 MPU. Although this, the functioning speed and other performance parameters of the Pentium 4 duo were greatly improved over the previous generation. So, the dielectrics with high-κ value have been widely applied in numerous applications (shown in figure 1.1)) as an insulating layer in thin-film transistors. Instead of the FPD and CMOS technology, these high-κ metal-oxide-based TFTs have been utilized to fabricate low-power consuming light-emitting transistors,[17] photodetectors,[18] memory devices,[19-21] and synaptic devices[22, 23] and so on.

Despite many advantages, it is tough to achieve a significant ON/OFF ratio and higher mobility simultaneously in a TFT with high-κ dielectrics[24] because of their large surface roughness and modest band offset barrier. To overcome these shortcomings, several approaches like high-κ stacked dielectrics[25, 26] and different interface engineering[27, 28] have come to light.

1.2 Brief History and Principles of TFTs

The transistor's history has been established by J. E. Lilienfeld and O. Heil. Their early inventions highlighted the ability of solid-state electronic materials in amplification devices.[29-31] Weimer designed the first thin film transistor in 1962 at RCA Lab utilizing vacuum-based deposition and shadow masking.[32] It was an n-type TFT on glass substrates with a nanocrytalline CdS as the channel layer, SiO_x (x = 1) as gate dielectric, and Au acted as electrodes. After two years, the first transistor with a metal-oxide active layer (SnO_2 channel) was developed using photolithography. In 1996, oxide TFTs were reintroduced as a potential

ferroelectric memory TFT.[33] Oxide TFTs first debuted as a feasible alternative to a-Si in display backplanes in 2003, especially, Zinc oxide (ZnO) based TFTs, could attain electron mobility higher than 1 $cm^2.V^{-1}.s^{-1}$. In the same year a breakthrough took place when Nomura et al. established an single-crystalline Indium Gallium Zinc Oxide (IGZO) semiconducting channel that reveals mobility of 80 $cm^2.V^{-1}.s^{-1}$and an ON/OFF ratio of 10^6.[9] These highly efficient TFTs show potential applications in various fields.

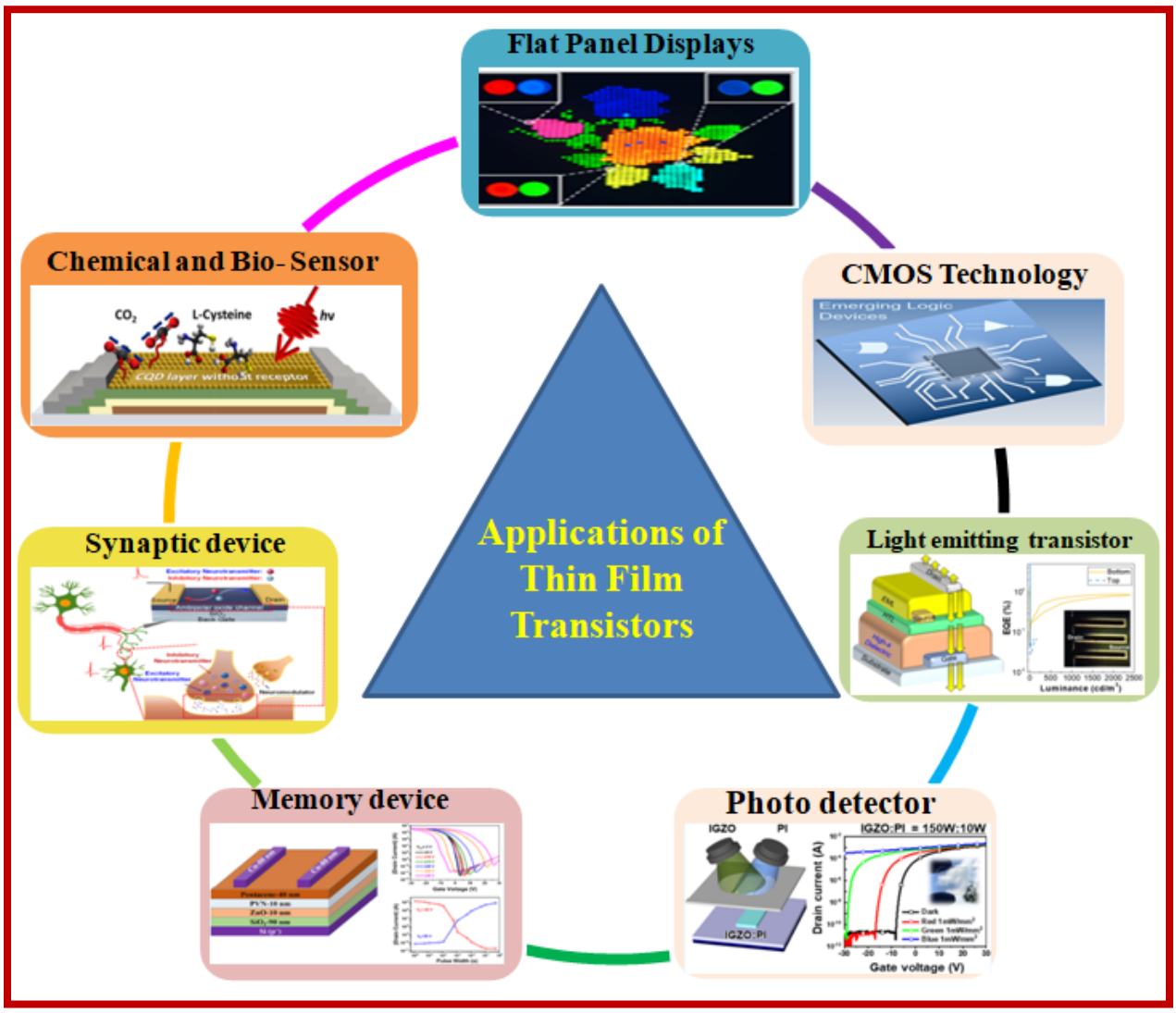

Figure 1.1 *Various applications of metal oxide-based TFTs. Reproduced with permission.[34-40]. Copyright 2019, 2021, 2022 American Chemical Society.*

In TFTs, the field effect is created by regulating the conduction of current between the drain and sources via the gate electrode. Capacitive injection of carriers next to the dielectric/semiconductor interface regulates carrier migration via the gate electrode.

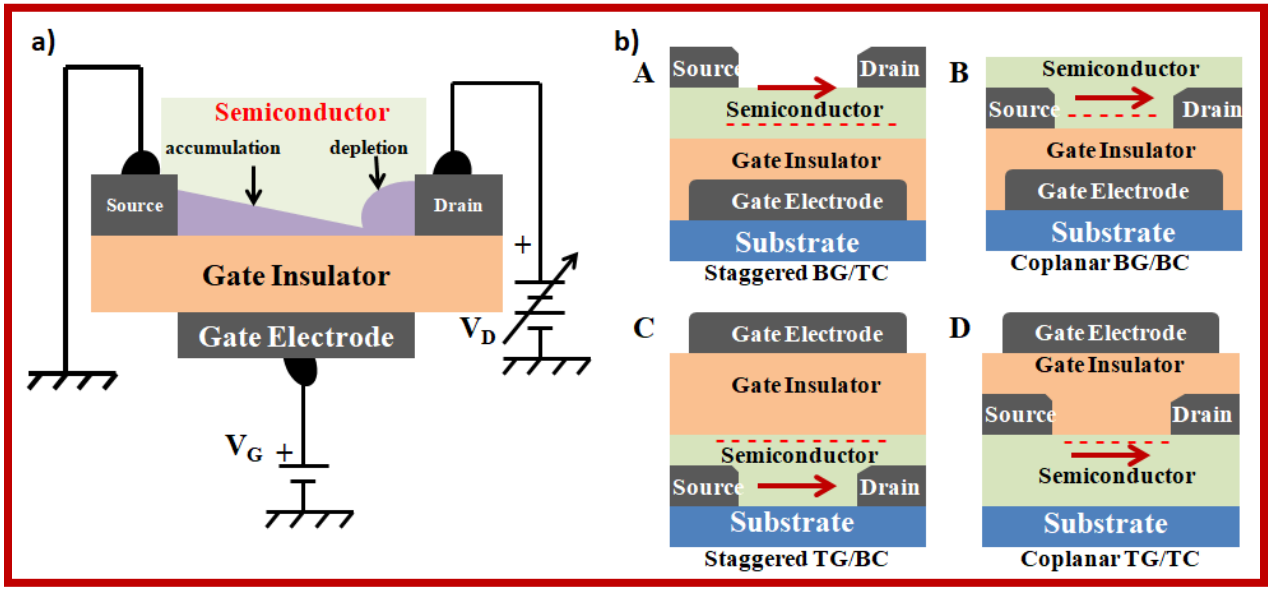

Figure1.2 *Schematics of a) main components of thin film transistor and its working principle, and b) various possible TFT device configurations according to the position of electrodes.*

Figure 1.2 a) shows the TFT device configuration, which contains a semiconducting layer in between the source and drain electrodes and a gate insulator (dielectric) in between the gate electrode and semiconductor. Depending on the device (top gated or bottom gated), the gate insulator layer can be placed on the top or bottom of the semiconductor. Furthermore, based on the position of the source-drain electrodes, the device could be top or bottom contact. The substrate is at the bottom of the device; on which everything is set out. Furthermore, the working principle of TFTs can be explained in figure 1.2 a). When the source electrode is grounded (V_S = 0 V) and a positive gate voltage (V_G > 0 V) is applied on an n-channel enhancement mode TFT,

charge carriers will begin to cumulate at the semiconductor/dielectric interface. The carriers will flow from the source to drain by adding a positive drain voltage (V_D > 0 V). According to Weimer's definition, device layouts are categorized as staggered or coplanar based on whether the source and drain are on opposing sides of the same semiconductor.[6] Schematics of the typical four types of device configuration have been presented in the figure 1.2 b), each with different the benefits and drawbacks.

$$\mathbf{I_D = \frac{1}{2}(\mu C)\left(\frac{W}{L}\right)\left[2(V_G - V_T)V_D - V_D^2\right],} \quad \mathbf{0 \le V_D \le V_G - V_T} \ldots\ldots\ldots\ldots (\mathbf{1.2})$$

$$\mathbf{I_D = \frac{1}{2}(\mu C)\left(\frac{W}{L}\right)(V_G - V_T)^2,} \quad \mathbf{V_D > V_G - V_T} \ldots\ldots\ldots\ldots\ldots\ldots (\mathbf{1.3})$$

With the same manner of conventional MOSFETs, the I-V characteristics of a TFT can be explained by equations 1.2 and 1.3, where μ is the field-effect mobility, and C is the areal capacitance of the gate dielectric layer, V_T is the threshold voltage, V_G and V_D are voltage applied to gate and drain, W and L represent the width and length of the device channel, respectively. With significant applied V_G, the channel becomes active, and the channel current I_D raises with increasing V_D. As V_D rises, the current increases linearly until the channel can no longer sustain further current, as described by equation 1.3. At this point, the channel seems to be saturated, and a saturation zone can be observed in figure 1.2 a) where the current levels off. By increasing V_G, the saturation current can be enhanced, enabling considerable carriers to accumulate near to the semiconductor-insulator interface. Here, the typical I_D vs. V_D plot as illustrated in figure 1.3 a) is called the output characteristics of TFTs. Whereas, the transfer curve, shown in figure 1.3 b), is a plot between I_D vs. V_G. As demonstrated in figure 1.3 b), the channel current tends to very poor until the gate voltage exceeds a certain level, at which point it

rapidly rises and finally levels out. The threshold voltage (V_T) is defined as the critical value of the gate voltage at which drain current starts to increase. Field-effect mobility (μ), ON/OFF ratio, threshold voltage (V_T), and subthreshold swing (SS) are all important electrical characteristics in TFTs. These parameters are influenced by device configuration, fabrication technique, oxide semiconductor, and the contact between semiconducting layer and gate dielectric. The desirable electrical properties of TFTs are such as high mobility and ON/OFF ratio, near-zero threshold voltage, and a minimal subthreshold swing. The following sections describe each of these parameters in more detail.

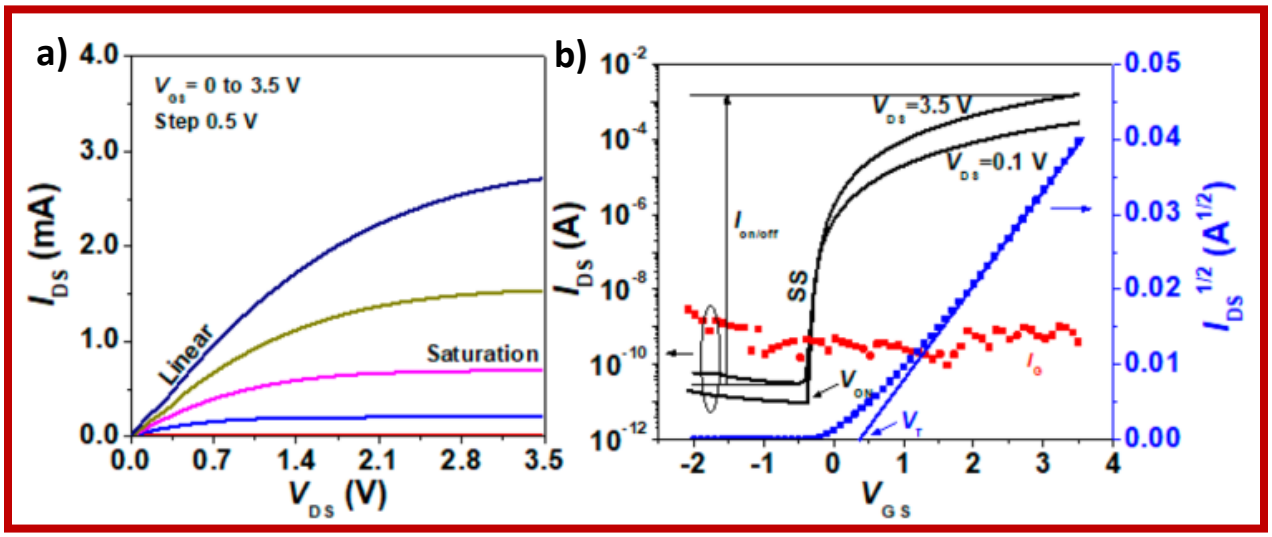

Figure 1.3 *Typical a) I_D vs. V_D and b) I_D vs. V_G characteristics of n-channel transistors.[41]*

1.2.1 Field-Effect Mobility (μ)

The carrier mobility, a characteristic that represents the efficiency of charge carrier passage in a material, has an impact on a device's maximum drain current. Calculating the Hall Effect mobility is a standard method for determining the inherent mobility of bulk materials. TFT mobility differs from the characteristic bulk mobility of its semiconductor because of the narrow

thin-film channel through which charges conduce. Furthermore, saturation mobility is influenced by dielectric charge dispersion, interface trap states, and surface quality.[42] TFTs can be used to extract a variety of mobilities, including effective mobility, field-effect mobility, and saturation mobility. The field-effect mobility is the most broadly adopted mobility, which can be represented as equation 1.4

$$\mu = \frac{\left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2}{\frac{1}{2} C_i \frac{W}{L}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.4)$$

1.2.2 ON/OFF ratio

The ON/OFF ratio is derived the device's highest drain current by its lowest drain current.[43] The noise level of the measurement equipment, channel sheet resistance, and TFT gate leakage current significantly influence the minimum drain current. In contrast, maximum drain current, is governed by the semiconductor and the field-effect transistor's capacitive injection effectiveness.[6] In a good quality TFT, expected ON/OFF ratio should be > 10^5.

1.2.3 Threshold Voltage (V_T)

The threshold voltage (V_T) is the voltage at which a conductive channel forms near the dielectric/semiconductor interface.[43] The frequent way of obtaining the threshold voltage is to extrapolate the linear regime plot of $(I_D)^{1/2}$-V_G. The required value of threshold voltage is close to 0 V to ensure the device works at low voltage. The device is called in an 'enhancement mode' operation when the threshold voltage of an n-type TFT is positive, and it is in depletion mode, when negative. The inverse is true for p-type TFTs. The enhancement mode is advantageous since it does not require any voltage to switch off the transistor, which simplifies circuit design

and reduces resource utilization. The gate voltage required to turn off a transistor is determined by the threshold voltage.[44]

1.2.4 Subthreshold Swing (SS)

The efficiency with which a TFT switches on and off is evaluated by subthreshold swing (SS), directly associated to the dielectric/semiconductor interface quality.[43] It is the inverse of the I_D-V_G plot's highest slope (equation 1.5), and it displays the V_G required to upgrade the drain current by a decade. Low Subthreshold Swing (<100 mV.decade^{-1}) reduces device energy consumption and operating voltage.[45]

$$\mathbf{SS} = \left[\frac{\partial(\log \mathbf{I_D})}{\partial \mathbf{V_G}}\right]^{-1} \ldots\ldots\ldots\ldots\ldots (\mathbf{1.5})$$

1.3 TFT Components: Their Role in TFT Characteristics and Material Selection Procedure for Components

A thin film transistor consists of three main components, namely a gate insulator (dielectric), an active semiconducting layer, and electrodes (gate, source and drains). A detailed discussion of each component has been described in the following section.

1.3.1 Gate Insulator (Dielectric)

An electrical insulator that may be polarized by an electric field is referred as a dielectric. The dielectric polarization generally occurs when a dielectric is subjected to an external electric field, and the electrical carriers move from their prior equilibrium positions. As a result, positive polarities are shifted towards a field direction, while negative polarities are displaced in the opposite direction, resulting in an internal electric field within the dielectric that suppresses the

overall field.[46] As discussed earlier, dielectric film is sandwiched in between the semiconductor layer and gate electrode and acts as a parallel plate capacitor. Also, the dielectric characterizations are done in metal-insulator-metal (MIM) structure as demonstrated in figure 1.4. Figure 1.4 a) shows the MIM device (3D view) without any externally applied bias corresponding random orientation of dipoles in the dielectric layer (figure 1.4 c), cross-section view). On the other hand, when an external bias is applied to it, dipoles are oriented in a particular direction (illustrated in figure 1.4. b) and d)). The key parameter, the electrical charge storage capability of a capacitor at an applied voltage, is the areal capacitance (C), is usually measured in a parallel-plate capacitor design and expressed in equation 1.1. The typical dispersion relation of areal capacitance with frequency for high-κ ($\kappa > 3.9$) and low-κ ($\kappa \leq 3.9$) dielectrics are shown in figure 1.5 a). The areal capacitance of excellent grade high-κ materials normally remains steady at lower frequency regime but drops dramatically at higher frequencies. Some polarization in high-frequency materials cannot follow the alteration in a high-frequency electric field because each polarization operates differently in various frequency ranges. For good grade low-κ materials, the variation in areal capacitance is not taken into account over the entire frequency range because electronic polarisation contributes the most to 'κ'. The electrical characteristics of a gate insulator are another important factor to consider. Ideally, a dielectric should entirely impede the flow of electrical current through it, during application of electric field. However, practically, a certain amount of leakage current (I_{leak}, or leakage current density, J_{leak}), transfers through the dielectric, the quantity of which is normally determined by the electrical field. When a part of an insulating layer becomes conductive, an exponential increase in I_{leak} occurs (figure 1.5 b). The dielectric film is often permanently damaged as a result of the process. The two primary features of gate dielectric are the breakdown voltage (V_b) and

breakdown field (E_b). The dielectric layers should have high V_b and E_b for effective electronic device functioning. Breakdown voltage should be 1.5 times the maximum operational voltage of the device.

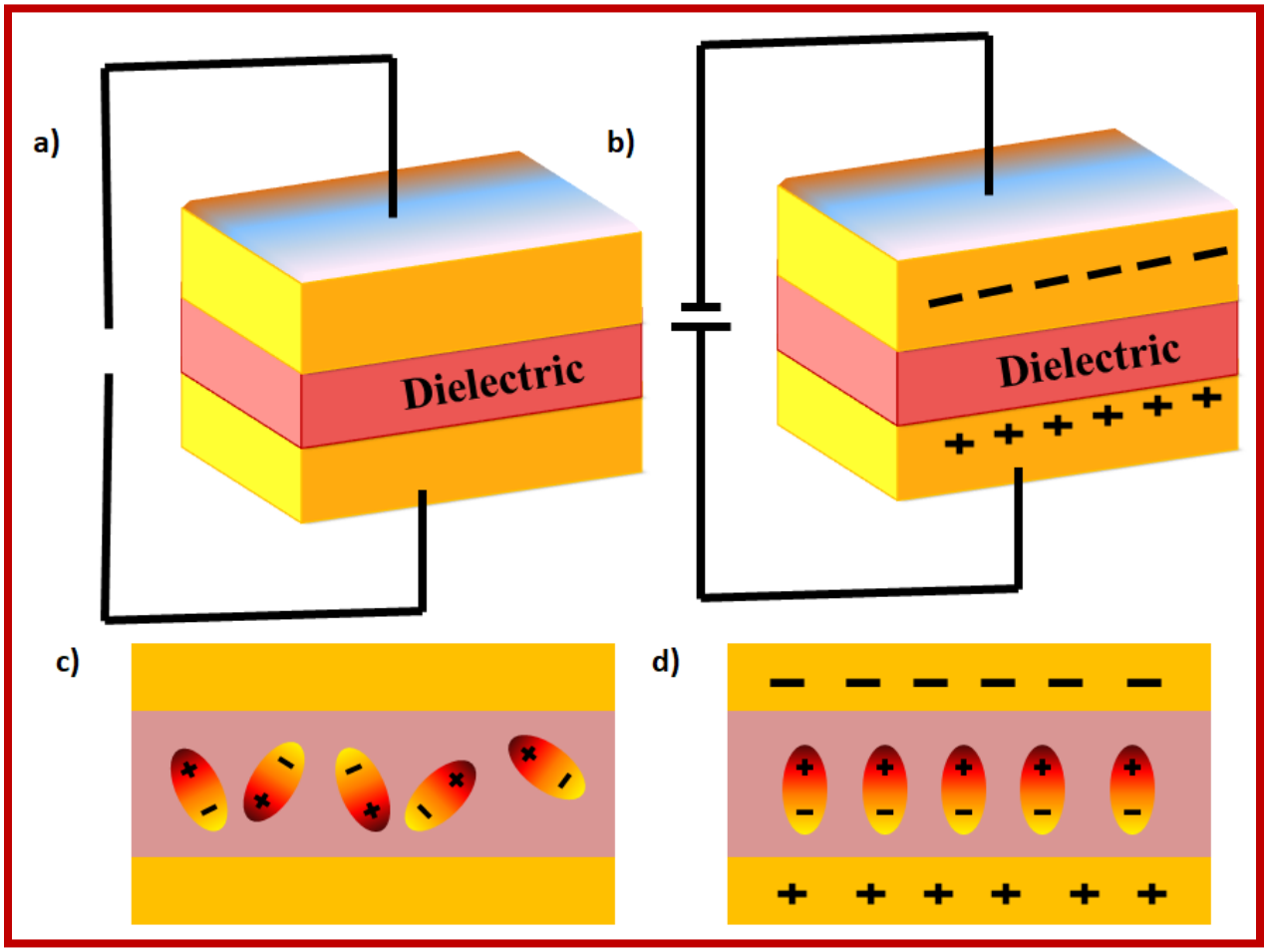

Figure 1.4 *Graphical representation of metal-insulator-insulator (MIM) device a) without, and b) with applied bias. Working of a dielectric inserted parallel plate capacitor c) random orientation of the dipoles in without bias condition, and d) directional orientation in applied bias condition.*

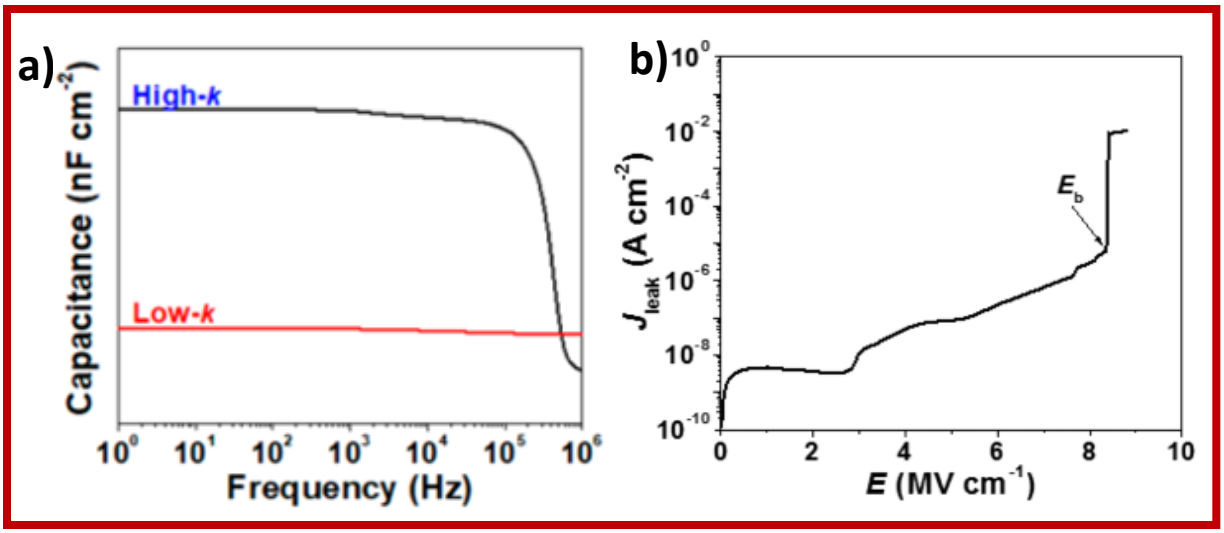

Figure 1.5 *a) Capacitance dispersion relation of typical high and low k dielectric materials, and b) dependence of gate dielectric leakage current with applied field.[41]*

1.3.2 Semiconductor

Because of the high manufacturing cost, semiconductor with high mobility is not the most stringent design criterion, and researchers are looking for some alternative of single-crystal silicon for large-area electronics. Possible alternatives of this large-area electronic applications are polycrystalline or amorphous silicon semiconductors, polycrystalline and amorphous metal oxide semiconductors, and organic semiconductors.[47] Metal oxide (MO) semiconductors, particularly amorphous phase of MO semiconductors, are prospective options as a transparent semiconductor for TFT component, which have achieved excellent development, notably in the display industry.[48] Metal oxide semiconductors have great environmental and thermal budget stability, superior optical transparency, and potential for film fabrication at relatively low temperatures, which makes them ideal for realistic applications. After SnO_2 and ZnO, In_2O_3:Sn (ITO) was known as the earliest transparent conducting oxide (TCO) material roughly sixty years ago, in 1954.[49] Aside from the traditional applications of troublesome silicon, this opens

up new avenues for completely non-hazardous, low-cost, and smooth film production method with good electrical properties. Amorphous oxide semiconductors (AOS) are made up of post-transition metallic ions having electronic configurations of (n-1) $d^{10}ns^0$, where n > 4. Despite their amorphous nature, they exhibit better charge carrier mobility, making them a fascinating subgroup of transparent semiconductors. Because of its unusual band structure, AOS maintains excellent mobility in the amorphous state in comparison to ordinary amorphous silicon and amorphous chalcogenides. In silicon, the valence and conduction bands are formed by highly directed sp^3 hybrid orbitals. The very high charge carrier mobility (>1000 $cm^2.V^{-1}.s^{-1}$) in single crystalline silicon is attributed to the substantial overlap of sp^3 orbitals and extensive conduction band broadening in the periodic single crystal structure. However, in amorphous silicon, a little overlap of the sp^3 orbital inhibits the spreading of the conduction band, limiting mobility to less than 1 $cm^2.V^{-1}.s^{-1}$. The conduction band minima (CBM) may be able to create effective channels for conducting the free electron collected in empty s-states of metal cations in AOS materials. The fact that 's' states have a larger spatial area than inter-cation distances indicates that AOS possesses crystalline-like electron mobility.[9, 50, 51] The spatial overlap of the s state is controlled by the primary quantum number 'n', hence transition metal ions with the electronic structure (n–1) $d^{10}ns^0$, where n > 4, are the best choices for AOS. This condition is also assembled for p-block indium (In) and tin (Sn) with the identical electronic structure of [Kr] $(4d)^{10}(5s)^0$. On the other hand, the more dispersion in valence band minima (VBM) or smaller the hole effective mass, the more holes conduct in metal oxide semiconductors. Cu(I) contained compounds such as copper oxide Cu_2O, delafossites $CuMO_2$ (M = Al, Ga, or In), and oxychalcogenides (LaCuOCh (Ch = S, Se, or Te) [52, 53]are currently receiving a lot of interest. In contrast to conventional n-type metal oxides, these Cu compounds contribute a 3d state near to

VBM, resulting in decreased hole effective mass and improved hole transport capabilities. Another recently discovered and intriguing possibility is stannous oxide (SnO), in which the hybridization of the 5s orbital of Sn with the 2p orbital of O in the valence band results in improved hole mobility.[54] Because of this feature, Cu_2O and SnO have both been successfully used in TFTs and digital circuits.[55, 56]

1.3.3 Electrodes

TFTs are three-terminal devices with gate, drain, and source electrodes. Most studies concentrated on enhancing the quality of the dielectric surface, such as minimizing surface roughness and traps and increasing surface energy to obtain high-performance TFTs. However, the effect of the gate material and its junction with the gate dielectric has a significant impact on TFT performance. The gate electrode surface morphology can greatly affect the surface quality of the overlying gate dielectric in a bottom gate arrangement, and the work function of the gate electrode can effectively influence the threshold voltage by modifying the flatband voltage. More importantly, remote phonon and electrostatic scatterings induced by the bulk dielectric and interface of dielectric/gate electrode might affect the carrier mobility of Si MOSFETs.[57, 58] TFT performance is additionally influenced by the interaction of source-drain (S-D) electrodes in contact with the semiconductor channel interface (materials, contact uniformity, and parasitic resistance). Because characteristics like μ and V_T are dependent on the impedance between channel layer and S-D, the S-D contact materials used in oxide-based TFTs must be carefully chosen.[59] When the S-D contact resistance is larger, a higher applied voltage across the S-D is needed to inject carriers into the channel, causing current congestion and poor current.[60] In oxide-based TFT devices, various metals including Au, Ag, Al, Mo, Ti and transparent IZO, ITO electrodes are employed very frequently. Among them, IZO and ITO electrodes enable for fully

transparent TFT manufacturing, but the high electron affinity of oxide electrodes sometimes creates nonlinear output characteristics in the linear regime, resulting in a potential barrier (Schottky type) between the electrodes and the a-IGZO films.[61]

1.4 Requirement of high-κ dielectric in TFT community: Their advantages and drawbacks

The demand for low-power, very small-scale electronic devices are growing day by day. Because of the gradual increase in gate leakage current, the scaling down of the SiO_2 layer has reached its limit in order to meet Moore's law. Since TFTs are the basic building block of IC-based electronic industries, a proper SiO_2 gate dielectric replacement is crucial for keeping the rest of the gate dielectrics' standards. The ideal choice is to employ high-κ materials (κ value > SiO_2, i.e. 3.9) with larger thickness while keeping an appropriate effective oxide thickness (EOT). In addition to a high-κ value, a gate dielectric for thin film transistors should meet other characteristics such as a wide bandgap, resistance to moisture absorption, a smooth surface morphology with few defects in the surface and bulk, and so on.[41] With κ > 10, high-κ fluorinated polymers like PVDF-TrFE have been employed as dielectric layers. However, because of their intrinsic ferroelectric nature, they have a large hysteresis in their I-V characteristics. As a result, their use has been limited to memory application only.[62, 63] Due to the ionic electric double effect, electrolyte-based dielectrics often display significant areal capacitance (C) on the scale of 10 μF. cm^{-2}, allowing ultralow voltage operation of devices.[64] On the other hand, the ionic liquid is not mechanically strong, and due to poor interfacial adhesion, the dielectric layer can easily delaminate from the substrate during bending in the case of flexible TFTs. Besides, ion gels are also thermally unstable, and unwanted electrochemical

doping from the liquid electrolyte dielectric is a critical issue for its application as a gate dielectric. Mixing P(VDF-TrFE) with ion gel resulted in outstanding thin-film transistor (TFT) performance for a wide range of semiconductors, as reported recently.[65] On the other hand, high-κ metal oxide dielectrics (e.g., TiO_2, HfO_2, ZrO_2, and Al_2O_3) have been extensively explored because of their high C and low J_{leak}. In spite of many advantages, the high-κ dielectric materials are having a number of critical issues that need to be resolved for practical applications. The high-κ dielectric materials with extremely high permittivity (> 40) typically contain large polar groups, resulting in frequency-dependent dielectric constants. Besides, high-κ dielectric may have high dielectric loss that results in high power dissipation of the TFT. In addition, it may create poor bias stress response in TFT operation.[66]

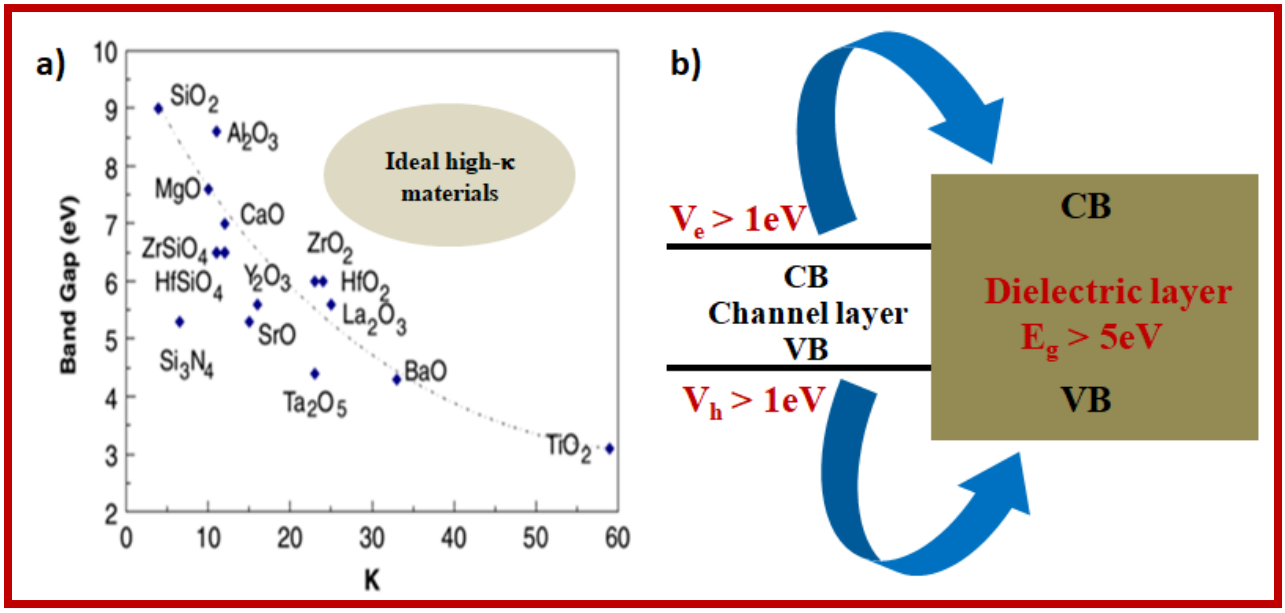

Figure 1.6 *a) The decrease of bandgap values with increasing dielectric constants of well known metal-oxide dielectrics, b) band offset criteria for high-κ dielectrics, where V_e and V_h denote the potential barriers for electron and hole, and CB and VB represent the conduction and valence bands for the semiconducting channel and dielectric films, respectively.[41]*

Besides metal oxides (MOs), metal nitrides (Si_3N_4, AlN) and metal oxide perovskites have also commonly used as inorganic TFT gate dielectrics.[67-69] The correlation between energy band gap (E_g) and dielectric constant (κ) is inversely proportional in common inorganic dielectrics (figure 1.6 a)), hence dielectric films with a lower E_g should be preferred to improve κ value. However, a large E_g is useful for reducing charge creation owing to thermal/photoexcitation processes and suppressing charge transfer from the electrodes.[70, 71] To keep Schottky emission leakage minimal, the band offsets of the dielectric VBM in a p-channel transistor and the CBM in an n-channel transistor should be > 1 eV corresponding to those of the semiconductor (figure 1.6 b)).[72] In 2009, Pal et al. introduced first time a new ion-conducting oxide electrolyte (sodium-β-Alumina (SBA)) thin film via cost-effective solution processed technique and it's successfully utilized as a gate insulator material for the fabrication of low voltage TFT. This 75-nm-thick SBA insulator film exhibited significantly large areal capacitance of 2 $\mu F.cm^{-2}$ because of ionic movement with very low leakage current. The dielectric thin film exhibits a very high-κ value of 170 with a considerably high E_b (> 8 eV). This high value of capacitance was attributed to the significant improvement in polarisation achieved by displacement of an incorporated alkali ion in an applied electric field while maintaining a lower leakage current owing to electron transportation impediment within the dielectric lattice (shown in figure 1.7 a)). Figures 1.7 b) and c) show the output and transfer characteristics. SBA is a promising alternate gate insulator for low operating voltage TFTs with high mobility and a modest ON/OFF ratio[73]. Following this work including SBA other alkali metal (Li, K) doped alumina dielectrics are also synthesized with moderately lower processing temperature (500°C) than initial report (830°C).[74, 75] But the hygroscopic nature of alkali ions affects the device stability in ambient conditions. The conductivity of the alkali ions can be raised by physiosorbed

water in alkali metal incorporated alumina. The interface charge accumulation could become more substantial as alkali ions become more mobile, prompting the field driven current to deteriorate. Also, the probability of interfacial trap state generation increases which increase the threshold voltage, subthreshold swing, diminishing device performances.

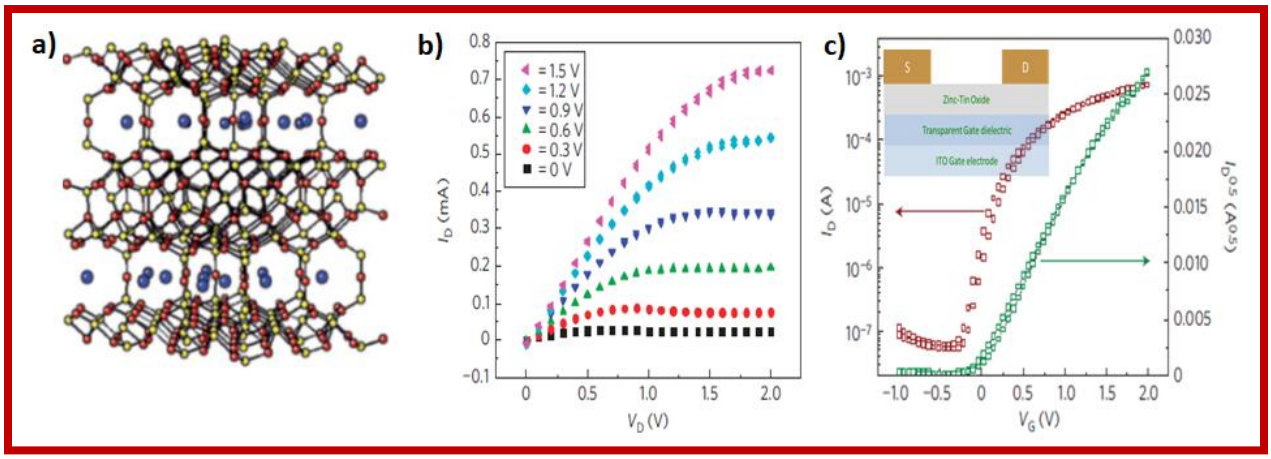

Figure 1.7 *a) Representation of SBA crystal structure, where blue symbolizes the mobile sodium ion and red and yellow represent oxygen and aluminum atoms, respectively. a) Output and b) transfer characteristics of SBA based Zinc Tin Oxide TFT with varying operating voltage (inset of c) shows the schematic diagram of TFT device).[73]*

1.5 Role of Interfacial engineering in the improvement of TFT Device performance

Earlier, several approaches have been taken to reduce interfacial trap states of different inorganic high-κ dielectrics. Among them dielectric/dielectric stack formation[76, 77],self-assembled monolayer (SAM) deposition [78, 79], stacking of semiconductor layer[80] and insertion of electron injecting layer in between gate electrode and insulator[81, 82] are quite popular. Here a few examples of each type of engineering are discussed in detail. Using a gate dielectric stack, Liu et al.[77] reported high-κ HfGdO (HGO) and amorphous IGZO TFTs. Though the HGO

dielectric lowers the operating voltage but due to the high surface roughness and leakage current its practical applications have been hindered. Then a passivation layer of Al_2O_3 was applied with a different combination like Al_2O_3/HGO, HGO/Al_2O_3, and Al_2O_3/HGO/Al_2O_3. The better device performance has been achieved with Al_2O_3/HGO-based dielectric with respect to the other combinations as shown in figure 1.8 a). The Al_2O_3/HGO-based device exhibits higher mobility of 23 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio 1.2×10^7 and low threshold voltage 0.74 V, subthreshold swing 0.09 $V.decade^{-1}$, mainly attributed to Al_2O_3 passivation layer by facilitating a smoother surface and suppressing interface trap state density and interface scattering effect. Figure 1.8 b) shows the comparative device performance of n-type perylene diimide (PDIF-CN_2) TFT with bare and phosphonic acid (PA)-modified Zr-SAND.[83] The devices operate at a low voltage (< 4 V) and the mobility is enhanced with the increasing PA alkyl chain from C_6 to C_{14}, and then reduces slightly for the most extended chain length (C_{18}). Simultaneously, TFT performance is much better on the SAM-modified Zr-SAND surface than on a bare Zr-SAND surface. The PA-SAMs improve ON/OFF ratios by 100, and the threshold voltage switches from negative (-1.2 V) to positive (0.01 V) as the PA-SAM chain length increases. Hysteresis behavior in TFTs characteristics in the high-κ dielectric-based device causes a significant power loss in integrated circuits. Generally, the hysteresis is caused by interfacial trap states present in high-κ dielectric/semiconductor interface. HfO_2 is a well known high-κ dielectric among transition or rare earth metals based oxides with a dielectric constant greater than 20. But the single layer HfO_2 based TFTs reveal a significant amount of hysteresis. Further, combined with a high-band gap Al_2O_3 dielectric, the hysteresis of the IGZO based TFT is totally removed as illustrated in figure 1.8 c). Here mainly, the electron injection nature of ZrO_2 help to compensate for the effect of interfacial trap states; hence the device performance has been improved.[81] Not only has

engineering been done in the dielectric part some examples have been found in the semiconductor part also. As depicted in figure 1.8 d) due to the use of bilayer semiconductor (ZnO: H/ZnO) device performances have been upgraded with a single layer ZnO based TFT.[84] In this case, the ultrathin (~ 3 nm) hydrogenated ZnO layer (ZnO: H) may provide adequate carrier concentration and minimize interface trap density. However, the thick pure-ZnO layer could regulate channel conductivity. So, from the previous discussion, it is clear that interfacial engineering plays a crucial role in TFT device performance improvement. It creates a factual background to carry on my thesis work in this direction.

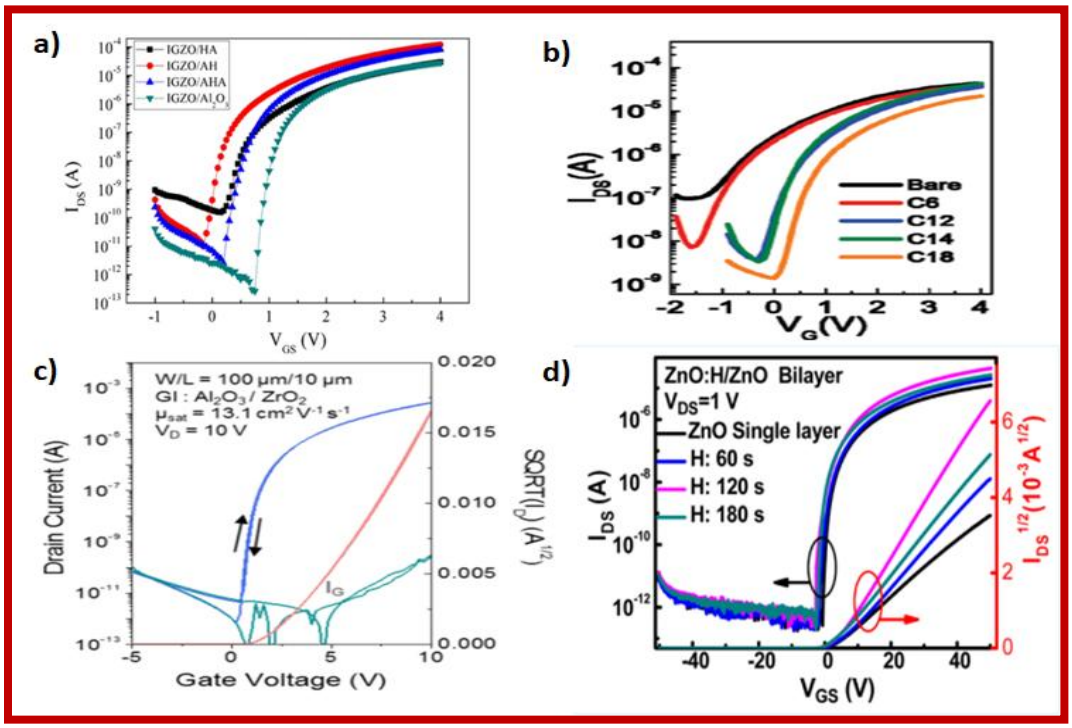

Figure 1.8 *Improvement of device performances using different interfacial engineering. Examples of interfacial engineering using a) dielectric stacks, b) self-assembled monolayer (SAM) passivation layer, c) electron-donating gate dielectric/gate electrode interface, and d) semiconducting bilayer. Reproduced with permission.[77, 81, 83, 84] Copyright 2011,2016,2018,2020 American Chemical Society.*

Based on the earlier progress of interface layer study for higher performance TFT, in this thesis work I have focused on the development of different stacked dielectric thin films to reduce the effect of dielectric/semiconductor interface trap states and DC conduction of solution processed ion-conducting gate-dielectric based metal oxide thin film transistors for upgradation of device performance.

1.6 Ferroelectric Field Effect Transistor (FEFET) with ionic ferroelectric gate dielectric

Ferroelectric Field Effect Transistors (FEFETs) are a special class of transistors where the conventional gate dielectric layer of TFT is replaced by a ferroelectric material. Biasing these FEFETs causes a permanent polarisation in the ferroelectric layer. As a result, even when the biasing is removed, the device retains its polarised state enabling it to perform as non-volatile memory device. A comparative diagram is shown in figure 1.9. Retention time and remnant polarisation are the key figure of merits of a FEFETs. Brief descriptions of these features are given as follows.

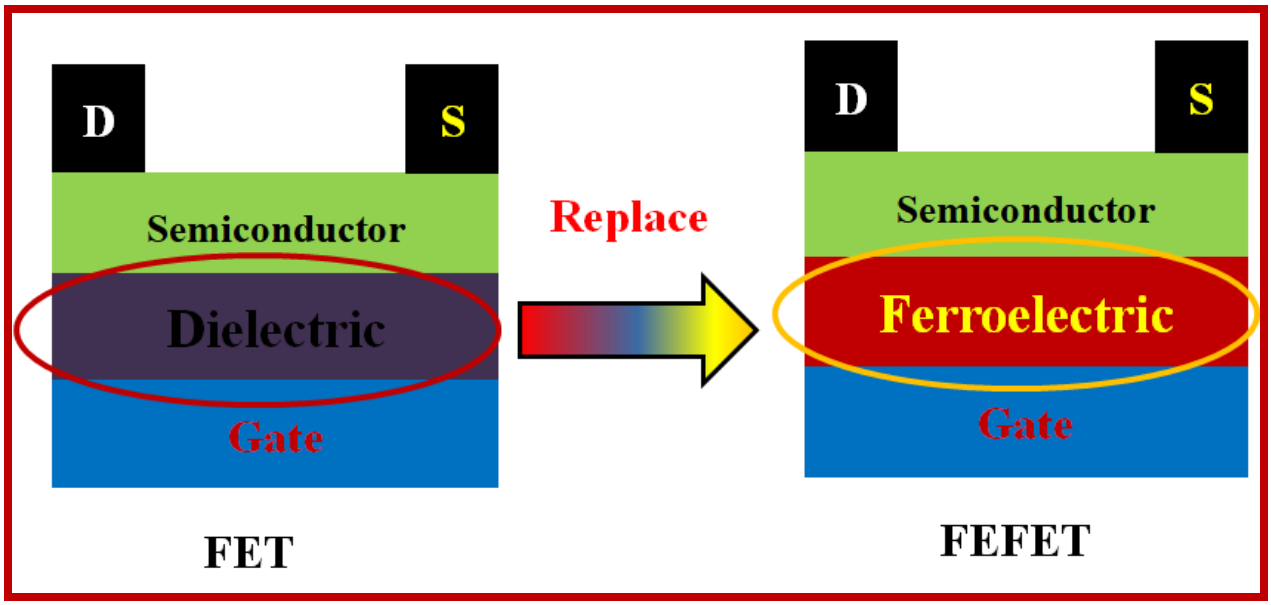

Figure 1.9 *Schematic representations of FET and FEFET.*

1.6.1 Retention Time

It implies for how much time the FEFET can retain its polarised state. Longer retention time is always favourable as it leads to better memory retention ability. Also high memory window leads to device's good read/write ability.

1.6.2 Remnant Polarisation (P_r)

High remnant polarisation is an indication of good ferroelectric material. It defines the amount of polarization that remains in our device after switching off bias.

The longer retention ability and high remnant polarisation of the ferroelectric material allow it to be incorporated into memory devices[85], synaptic devices,[86] high performing logic units, neural networks[87], negative conductance transistors[88] for ultra-low power consuming devices. Additionally, ferroelectric field effect transistor (FEFET) based memory technology is an important alternative to flash and other existing non-volatile memory technologies due to its

small cell size, low power consumption, fast programming/erase speed and nonvolatility. Moreover, nondestructive read operation is the additional superiority of FEFETs over 1-transitor 2-capacitor (1T-2C) based memory technology. However, the reports on retention time in FEFETs are far from the demand of ten-year retention for non-volatile memory devices, which is the main bottleneck of its practical application. The two well studied reasons attributed to the shorter memory retention time are a) presence of depolarization field (E_{depol}) and b) gate leakage current. In case of metal-ferroelectric-metal (MFM) the polarization charge of the ferroelectric layer attracts the opposite charges towards it from the adjacent metal surfaces, resulting in the elimination of E_{depol}. But in the case of FEFET the polarization charges see dissimilar charge densities in the two sides due to the lower carrier concentration of semiconductor layer compared to gate electrode. So, the E_{depol} remains uncompensated. Regarding this challenge, an approach of fully charge compensation of FEFET has been done by introducing a thin film of ion-conducting Li-Al_2O_3 dielectric on both sides of $LiNbO_3$ ferroelectric to improve the device performance of the FEFET. The Li ion movement Li-Al_2O_3 dielectric towards the close proximity of $LiNbO_3$ ferroelectric would effectively help to compensate for depolarization charges.

1.7 Scope and Objective of the Present Work

Metal-oxide TFTs have been widely researched for a range of applications, including active-matrix light-emitting diodes (AMLEDs), light-emitting transistors (LETs), biosensor arrays, photodetectors, memory, synaptic devices, and so on, owing to its excellent charge transport properties. These metal oxide TFTs feature great temperature and chemical stability, as well as outstanding mobility with a high ON/OFF ratio, which are all essential for practical applications. Most of these TFTs require a rather high operating voltage (> 40 V) because to the low dielectric constant (κ) of standard SiO_2 gate dielectric, limiting their applicability to portable equipment.

Furthermore, the high-κ polarisation response of dielectric materials, specifically binary oxide dielectric materials and their thin films has been thoroughly investigated as gate dielectric materials in thin-film transistors with low power consumption. Pal et al. were the first to demonstrate a new technique for developing dielectric materials with excellent 'κ' values by introducing ionic doping into oxide lattices; Sodium-β-Alumina (SBA) is the first ion-conducting metal-oxide (ICMO) dielectric which has been successfully implemented as a gate insulator in low voltage TFTs.[73] In contrast, metal oxide dielectric materials encounter some issues due to their lower bandgap, low band offset with existing metal oxides, a higher number of interfacial trap states owing to high polarity, and hygroscopic nature, which limits their use in reliable and stable device applications. We established some interfacial engineering with the ion-conducting metal oxide dielectric material by a) using metal oxides capable of electron injection, and b) implementing a very smooth amorphous carbon (a-C) layer to improve the device operation. Additionally, ferroelectric field effect transistor (FEFET) based memory has many advantageous features including miniature cell size, less power consumption, fast write/erase speed and nonvolatility, makes it an appealing substitute to other existing non volatile memory devices. Moreover, nondestructive read operation is the additional superiority of FEFETs over 1-transitor 2-capacitor based memory technology. However, the retention time achieved by the FEFETs is not more than few day which is quite far from the demand of ten-year retention period for a non-volatile memory, is the main bottleneck of its practical application. The two well studied reasons attributed to the shorter memory retention time are a) presence of depolarization field and b) gate leakage current. Further, we have done some interfacial engineering with well established $LiNbO_3$ ferroelectric using ICMO to minimize depolarization field and leakage current. So, the main focus of the thesis is to fabricate low operating voltage

ion-conducting dielectric-based TFTs via a cost-effective solution process and device performance improvement in respect of threshold voltage, subthreshold swing and current ON/OFF ratio through some interfacial engineering. Also, to improve FEFETs device performance by reducing depolarization field and leakage current generated through the ferroelectric layer. Overall, the research provides an overview of the use of ion-conducting materials as gate dielectrics and the inserting of different interface layers to construct a bilayer or trilayer dielectric stack for the fabrication of high-performance and low-voltage TFTs. The summary of the next thesis chapters are discussed briefly in the following section

Chapter 2 discusses the preparation of dielectrics, semiconductor, and materials used as an interfacial layer through the low-cost solution process. The thin film of dielectric, semiconductor, and interfacial layers are deposited by spin coating method and used for TFT fabrication. In addition, the methodologies for characterization of materials and devices are thoroughly covered in this chapter.

Chapter 3 describes the development of a high-performance sol-gel derived low operating voltage SnO_2 thin-film transistor with an ion-conducting Li-Al_2O_3 dielectric and a TiO_2 gate interface layer between the gate insulator and gate electrode. A comparison of SnO_2 TFTs with and without a TiO_2 interface layer has been demonstrated. When compared to a device without a TiO_2 interface, the formation of a Schottky junction between p^{++}-Si and n-type TiO_2 aids in the accumulation of extra electrons at the Li-Al_2O_3/SnO_2 interface, which basically refills the interface trap-states and decreases the sub-threshold swing (SS) as well as threshold voltage (V_T) and increases the saturation carrier mobility. As contrasted to a bare Li-Al_2O_3 dielectric, the TiO_2/Li-Al_2O_3 stack dielectric with a high TiO_2 value improves capacitance and lowers leakage current. In a TiO_2/Li-Al_2O_3 stack TFT a higher ON/OFF ratio of 7.2×10^3, effective carrier

mobility (μ) of 16.4 $cm^2.V^{-1}.s^{-1}$, lower SS of 250 $mV.decade^{-1}$, and V_T of 0.73 V has been attained. This research shows a new approach to developing high-yield TFT devices, using an appropriate bilayer gate-dielectric stacks.

Chapter 4 depicts that the Mn_2O_3 gate interface is used to fabricate a high-performance solution-processed sub-volt tin oxide thin film transistor (TFT) onto a sol-gel prepared ion conducting gate dielectric. A comparison of device characterization of two distinct TFTs with and without Mn_2O_3 gate interface reveals that Mn_2O_3 induces excess electrons to the semiconductor/dielectric interface trap states, lowering the device's threshold voltage and subthreshold swing. Furthermore, the depletion layer of the ITO/Mn_2O_3 interface suppresses gate leakage current, which helps to increase the device's ON/OFF ratio. A high capacitance of the dielectric film has been achieved by introducing a high-κ Mn_2O_3 layer between the Li-Al_2O_3 gate dielectric and the gate electrode. This helps in attaining current saturation at lower gate bias. The electron mobility of such a sub-volt TFT with an addition Mn_2O_3 layer in the gate dielectric is 17 $cm^2.V^{-1}.s^{-1}$, the ON/OFF ratio is 3.3×10^4, and the sub-threshold swing is 124 $mV.decade^{-1}$. By identifying suitable material combinations for gate dielectrics, this study proposes a promising alternative approach for the fabrication of high-performance, sub-volt TFTs .

Chapter 5 illustrates that a low-cost solution-processed $LiNbO_3$ based FEFET device fabrication and enhancement of its performances by introducing interfacial Li-Al_2O_3 dielectric material. The improved carrier mobility of 1.9 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio of $1.6\times10^{4,}$ and subthreshold swing (SS) of 167 $mV.decade^{-1}$ are attained with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked ferroelectric layer over only $LiNbO_3$ ferroelectric. The device also has a relatively long retention time. The better performance of this device is explained by using a band model. It is proposed that the intervening of high bandgap Li-Al_2O_3 interfacial layer on both sides of $LiNbO_3$ results in

complete charge compensation as well as prevents charge carrier injection from p^{++}-Si and SnO_2. These phenomena support the better operation of the FEFET device with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. This work demonstrates that the addition of an interfacial Li-Al_2O_3 layer significantly upgrades the electrical properties of the FEFET.

Chapter 6 deals with the comparative studies of two sets of SnO_2 thin film transistors with and without amorphous carbon (a-C) layer using sol-gel-derived Li-Al_2O_3 as a gate dielectric. A remarkable change in the device performance has been realized by inserting a microwave synthesized ultra-smooth a-C layer between gate dielectric and semiconductor as a passivation layer. The coordination bond formation between N and Sn atom helps for better growth of SnO_2 on the top of a-C layer. In addition, the high smoothness of the a-C layer essentially reduces the interface trap state densities by passivation of dangling bonds and defects of high-κ Li-Al_2O_3 dielectric. These phenomena effectively enhance the device performance and stability with a-C layer. Therefore, a better device performance has been achieved in terms of higher saturation mobility of 21.1 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio of $7.0\times10^{4,}$ and lower SS value of 147 $mV.decade^{-1}$ in device-2 with the a-C passivation layer. Also, this device exhibits lower hysteresis and better cyclic stability over device-1 without a-C layer. To the best our knowledge, this research shows the use of simply fabricated ultra smooth a-C layer as an interface modification layer to improve the TFT device performance first time

Finally, chapter 7 is devoted to summarizing the thesis's major findings. Lastly, the future scopes of work relevant to the current thesis have been discussed briefly.