PREFACE

Thin-film transistors (TFT) serve as the foundation of flat-panel display devices. In order to achieve great performance while lowering production costs, researchers looked into a variety of materials in TFTs. Metal-oxides have gained a lot of attention in recent years for thin film transistors due to their broad area manufacturing compatibility, high mobility, and low leakage density properties. At present time, higher resolution, larger screen sizes, and reduced power consumption in FPDs have become increasingly important, which pushes traditional amorphous Si (a-Si) TFT technology to its limits. On the other hand, metal-oxide TFTs have been widely explored for a variety of applications, including phototransistor arrays, gas and pressure sensors, light emitting transistors, photo-detectors, memory, and synaptic devices etc. These metal oxide TFTs possess excellent temperature and chemical robustness, as well as superior mobility and a significant ON/OFF ratio, all of which are crucial for practical applications. However, because of the low dielectric constant (κ) of traditional SiO_2 gate dielectric, most of these TFTs require a fairly high voltage level (<40 V), limiting their utility in portable electronic gadgets (e.g., laptop, tablet, mobile, etc.). Furthermore, the high-κ polarisation response of dielectric materials, specifically binary oxide dielectric materials, has been studied extensively as gate dielectric materials in TFTs with low voltage operation. Although having various superiority, metal oxide dielectric materials encounter some issues due to their lower bandgap, low band offset with existing metal oxides, a higher number of interfacial trap states owing to high polarity, and hygroscopic nature, which limits their use in reliable and stable device applications. In 2009, Pal et al. first time developed a sol-gel derived gate dielectric material (Sodium-β-Alumina, SBA) with higher 'κ' value by introducing ionic doping into oxide lattices, and successfully employed as a gate insulator in low voltage TFTs. The higher 'κ' value in SBA is generated because ionic

polarization that originated due to the Na ion movement in alumina matrix which facilitates operation of TFTs in low voltage regions. This ion-conducting metal oxide (ICMO) class of dielectric material essentially meets the requirement of moderate bandgap in addition to high-κ value. But, further studies on these SBA based TFT reveal that the hygroscopic nature of SBA or other alkali ions incorporated aluminas significantly degrade the device operations. This device property deterioration is attributed to the charge trapping at dielectric/semiconductor interface caused by rapid movement of alkali ions after physisorption of water molecules. So in concern of current challenges faced by high-κ ICMO dielectrics, I established some interfacial engineering with the ion-conducting dielectric material by a) using metal oxides semiconductor (like TiO_2, Mn_2O_3) in between gate electrode and gate dielectric, and b) implementing a very smooth amorphous carbon (a-C) layer in between the gate dielectric and semiconductor layer to enhance the device performance. Furthermore, because of its tiny cell size, low power consumption, rapid write/erase speed, and nonvolatility, ferroelectric field effect transistor (FEFET) based memory storage is a viable alternative to flash and other existing nonvolatile memory technologies. Moreover, nondestructive read operation is the additional superiority of FEFETs over 1-transitor 2-capacitor (1T-2C) based memory technology. However, the reports on FEFET retention period are far from the ten-year retention standard for a non-volatile device, which is the main bottleneck in its widespread implementation. The two well studied reasons attributed to the shorter memory retention time are a) presence of the depolarization field and b) gate leakage current. Further, I have done some interfacial engineering with well established $LiNbO_3$ ferroelectric using ICMO to minimize depolarization field and leakage current. So, the main goal of my thesis work is to fabricate low operating voltage ICMO dielectric-based TFTs via a cost-effective solution process and improvement of the device performances in terms of threshold

voltage, subthreshold swing and current ON/OFF ratio through some interfacial engineering. Also, improvement of $LiNbO_3$ based FEFETs performances using ICMO dielectric as a charge compensating layer. As a whole, the thesis gives an outline of the use of ion-conducting materials as gate dielectrics and the intervening of different interface layers to form a bilayer or trilayer dielectric stack for the fabrication of high-performance and low-voltage TFTs. The thesis is arranged into seven chapters based on the aforementioned discussion:

Chapter 1 consists of a brief introduction of metal oxide thin-film transistors, its components and application along with the scope of my thesis work.

Chapter 2 discusses the material preparation of dielectrics, semiconductor, interfacial layer and thin film deposition through solution processed technique. Specifically in this thesis, the thin film of dielectric, semiconductor, and interfacial layers are deposited by spin coating method and used for TFT fabrication. In addition, the methodologies for characterization of materials and devices are thoroughly covered in this chapter.

The development of a high-performance sol-gel derived low operating voltage SnO_2 thin-film transistor with an ion-conduction Li-Al_2O_3 dielectric and a TiO_2 gate interface layer between the gate insulator and gate electrode is described in chapter 3. A comparative study of a set of SnO_2 TFTs with and without TiO_2 interface layer has been illustrated. The formation of a Schottky junction between p^{++}-Si and n-type TiO_2 aids in the accumulation of extra electrons at the Li-Al_2O_3/SnO_2 interface, which basically fills up the interface trap-states and diminishes the sub-threshold swing (SS) as well as threshold voltage (V_T) and increases the saturation carrier mobility of the device when compared to a device without TiO_2 interface. As contrasted to a bare Li-Al_2O_3 dielectric, the TiO_2/Li-Al_2O_3 stack dielectric with a high TiO_2 value improves

capacitance and lowers leakage current. In a TiO_2/Li-Al_2O_3 stack TFT with an ON/OFF ratio of 7.2×10^3, it attained effective carrier mobility (μ) of 16.4 $cm^2.V^{-1}.s^{-1}$, SS of 250 $mV.decade^{-1}$, and V_T of 0.73 V. This research opens a new approach to developing high-performance TFT devices, using an appropriate bilayer stack of gate-dielectrics.

Chapter 4 depicts that the Mn_2O_3 gate interface can be used in between gate electrode and ionic gate dielectric to fabricate a high-performance solution-processed sub-volt tin oxide thin film transistor (TFT). A comparison of device characterization of two distinct TFTs with and without Mn_2O_3 gate interface reveals that Mn_2O_3 induces excess electrons to the semiconductor/dielectric interface trap states, lowering the device's threshold voltage and subthreshold swing. Furthermore, the depletion layer of the ITO/Mn_2O_3 interface suppresses gate leakage current, which helps to increase the device's ON/OFF ratio. A high capacitance of the dielectric film has been achieved by introducing a high-Mn_2O_3 layer between the Li-Al_2O_3 gate dielectric and the gate electrode. This helps in achieving current saturation at lower gate bias. The electron mobility of such a sub-volt TFT with an additionl Mn_2O_3 layer in the gate dielectric is 17 $cm^2.V^{-1}.s^{-1}$, the ON/OFF ratio is 3.3×10^4, and the sub-threshold swing is 124 $mV.decade^{-1}$. By identifying suitable material combinations for gate dielectrics, this study proposes a promising alternative approach for the development of high-performance, sub-volt TFT fabrication.

Chapter 5 illustrates a low-cost solution-processed $LiNbO_3$ based FEFET device fabrication and enhancement of its performances by introducing interfacial Li-Al_2O_3 dielectric material. The improved carrier mobility of 1.9 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio of 1.6×10^4 and subthreshold swing of 167 $mV.decade^{-1}$ are attained with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked ferroelectric layer over only $LiNbO_3$ ferroelectric. The device also has a relatively long retention time. The improved performance of this device is explained by using a band model. It is proposed that the

intervening of the high bandgap Li-Al_2O_3 interfacial layer on both sides of $LiNbO_3$ results in complete charge compensation that originated due to ferroelectric polarization of $LiNbO_3$ thin film. In addition, this Li-Al_2O_3 interfacial layer prevents charge carrier injection from p^{++}-Si and SnO_2. These phenomena support the better operation of the FEFET device with Li-Al_2O_3/$LiNbO_3$/Li-Al_2O_3 stacked dielectric. This work demonstrates that the addition of an interfacial Li-Al_2O_3 layer significantly upgrades the electrical properties of the FEFET.

Chapter 6 deals with the comparative studies of two sets of SnO_2 thin film transistors with and without amorphous-carbon (a-C) semiconductor/dielectric interface layer using sol-gel-derived Li-Al_2O_3 as a gate dielectric. A remarkable change in the device performance has been realized by inserting a microwave synthesized ultra-smooth a-C layer between gate dielectric and semiconductor as a passivation layer. The coordination bond formation between N and Sn atoms helps for better growth of SnO_2 on the top of a-C layer. In addition, the high smoothness of the a-C layer essentially reduces the interface trap state densities by passivation of dangling bonds and defects of high-κ Li-Al_2O_3 dielectric. These phenomena effectively enhance the device performance and stability with a-C layer. Therefore, a better device performance has been achieved in terms of higher field effect mobility of 21.1 $cm^2.V^{-1}.s^{-1}$, ON/OFF ratio of $7.0\times10^{4,}$ and lower SS value of 147 $mV.decade^{-1}$ in the device with the a-C passivation layer. Also, this device exhibits lower hysteresis and better cyclic stability over the device without a-C layer. To the best of my knowledge, this is a very fast demonstration of the use of a-C layer as a semiconductor/dielectric interface modification layer to improve the metal oxide TFT device performance.

Finally, chapter 7 is devoted to summarizing the thesis's major findings. Lastly, the future scopes of work relevant to the current thesis have been sketched out briefly.

At the end of the thesis, there is a list of periodicals and books that were utilized to bind the thesis together as references.