Chapter 6

Solution processed low operating voltage SnO_2 thin film transistor by using Li_2SnO_3 gate dielectric

6.1 Introduction

Stannic oxide (SnO_2) is a popular n-type oxide semiconductor with high carrier mobility.[118, 208] Besides, in some cases tin oxide shows its p-type or ambipolar semiconducting behavior.[209-211] Particularly thin film transistor with SnO phase shows very good p-channel behavior.[212, 213] However, incorporation of Li-ion can alter its electrical conductivity rapidly.[214] In lower doping levels, it increases its electrical conductivity.[215] However, when the ratio of Li and Sn becomes 2:1, it forms lithium stannate (Li_2SnO_3) compound, which is a good electronics insulator with high ionic conductivity.[216] This Li_2SnO_3 is one of the most popular solid state electrolyte materials due to its higher Li content and Li-ion conductivity with good thermodynamic stability.[217] Because of these reasons, Li_2SnO_3 has been highlighted as one of the most promising Li-ion battery electrode materials.[218] Besides, Li_2SnO_3 can be employed as a nuclear fusion reactor breeding material as well as a microwave dielectric material.[219] Due to the high ionic conductivity and low electronic conductivity of Li_2SnO_3, this material is capable to construct a high capacitive film that can be used as a gate dielectric material of a low voltage thin film transistor (TFT). Besides, low DC conductivity, high breakdown voltage are also important requirements for the use of gate dielectric in TFTs. Until now, a number of inorganic oxide materials including Al_2O_3,[220] ZrO_2,[221, 222] HfOx [223] and polymer materials[224] have been employed to make TFTs with a low operating voltage. Besides, Al_2O_3-based ionic oxide shows great promise for this application.[42, 225-227]Instead of showing very high performance of these dielectrics for TFT fabrication, high processing temperature is one key limitation for using them for flexible substrates.

In this work, we have deposited a thin film of Li_2SnO_3 by sol-gel method, which shows a very high value of areal capacitance with high breakdown voltage and low leakage current. Besides, breakdown voltage of this film is also quite high which can be an appropriate choice as gate insulator of a low voltage TFT. A SnO_2 TFT was fabricated over a heavily doped silicon (p^{++}-Si) substrate by a spin coating method to determine its performance as a gate insulator. From that study, it has been observed that SnO_2 TFT with Li_2SnO_3 gate dielectric shows a good n-channel TFT behavior that operates within 3 V. However, on/off ratio of this device is quite poor. This TFT performance was further improved by an additional TiO_2 thin film. Boosting of device performance by using a multilayer high-k staked dielectric and multicomponent high-k dielectric have been reported earlier.[228, 229] The mechanism of the improvement of this TFT performance due to the additional TiO2 layer has been discussed in detail.

6.2 Thin film device fabrication

All metal oxide TFTs were fabricated with a bottom-gated and top-contact geometry over 15 mm x 15 mm heavily p doped Si (p^{++}–Si) substrate that serve as a gate electrode. Two types of transistors were made-up using Li_2SnO_3 and Li_2SnO_3/TiO_2 dielectrics called Device 1 and Device 2 **(figure-6.1)** respectively. At the beginning, substrates were washed in a soap solution, DI water, acetone and isopropanol in successive steps as mentioned in our previous work [42, 117, 153, 154, 230]. Thereafter to eliminate the leftover hydrocarbons from the substrate's surface and to make them compatible for solution deposition, all those wet cleaned substrates were then dry cleaned with oxygen plasma for 10 minutes. The filtered precursor solution of Li_2SnO_3 has been spin coated over a clean p^{++}-Si substrate with a spinning speed of 4000 rpm for 1 minute followed by a drying process at 90ºC hotplate to remove the

solvent. After that, those samples were annealed at 350ºC for 30 minutes in a high temperature furnace. To reach the desired thickness of gate dielectric, this process was continued for 2 more times. In the final step of dielectric deposition, samples were annealed at 500ºC to get a polycrystalline film of Li_2SnO_3. For TiO_2/Li_2SnO_3 bi-layer dielectric, TiO_2 thin film was deposited before Li_2SnO_3 deposition. For that deposition, a precursor solution of TiO_2 (titanium butoxide, 300 mM) has been spin casted in a similar way and was kept at 500ºC for 30 minutes to get polycrystalline thin film of TiO_2. Thereafter, the Li_2SnO_3 dielectric was coated over the TiO_2 film under the same condition. Then, these bi-layer (TiO_2/Li_2SnO_3) dielectric thin films were left inside a high temperature furnace for 30 minutes at 500ºC to obtain a compact bilayer polycrystalline thin film. To deposit SnO_2 film, a filtered precursor solution of $SnCl_2$ (300mM) has been spin casted (4000 rpm/30 seconds) over the dielectric thin film (Li_2SnO_3 or TiO_2/Li_2SnO_3) and subsequent drying processed on 90˚C hotplate. Then these samples were transferred to a 500ºC furnace for the final annealing process that was capable of obtaining the polycrystalline phase of SnO_2 thin film. Finally, thermally evaporated aluminum source-drain electrodes (100 nm) have been deposited through a shadow-mask method, resulting in the TFTs device with a 'width to channel length' ratio of 118 (W/L = 23.6/0.2 mm). Two thin film devices with a 'metal insulator metal (MIM)' device structure were synthesized under the similar ways which were followed for TFT fabrication to evaluate the capacitance and insulating behaviour of Li_2SnO_3 material. This Metal-Insulator-Metal (MIM) device for single and bi-layer dielectric thin films are p^{++}-Si/ Li_2SnO_3/Al and p^{++}-Si/ TiO_2/Li_2SnO_3/Al respectively that are shown in **figure 6.1c)** and **d)** respectively. Similar devices except the top Al electrode were fabricated for X-ray diffraction and AFM studies.

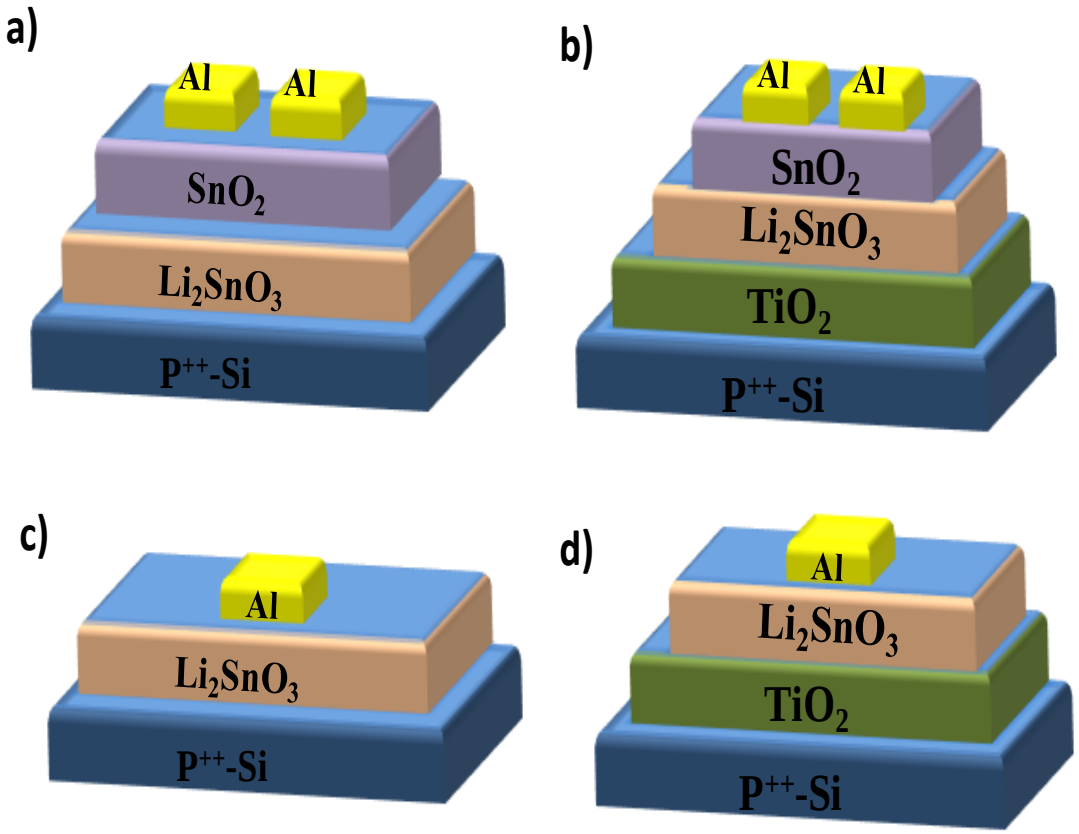

Figure 6.1: Device architectures of a) device-1 (without TiO_2 gate interface), and b) device-2 (with TiO_2 gate interface), c) MIM structure of device-1, d) MIM structure of device-2.

6.3 Result and discussion

6.3.1 Thermal analysis

To measure the crystallization temperature of Li_2SnO_3 dielectric, Thermogravimetric Analysis (TGA) and differential thermal analysis (DTA) were studied simultaneously. These investigations were performed with a powder precursor sample at a heating rate of 20ºC/minute under N2 atmosphere. **Figure 6.2** shows the l behavior of the sample under the thermal conditions. This data shows the 20% weight loss of the

sample within140ºC, which is attributed to the moisture evaporation and physically adsorbed water. A corresponding exothermic peak at 140ºC is present in the DTA curve. Around 6% weight loss has been detected in the temperature range of 300ºC to 400ºC which is associated with the decomposition of hydroxyl groups of the sample. In the temperature range of 400ºC-600ºC, no substantial weight loss was recorded. An exothermic peak was seen about 600ºC, which is connected with the crystallization of Li_2SnO_3 powder. Based on this DTA/TGA data, 500ºC annealing temperature was assigned to get the crystallized phase of Li_2SnO_3 dielectric film.

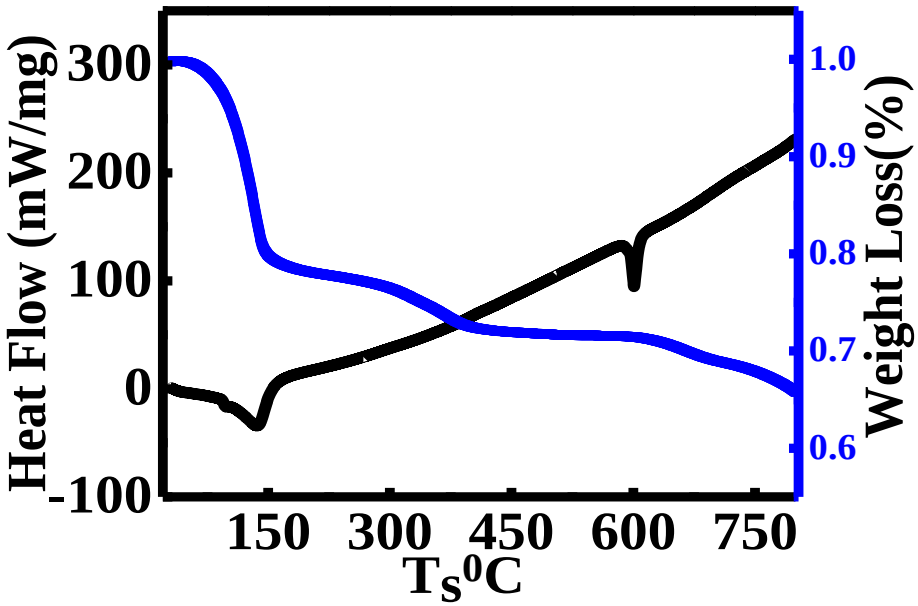

Figure 6.2: TGA and DTA graph of Li_2SnO_3 powder

6.3.2 Structural analysis

Grazing incidence X-ray diffraction (GIXRD) measurements were performed to determine the crystalline phase of metal-oxide thin films. **Figure 6.3a)** shows the GIXRD data of TiO_2 thin films, indicating its good crystalline phase with intense reflection from (101), (200), (211). The GIXRD data of SnO_2 shows the reflection form (110), (101), (111) and (211) reflections **(figure 6.3b),** which implies its crystalline

phase. The GIXRD data of Li_2SnO_3 **(figure 6.3c)** confirm the diffraction peaks at 26.6, 33.7 and 48.5 correspond to the reflection planes of (022), (023) and (043) respectively. The TiO_2/Li_2SnO_3 bi-layer stacked dielectric shows the same set of data as single layer Li2SnO3 thin film **(figure 6.3d).**

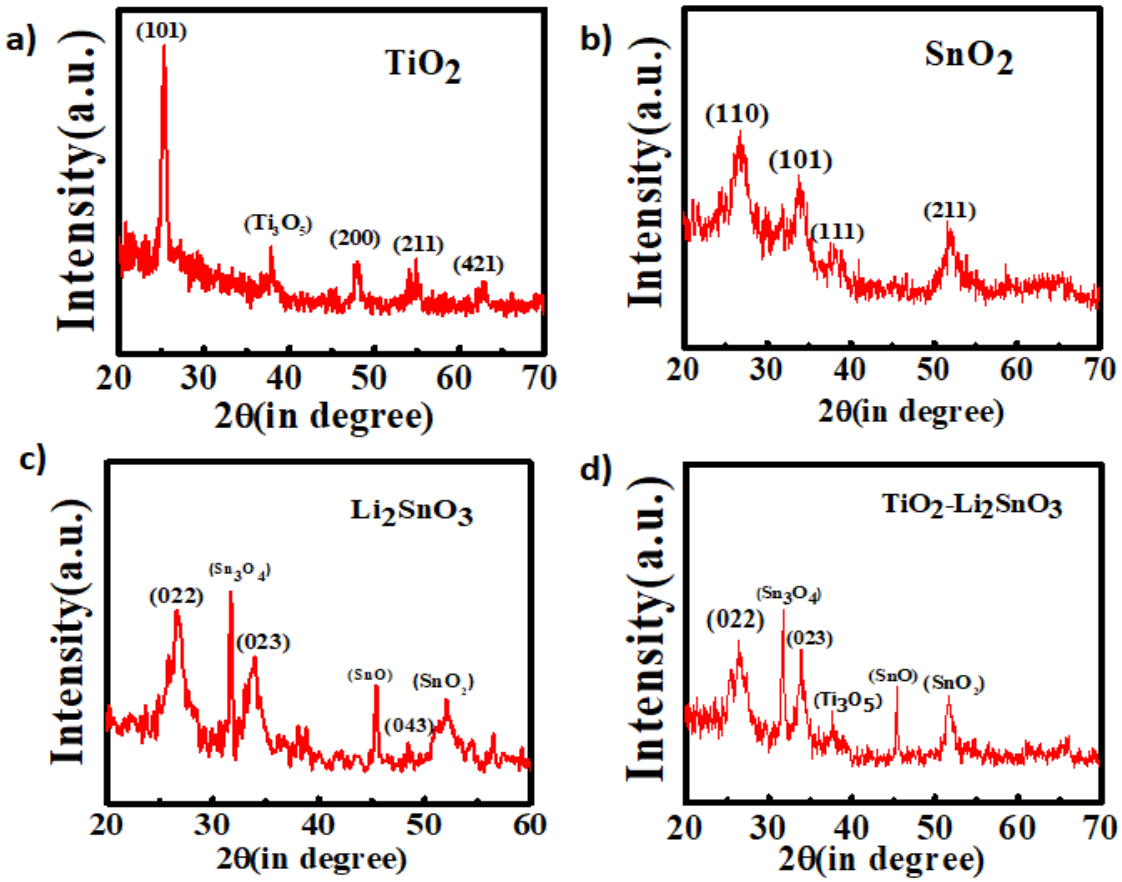

Figure 6.3: a) GIXRD pattern of TiO_2 thin film b) GIXRD pattern of SnO_2 thin film c) GIXRD pattern of Li_2SnO_3 thin-film d) GIXRD pattern of TiO_2/Li_2SnO_3 thin film.

6.3.3 Optical properties of dielectric thin films

To realize the optical characteristics of dielectric thin films, UV-VIS absorption and transmission studies were performed. Thin-film of single and bilayer dielectrics was coated through a spin casting method on quartz substrate under the same conditions as followed for TFT fabrication. **figure 6.4** shows the transmittance data of samples and it is clear that the thin film of dielectric Li_2SnO_3 is 93% optically transparent and bilayer TiO_2/ Li_2SnO_3 is around 76% in the UV-Vis range (300-800 nm). High transmittance of Li_2SnO_3 film originates from the smooth and uniform nature of the film which causes

very low scattering. Because of the additional TiO_2 layer, TiO_2/Li_2SnO_3 stacked film increases surface roughness that adds surface scattering from grains resulting in reduced transparency of the bi-layered TiO_2/Li_2SnO_3 sample.

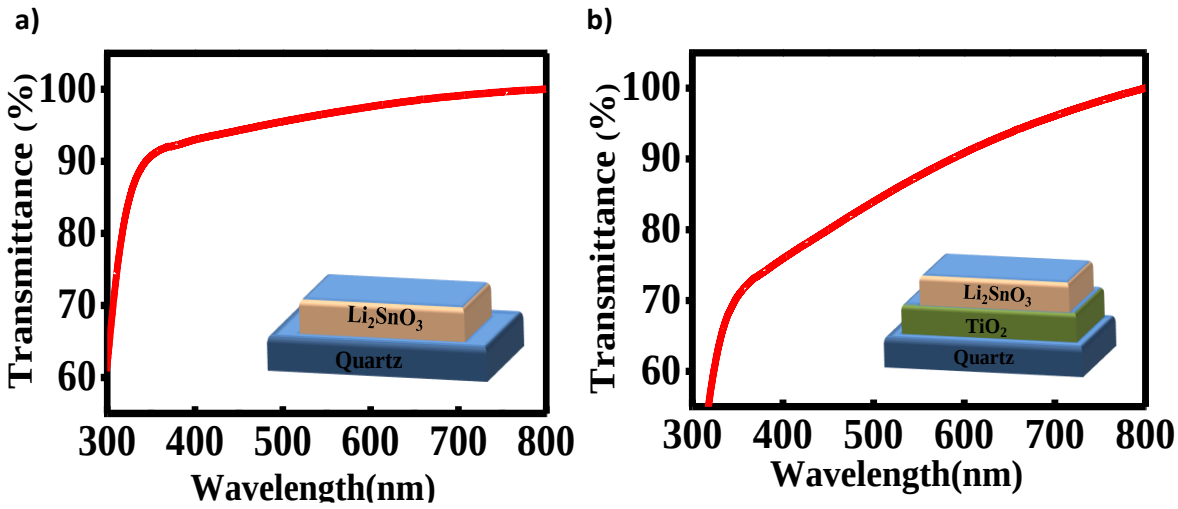

Figure 6.4: Optical transmittance plot of a) Li_2SnO_3 Dielectric film b) TiO_2/Li_2SnO_3 bi-layered dielectric film

6.3.4 Dielectric and Electrical Characterizations

Devices with MIM device structure were made with the dielectric film sandwiched between p^+-Si and Al electrodes to observe the insulating nature and areal capacitance of dielectric thin films. The current density vs. voltage data for both single-layer Li_2SnO_3 and bi-layer TiO_2/Li_2SnO_3 are shown in **figure 6.5 a**. Single-layer Li_2SnO_3 and bilayer TiO_2/Li_2SnO_3 show the current density of 3.8×10^{-5} A/cm^2 and 5×10^{-4} A/cm^2 respectively at 5 volts. These data distinctly depict that the current density of both single and bilayer dielectrics is quite low, indicating a good insulating nature of dielectric thin films which is suitable for the fabrication of thin-film transistors. It is known that nonuniformity and pinholes in dielectric thin films are the most probable

reasons for the high leakage current. From this leakage current data, we can speculate that the deposited dielectric thin films are uniform and have the least pinholes. Because of the lattice mismatching of two different grain geometries at interfaces, the current density of single layer Li_2SnO_3 is much greater than that of bilayer TiO_2/Li_2SnO_3[231] [154]. Table-1 summarizes the current density and areal capacitance of these films.

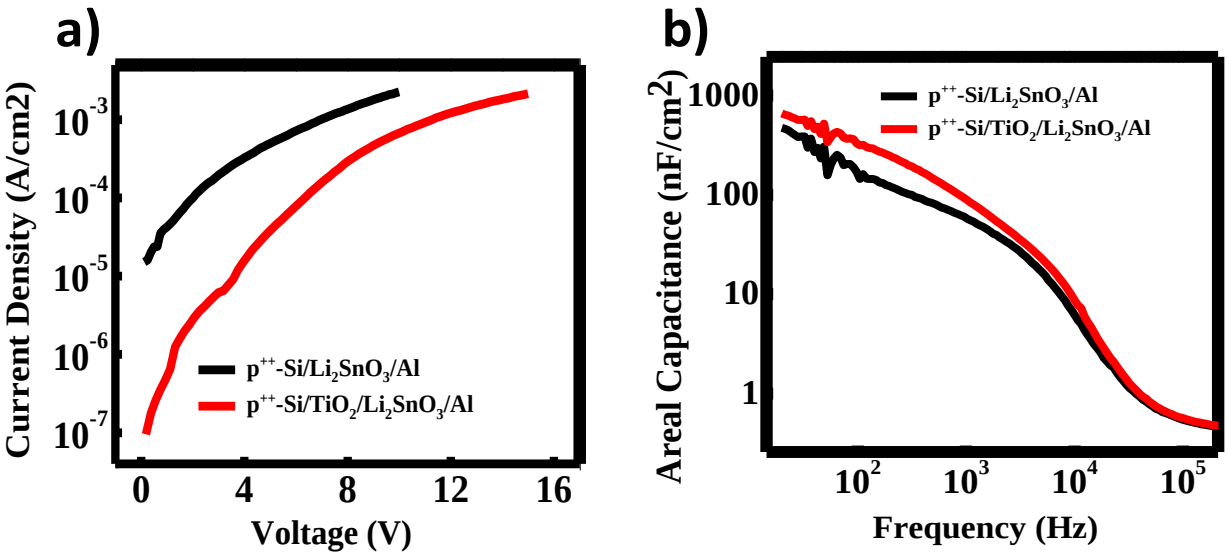

Figure 6.5: a) Current density versus applied voltage and b) areal capacitance versus frequency data of Li_2SnO_3 and TiO_2/Li_2SnO_3 with MIM structure.

To examine the variation in capacitance of dielectric thin films of single layer Li_2SnO_3 and bilayer TiO_2/Li_2SnO_3 in different frequencies, we performed frequency-dependent capacitance (C-*f*) measurement of the same MIM device, as shown in **figure 6.5 b**. From his study, it has been observed that the variation of both dielectrics up to 10^5 Hz is quite small which is suitable for the high-frequency application of TFTs. However, above 10^5 Hz, areal capacitance decreases rapidly with frequency because of the relaxation time of Li^+. The capacitance value of single layer Li_2SnO_3 and bilayer TiO_2/Li_2SnO_3 at a lower frequency (50Hz) is around 305 nF cm^{-2} and 518 nF cm^{-2} respectively, which are significantly higher than the previously reported solution processed high k dielectrics.[154] In the case of bilayer TiO_2/Li_2SnO_3 architecture, the device act as a combination of parallel plate capacitors connected in series. As a result, the effective capacitance can be calculated in the following way:

$$\frac{1}{C_{effective}} = \frac{1}{C_{TiO_2}} + \frac{1}{C_{\mathrm{Li2SnO3}}}$$

Since the dielectric constant of TiO_2 is very high (>80), therefore the areal capacitance per unit area of bilayer TiO_2/Li_2SnO_3 thin film becomes higher than the single-layer Li_2SnO_3 dielectric thin film.

Table 6.1 Current densities, areal capacitance per unit area of dielectric films

Dielectric	**Areal capacitance C (nF/cm^2)(at 50 Hz)**	**Leakage current density at 5 V bias (A/cm^2)**
Li_2SnO_3	305	5×10^{-4}
TiO_2/Li_2SnO_3	518	3.8×10^{-5}

6.4 Thin Film Device characterization

As mentioned earlier, two different metal oxide TFTs were fabricated by using single-layer Li_2SnO_3 and bi-layer TiO_2/Li_2SnO_3 thin films which are called device-1 and device-2 respectively. The W/L ratio of both devices is 118. Transfer and output characteristics of these TFTs were measured under air ambient conditions by using a semiconductor parameter analyzer that is shown in **figure 6.6**. Output characterization of both devices shows that drain current (I_D) saturation can be achieved clearly within 2V of drain voltage, while the gate voltage varies from-0.5 V to 2V (**figure-6.6 a** and **b**). This characterization indicated its capability to drive the device within 2.0 V external bias. The gate bias of both devices varied from -1V to 3V under 3 V drain bias to examine the transfer characteristics, as illustrated in **Figures 6.6 c** and **d**. This data indicates that the threshold voltage of Device 1 and Device 2 is 0.65 V and 0.2 V, whereas the on/off ratio is 14 and 50 respectively. Besides, hysteresis behavior of output and transfer characteristics were studied for both devices instead of having mobile Li^+ ions in the dielectric thin film, it has been found that there is practically no

hysteresis in the characteristics, implying the fasted switching of mobility ion concerning the polarization change of the external gate bias. It is made feasible by Li^+'s small size, which allows it to move quickly across the crystal channel. In addition, a considerable improvement has been observed in the transistor characteristics when the TiO_2 interface is introduced. The following equations are used to determine the effective carrier mobility (ECM), subthreshold swing (SS), and dielectric/semiconductor interface trap state of these TFTs, respectively. (23)

$$SS = \left[\frac{d(log\ I_D)}{d\ V_G}\right]^{-1} \ldots\ldots\ldots\ldots\ldots \quad (1)$$

$$I_D = \mu C \frac{W}{2L}(V_G - V_T)^2 \ldots\ldots\ldots\ldots \quad (2)$$

$$N_{SS}^{Max} = \left[\frac{SS \times log\ e}{\frac{kT}{q}} - 1\right]\frac{C}{q} \quad \ldots\ldots\ldots \quad (3)$$

Saturation drain current, capacitance per unit area, gate voltage, and threshold voltage are represented by I_D, C, V_G, and V_T, respectively. The effective carrier mobility of TFT has been calculated from transfer characteristics (**figure 6.6 c)** and **d**)) by using equation (2). The electron mobility Device-2 (TFT with TiO_2/Li_2SnO_3 stacked dielectric) obtained from **figure 6.6 d)** is 3.47 $cm^2V^{-1}s^{-1}$ which is significantly higher than Device-1 (TFT with Li_2SnO_3 dielectric) TFT (3.04 $cm^2V^{-1}s^{-1}$). Interface states are an important parameter to define the dielectric/semiconductor interface and quality of surface states. The interface-states-densities (N_{ss}^{max}) have been calculated using equation (3). **Table 6.2** summarizes the device characteristics of both TFTs.

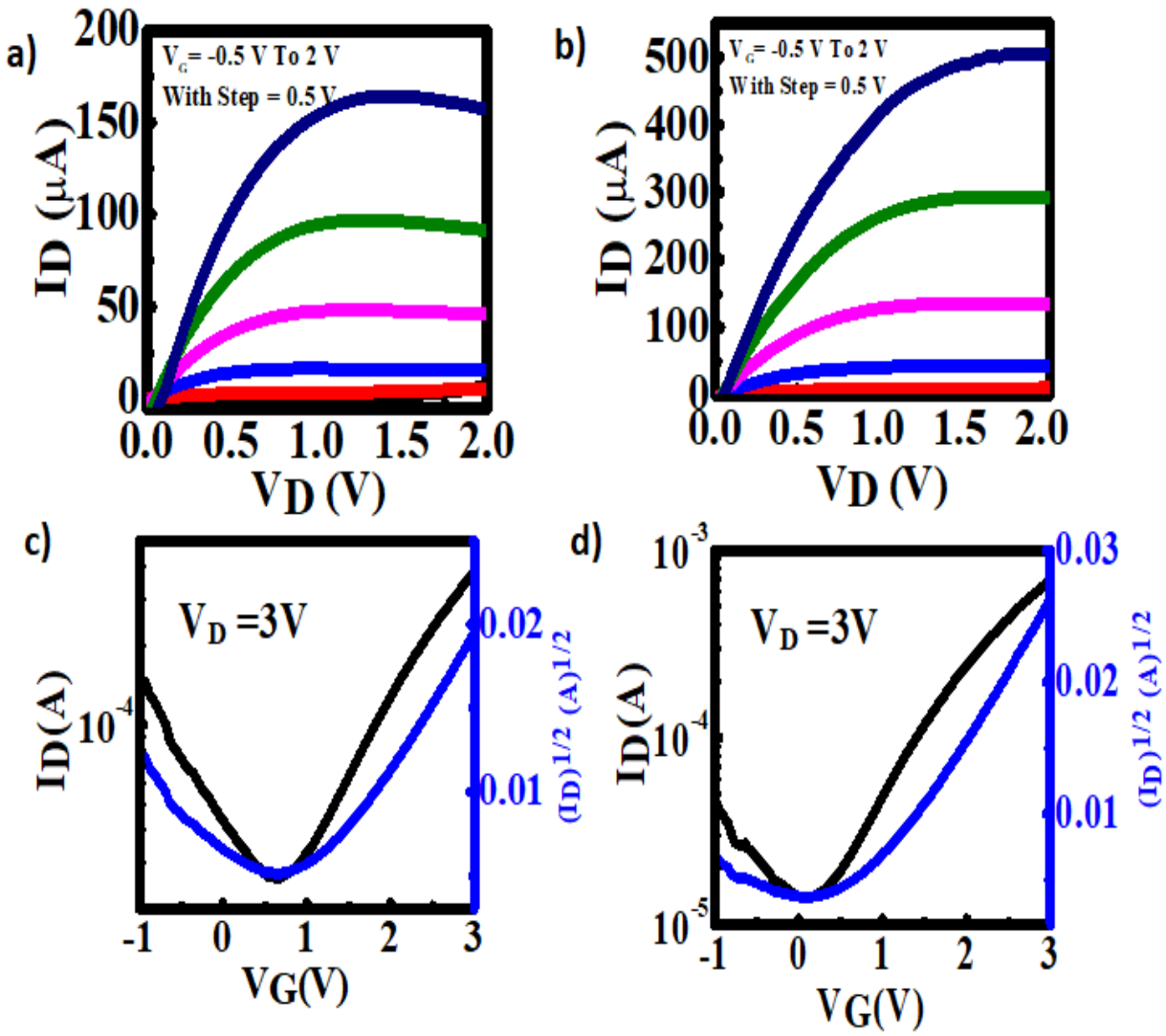

Figure 6.6: Output characteristics of TFTs within 2 V operating voltage a) Device-1 b) Device-2. Transfer characteristics of TFTs within 2 V operating voltage c) Device-1 d) Device-2.

Table 6.2: Device parameter of TFTs extracted from electrical characterization

Device	**Dielectric**	**On/Off ratio**	**Electron mobility[$cm^2V^{-1}s^{-1}$]**	**Threshold voltage[V]**	**Trap state Density [cm^{-2}]**	**Sub threshold Swing [V/dec]**
Device-1	Li_2SnO_3	14	3.04	0.65	4.9×10^{13}	1.6
Device-2	TiO_2/ Li_2SnO_3	50	3.47	0.20	6.35×10^{13}	1.23

The induced charge accumulation of semiconductor/dielectric interfaces by an additional TiO_2 layer is thought to be responsible for the noticeable improvement in TFT performance. The mechanism of this induced charge accumulation may be understood with the help of a model that is schematically presented in **figure 6.7**. At $V_G=0$, electron transfer from TiO_2 thin film to Si substrate because of potential difference at the p^{++}-Si/n-TiO_2 interface. As a consequence, a depleted positive charge layer is formed in the TiO_2 film which induces electron accumulation at the interface region of the SnO_2 film. When the gate bias is $V_G>0$, the TiO_2 layer becomes more positively charged due to the additional electron transfer from TiO_2 to the p^{++}-Si substrate. As a result, a relatively larger number of electrons are accumulated in the dielectric interface of the channel, as described in **figure 6.7 b**. In contrast, no electron transfer occurs either at zero bias or $V_G>0$ from dielectric to the p^{++}-Si substrate for single-layered Li_2SnO_3 based TFT which can induce such additional electron accumulation in the channel. Therefore, a comparatively larger gate bias is required to accumulate sufficient electrons in the transistor channel, causing a higher V_T of Device-1. As a consequence, the overall drain current for Device-1 for certain gate bias in accumulation mode is much lower than Device-2. From the band diagram illustration, it is clear that the electron donation from the TiO_2 layer is possible because of the electron transfer from TiO_2 to p^{++}-Si. Because of this mechanism, we found better TFT performance in terms of mobility and SS by using the TiO_2 layer.

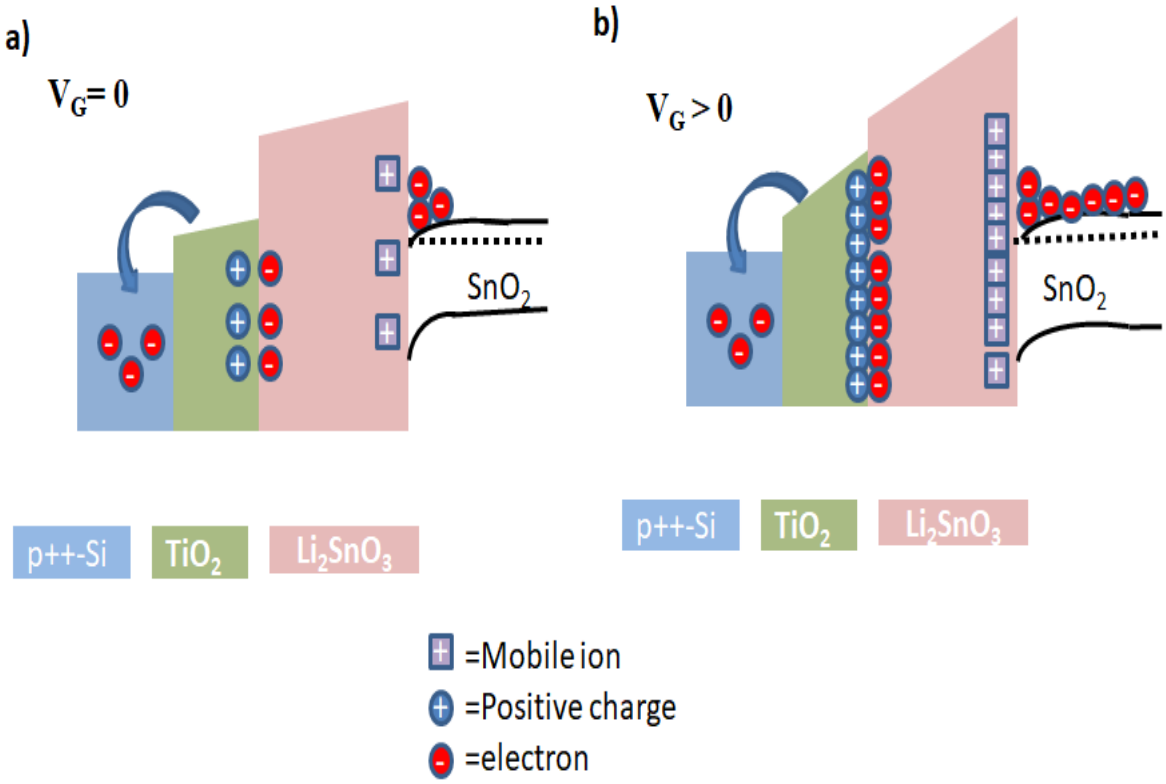

Figure 6.7: Energy band diagram of bi-layered TiO_2/Li_2SnO_3 stack dielectric under a) $V_G=0$ and b) $V_G>0$

6.5 Conclusion

In conclusion, Li_2SnO_3 thin film was deposited in a sol-gel technique which shows a good electrical insulating behavior. In addition, due to good ionic conductivity, Li_2SnO_3 thin film shows a high areal capacitance. A SnO_2 TFT has been fabricated by using the high capacitive Li_2SnO_3 thin film as the gate dielectric which can operate within 3.0 V external bias. The performance of SnO_2 TFT has been improved by utilizing TiO_2 thin film in between the p^{++}-Si and Li_2SnO_3 gate interface layer. A relative study of these two TFTs (with and without TiO_2 interface) revealed that the TiO_2 interface induced electron carrier in the channel of TFT that virtually reduces threshold voltage and the sub-threshold swing of the device. Furthermore, gate leakage current is significantly reduced, which aids in improving the device on/off ratio. Moreover, the addition of the TiO_2 layer enhances the areal capacitance of the stack dielectric film. As a consequence, saturation in drain current has been achieved at lower gate bias. This bilayered TiO_2/Li_2SnO_3 dielectric-based TFT showed carrier mobility of

3.47 V $cm^2V^{-1}s^{-1}$, on/off ratio of 50, interface states $6.35\times10^{13}/cm^{2,}$ and sub-threshold swing of 1.23 V/decade. Overall, this study reveals that tin oxide not only shows good semiconducting behavior, but Li-ion incorporation in a suitable ratio can make it a good insulating material that can be utilized as a gate dielectric of a low operating voltage TFT.