Chapter 4

Solution processed $SrTiO_3$ thin film as Gate dielectric of SnO_2 thin film transistor.

Chapter-4

4.1 Introduction-

Perovskite oxide materials have a general formula of ABO_3 and have created significant attention due to their numerous structural properties and extensive applications such as dielectric,[172] piezoelectrics,[173] ferromagnets, antiferromagnets, and multiferroics materials.[174, 175] Besides, their versatile electrical conductivity and their tunability make it possible to use these materials as semiconductors [176] and superconductors [177]. All these materials' functionality of perovskite oxide can be modulated through the alternation of interaction between lattice, spin, charge, and orbital degrees of freedom which is commonly done through different doping,[178] heterojunction, and epitaxial thin film formation.[175, 179] Particularly for charge transport modulation, epitaxial growth and heterojunction formation techniques of perovskite oxide materials are widely reported.[180, 181] Most of those charge transport modulations originated due to two-dimensional free electron gas and interface charge transfer.[182, 183] For these charge transport studies, a large number of perovskite oxide materials and their interfaces are reported in literature such as $SrTiO_3$, $BaTiO_3$, $LaAlO_3$, $BaSnO_3$, $SrSnO_3$ etc.[184, 185] Among them, for electronics device application, heterostructure with $SrTiO_3$ has been used mostly as a semiconductor.[176, 184] Besides, a good number works also reported application of $SrTiO_3$ as dielectric insulator.[186, 187] The thin film of $SrTiO_3$ has high dielectric constant (high-k) and good optical transparency. Therefore by making them a good insulating layer, it's possible to utilize this material for the application of gate dielectric of a low operating voltage thin film transistor.[115, 188, 189] Although, so far all these $SrTiO_3$ thin films those are used for TFT application are deposited through different physical vapor deposition techniques only.

In my Ph.D. thesis work, I have developed polycrystalline $SrTiO_3$ thin film by a solution-processed that shows extremely low electrical conductivity with quite good areal capacitance. Besides, the surface roughness of this thin film is also quite low. The leakage current and frequency dependence capacitance of this thin film has been studied with a metal-insulator-metal (MIM) device structure. Besides this, I have successfully utilized this thin film as a gate dielectric of a thin film transistor (TFT). Solution-processed amorphous tin oxide has been used as a semiconductor for this device. Due to this high areal capacitance of this $SrTiO_3$ thin film; TFT required only 2 V external voltage to run this device. Besides, TFT also shows reasonably good mobility and a quite good on/off ratio. Details of this study are given in the following section.

4.2 Thin film transistor (TFT) Fabrication

All these TFTs are fabricated in a bottom gate top contact thin-film transistor on a heavily doped cleaned Si substrate (p^{++}-Si) through a solution process method. Sol-gel-derived $SrTiO_3$ thin film has been used as gate dielectric and SnO_2 works as a semiconductor channel. The synthesis of these precursor materials and substrate cleaning have been discussed in the experimental section of this thesis (Chapter-2). The schematic device structure of this TFT has been shown in **figure 4.1**. After substrate cleaning, the precursor sol of $SrTiO_3$ was spin-coated over these substrates for 40 seconds at 4000 rpm under ambient air conditions. The substrates were placed on a preheated hot plate at 90˚C for 2 minutes after spin coating to remove the solvents and dry them. The samples were annealed in a furnace at 350˚C for 30 minutes after drying. After that, the thin film was annealed at 750˚C to obtain the polycrystalline phase of $SrTiO_3$. Cross-sectional SEM measurements revealed the thickness of $SrTiO_3$ thin film

is 60 nm. After dielectric coating, a precursor solution of SnO_2 (300 mM) solution was spin-coated onto the $SrTiO_3$ coated p^{++}-Si substrate followed by a drying Process for 5 minutes at 90˚C on a preheated hot plate. These dried samples were promptly annealed for 30 minutes in a preheated high-temperature furnace at 500˚C, resulting in a polycrystalline SnO_2 film. Finally, a thermal evaporator was used to deposit the aluminum source and drain electrodes on top of the SnO_2 layer at a pressure of 6 x 10^{-6} pa, using a shadow mask with a W/L (23.6mm/0.2 mm) ratio of 118).To test the capacitance and dielectric behavior of $SrTiO_3$ material, the thin-film device with a metal-insulator-metal (MIM) device structure was made using the same procedure.

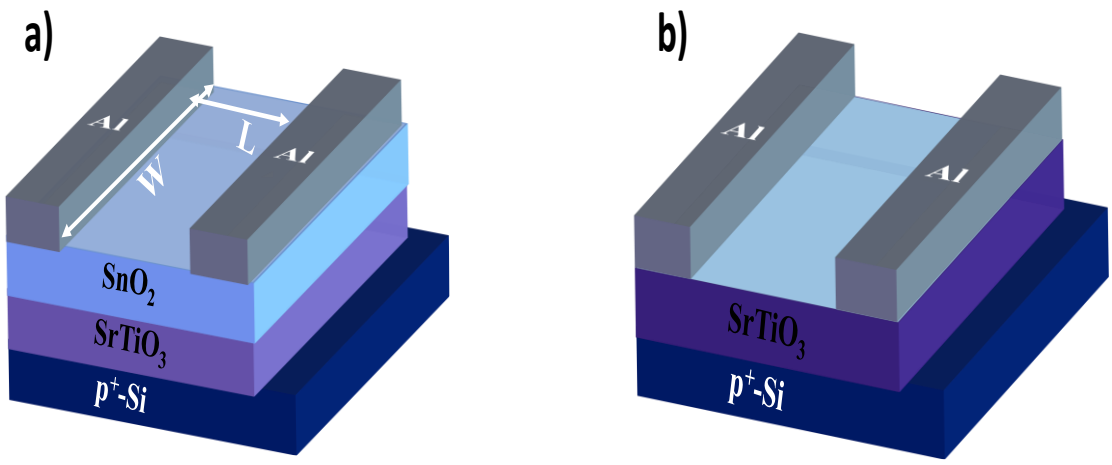


Figure 4.1: Device Layouts of a) Schematic of solution-processed metal-oxide TFT b) MIM structure.

4.3 Result and Discussion-

4.3.1 Thermal Analysis

The thermal behavior of sol-gel-produced STO powder was examined using thermos gravimetric analysis (TGA) at a heating rate of 20˚C /min from ambient temperature to 1000˚C in a nitrogen environment shown in **figure 4. 2**. The loss of physically adsorbed water molecules on the STO surface can be attributed to the initial weight loss (3.3%) within the range from 73˚C to 123˚C. Second weight loss (5.1%) was observed from 255˚C to 326˚C, ascribed to the loss of chemisorption fluids and decomposition salts and organics components such as 2-methoxy ethanol. Third mass loss is observed in between 556 and 667˚C which is ~ 22.9%, mainly due to the breakdown of residual organics. Then, in the range of 630–900˚C, weight loss is minimal, suggesting that STO has a broad crystallization window.

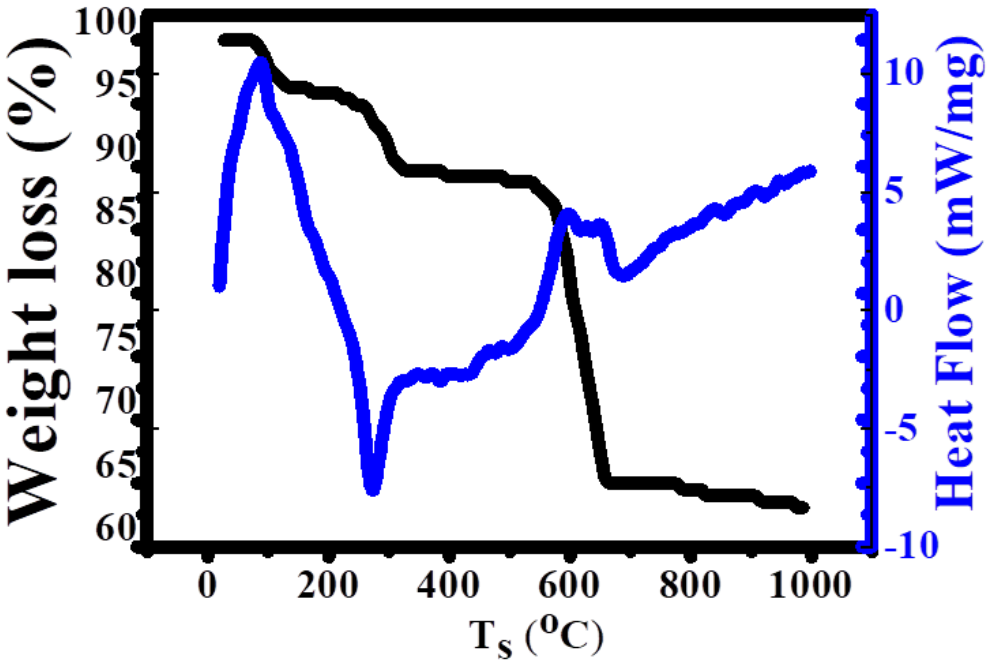


Figure 4.2: TGA and DTA graph of $SrTiO_3$ powder

4.3.2 Structural Analysis of the Thin Film and Powder of STO Dielectric

X-ray diffraction (XRD) and Grazing Incidence X-ray Diffraction (GIXRD) measurements were carried out on powder and thin-film samples, respectively, for structural studies of STO. **figure 4.3** shows the GIXRD of solution-processed STO thin films that were annealed at 350˚C /0.5 h, and 750˚C /0.5 h, respectively. The $SrTiO_3$ powder calcined at 750˚C exhibit a clear crystalline phase with diffracted peak generated from the planes of the reflections of (100), (110), (111), (200), (210), (211), (220), (300) and (310) at 2θ angles of around 22.57°,32.30°, 40.05°,46.35°,52.23°,57.68°,67.84°, and 77.31°, respectively, according to these GIXRD results. The diffractogram reveals well-defined peaks with high crystallinity. The d values of peaks and intensities are quite similar to those on JCPDS# 894934. $SrTiO_3$ was found to be polycrystalline, and the micro crystallites were cubic in shape, with lattice constants of a=b=c=3.90 Å.

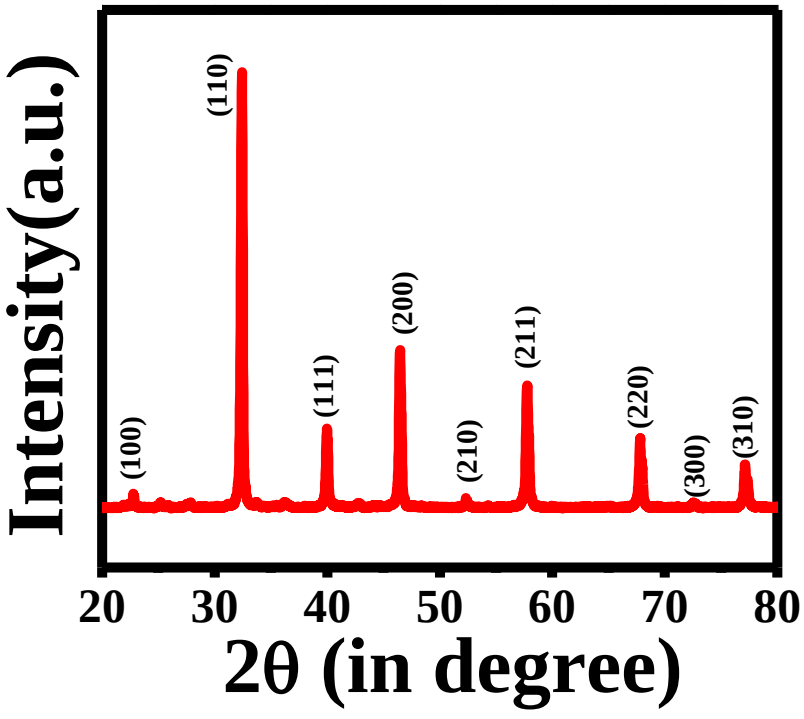


Figure 4.3: XRD pattern of $SrTiO_3$ Powder.

4.3.3 Optical Properties of Dielectric $SrTiO_3$ Thin Films-

Thin films of $SrTiO_3$ were deposited on a quartz substrate for optical transparency study that has been coated under the same conditions as TFT dielectric deposition. The transmittance value of this thin film is shown in **figure 4.4 a** which indicates the average transmittance of $SrTiO_3$ thin film is more than 90% within the range from 300 to 800 nm.

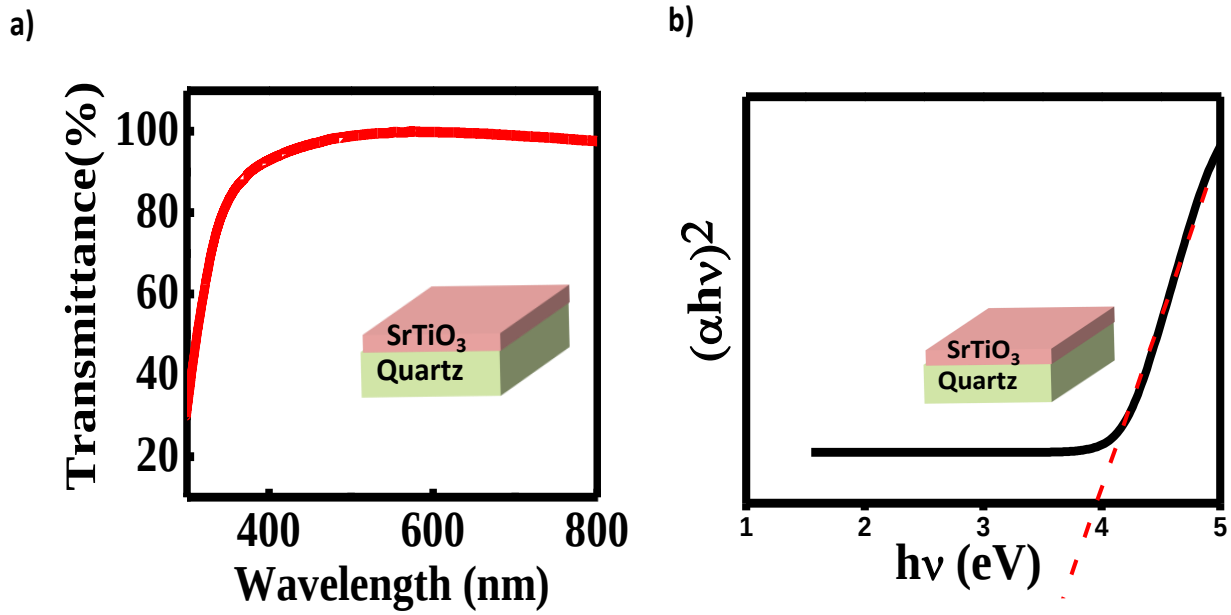


Figure 4.4: a) Optical transmittance spectra, b) optical band gap of $SrTiO_3$ thin film annealed at 750˚C.

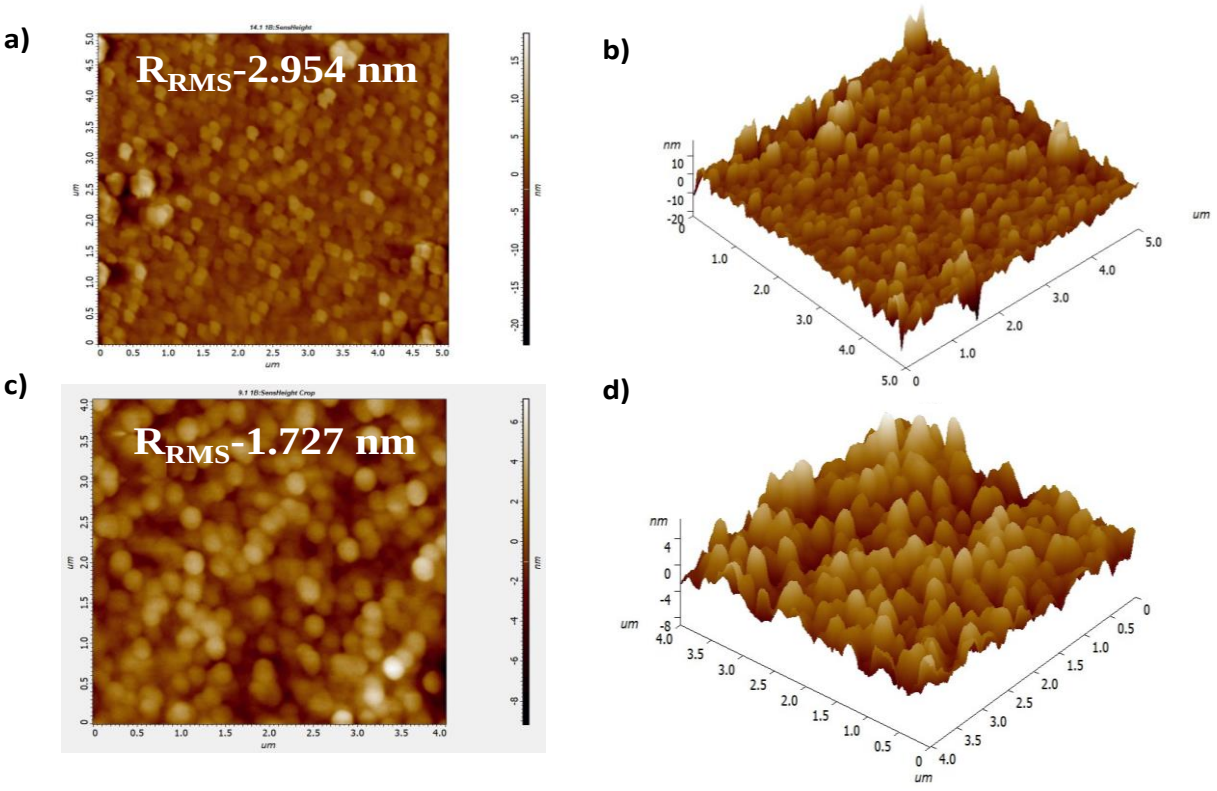
Using the optical absorption coefficient (α) of $SrTiO_3$ thin film, the optical band gap (Eg) of the STO dielectric thin film has been extracted by using the following relation,

$$(\alpha h\nu)^2=A(h\nu-E_g)\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Where hν is the energy of the photon. The extracted optical band gap Eg of this STO thin film is 3.98 eV was determined by extrapolating the linear portion of the plot relating $(\alpha h\nu)^2$ vs. hν plot. The optical band gap is comparable to that of the single crystals $SrTiO_3$ at room temperature.[188]

4.3.4 Surface Morphology of $SrTiO_3$ and $SrTiO_3/SnO_2$ Thin Films

The surface morphology of $SrTiO_3$ and $SrTiO_3/SnO_2$ stacked thin film were investigated by atomic force microscopy (AFM) as shown in **figure 4.5.** For this investigation, the precursor sol of STO dielectrics was deposited on the p^{++}-Si substrate under a similar condition to the TFT fabrication. This study indicates that the root-mean-square (RMS) roughness of $SrTiO_3$ thin film surface is 2.9 nm which is smooth enough for TFT fabrication and capable to provide a good dielectric/Semiconductor interface. The roughness of $SrTiO_3/SnO_2$ is 1.7 nm implies that the SnO_2 semiconductor doesn't change the surface roughness of the film. The 3-D images of $SrTiO_3$ and $SrTiO_3/SnO_2$ stacked thin film are shown in **figures 4.5 b** and **d** respectively, which implies that this roughness is distributed through the film in a similar way.



Fgure 4.5: 2-D and 3-D Surface morphologies of the solution processed $SrTiO_3$ dielectric thin films for (a), (b), p^{++}–Si/ $SrTiO_3$, (c),(d), p^{++}–Si/ $SrTiO_3/SnO_2$.

4.3.5 Capacitance and Electrical Measurements of $SrTiO_3$ Thin Film

With a device structure of p^{++}–Si/$SrTiO_3$/Al, the leakage current density and frequency-dependent capacitance of $SrTiO_3$ thin films were investigated which are shown in **figure 4.6 a** and **figure 4.6 b** respectively. For this study $SrTiO_{3,\ the}$ thin film was coated under the same condition as of dielectric thin film deposition of TFT. **Figure 4.6a** reveals that the leakage current density of $SrTiO_3$ thin film is 1.08 x 10^{-5} A/cm^2 at 5-volt external bias which is reasonably low and good enough for operating TFT up to 5V.

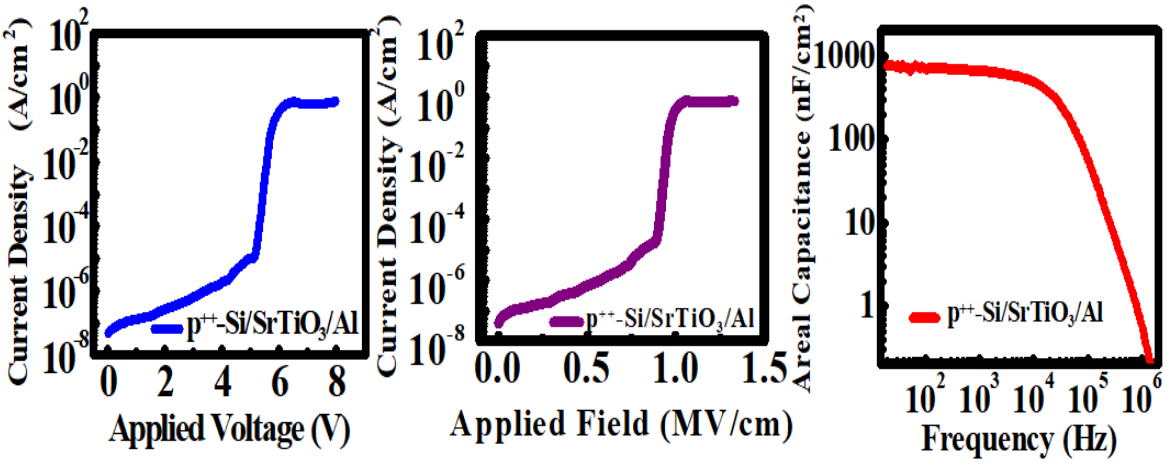


Figure 4.6: Variation of (a) leakage current density vs applied voltage, (b) leakage current density vs applied field, and (c) capacitance vs frequency of $SrTiO_3$ gate dielectric with MIM device architecture.

Frequency-dependent capacitance (C-f) measurement was carried out in the range of 20 Hz to 1 MHz to investigate the dielectric behavior of $SrTiO_3$ thin film as shown in **figure 4.6 c**. This data shows that the areal capacitance has a small variation up to the

frequency of 5 kHz and it rapidly drops above 10 kHz. At 50 Hz, the measured areal capacitance of $SrTiO_3$ thin film is ~737 nF cm^{-2}, which is significantly higher than similar thickness SiO_2 dielectric and previously reported solution processed high-κ dielectrics. As a result, a $SrTiO_3$ thin film is a viable option for use as a gate dielectric in a low operating voltage TFT fabrication.

Table 4.1 Current densities, areal capacitance per unit area of a dielectric film

Dielectric	**Areal capacitance C (nF/cm^2)(at 50 Hz)**	**Leakage current density at 5 V bias (A/cm^2)**
$SrTiO_3$	737	1.08×10^{-5}

The cross-sectional SEM image is used to estimate the thickness of the dielectric films as shown in **figure 4.7** it was 60 nm. Using this film thickness, the dielectric constant of $SrTiO_3$ thin film is calculated by using the formula $C=k\varepsilon_0 A/d$, where d is the film thickness. This calculation gives the dielectric constant of $SrTiO_3$ thin film ~ 50 which is quite a high value for using it as a gate dielectric of a low operating voltage TFT.

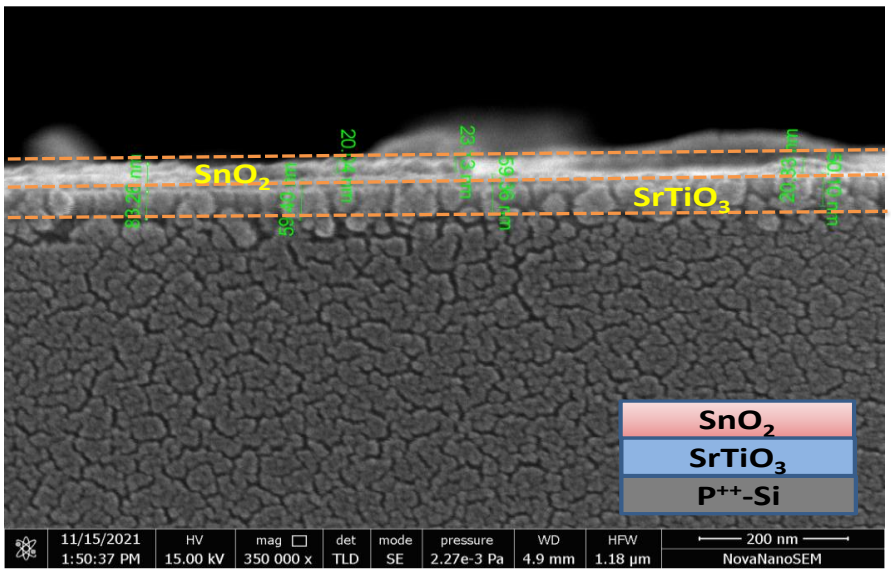


Figure 4.7: Cross-sectional SEM image of Device with a device structure of $SnO_2/SrTiO_3/ p^{++}$-Si.

4.4 Thin Film Transistor Characterization

As mentioned earlier, a TFT with a bottom gate-top contact design with a W/L ratio of 118 (W=23.6 mm; L = 0.2 mm) was fabricated to demonstrate the possibility of $SrTiO_3$ thin film as a gate dielectric (**figure 4.1a**). Transfer and output characteristics of the device are depicted in **figures 4.8 a** and **b**, respectively. **Figure 4.8** shows that the drain current required <2V drain voltage to saturate the I_D when an external gate voltage is within the 2 V range. This data implies that the external bias of 2 V is good enough to run this TFT. On the other hand, **figure 4.8 b** implies that the threshold voltage of TFT is 0.029 V, with an on/off ratio of 2.3×10^4. The effective carrier mobility (μ) and sub-threshold swing (SS) of certain TFTs were calculated from transfer characteristics by using the following equations;

$$\boldsymbol{I_D = \mu C \frac{W}{2L}(V_G - V_T)^2} \ \ldots\ldots\ldots\ldots \quad (1)$$

$$\boldsymbol{SS = \left[\frac{d(log\, I_D)}{d\, V_G}\right]^{-1}} \ \ldots\ldots\ldots\ldots\ldots \quad (2)$$

Gate voltage, threshold voltage, saturation drain current, and capacitance per unit area are represented by V_G, V_T, I_D, and C, respectively. **Table 4.2** shows the retrieved carrier mobility, on/off ratio, threshold voltage, subthreshold swings, and trap state density of TFT. The device's threshold voltage was calculated by extending the straight line of $I_{DS}^{1/2}$ against the V_G curve. The maximum electron mobility was achieved with the device (750˚C annealed–$SrTiO_3$ dielectric TFT) with a value of 0.23 $cm^2V^{-1}s^{-1}$. So far, many efforts have been given to utilize $SrTiO_3$ thin film as a gate dielectric of Si-based field-effect transistor and all of those $SrTiO_3$ thin films are deposited by the different

physical vapor deposition techniques.[190, 191] However, to the best of our knowledge, till now there is no report on solution-processed $SrTiO_3$ dielectric thin film for metal oxide TFT fabrication. Therefore, further study of this sol-gel derived $SrTiO_3$ dielectric with different combinations of metal oxide semiconductor can reduce operating voltage further with high carrier mobility.

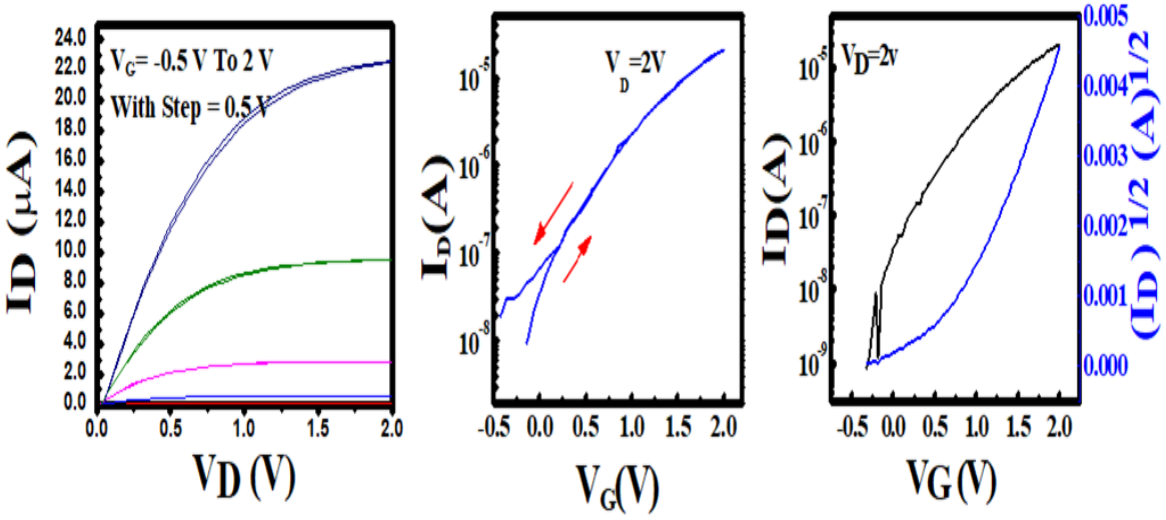


Figure 4.8: (a), (b) Output and transfer characteristics with hysteresis, and (c) transfer characteristics to extract slope for charge carrier mobility calculation for $Al/SnO_2/SrTiO_3/ p^{++}$-Si device structure.

The quality of dielectric/semiconductors is a very crucial issue for the improvement of the overall performance of TFT. This interface introduces surface trap state states that diminish the effective carrier mobility of the device. This interface-states-densities

(N_{SS}^{Max}) is commonly calculated by utilizing the SS value of output characteristics from the following equation;

$$N_{SS}^{Max} = \left[\frac{SS \times log\ e}{\frac{kT}{q}} - 1\right]\frac{C}{q} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Where, the Boltzmann constant and electrical charge are represented by k and q, respectively. The values of N_{SS}^{Max} determined for this TFT is 1.7 x 10^{13} cm^{-2} which is reasonably good for solution-processed metal oxide TFT.

Table 4.2 Device parameter of TFTs extracted from electrical characterization

Dielectric	On/Off ratio	Electron mobility [$cm^2V^{-1}s^{-1}$]	Threshold voltage[V]	Trap state Density [cm^{-2}]	Sub threshold Swing [V/dec]
$SrTiO_3$	2.3 x 10^4	0. 23	0.43	1.7x10^{13}	0.29

4.5 Conclusion

In the conclusion of this chapter, the deposition method of $SrTiO_3$ thin film has been developed by using a low-cost solution processing technique that is compatible with large-area fabrication. The crystalline phase of $SrTiO_3$ was obtained by ambient atmosphere annealing at 750˚C. An optical study of this thin film shows high transparency (>90%) in the visible region which is due to the low scattering from the thin film surface. An electrical study of the MIM device structure reveals that the leakage current density of this thin film is quite low (1.08 x 10^{-5} A/cm^2) up to the

external bias of 5 V which can be a suitable candidate as a gate dielectric of a TFT. Frequency-dependent capacitance study of the MIM device shows a high areal capacitance (737 nF cm^{-2} at 50 Hz) of the thin film which can reduce the operating voltage of TFT significantly. To realize the applicability of $SrTiO_3$ thin film as a gate insulator, a solution-processed SnO_2 TFT has been fabricated that needs only 2.0 external bias to operate this transistor. The extracted carrier mobility and on/off ratio of this device are 0.23 $cm^2 V^{-1} s^{-1}$ and 2.3 x 10^4 respectively. To the best of our knowledge, this is the first demonstration of solution-processed $SrTiO_3$ thin film as a gate insulator for metal oxide TFT. Further study on different metal oxide semiconductors by using $SrTiO_3$ thin film can reduce operating voltage and further high carrier mobility.