Chapter 3

Solution-processed $Pb_{0.8}Ba_{0.2}ZrO_3$ as a gate dielectric for low-voltage metal-oxide thin-film transistor

3.1 Introduction

Recently, there is a surge of interest in searching for solution-processed high dielectric constant (k) inorganic gate insulators as a key element of the low-voltage thin-film transistor.[155] Due to their high dielectric constant and coherent interface with oxide semiconductors, they lead to immense improvement in device performance. These low operating voltage metal-oxide thin-film transistors (TFTs) are of particular interest for next-generation display technology, and optoelectronics applications including light-emitting transistors [156] and photo transistors[157] because of their high mobility with high transparency. These TFTs can be deposited by both different vacuum-based depositions as well as solution-processed fabrication. Usually, high vacuum-based deposition like pulsed laser deposition, atomic layer deposition, RF magnetron sputtering, etc. is expensive processes sometimes not suitable for low-cost large-area electronics. In contrast, the fabrication of metal oxide thin films by solution processing is cost-effective and suitable for mass production.[158, 159]

A ferroelectric field-effect transistor (FeFET) was started its journey in the 1950s, particularly for its application in nonvolatile random access memory. That application becomes more important over the last several decades because of its requirement for high speed, low power consumption, and nondestructive readout operation.[160-163] Among different ferroelectric materials, $PbZrO_3$ (PZT) thin films are mostly investigated [164, 165], however, due to its oxygen vacancies, PZT creates a problem of polarization fatigue.[166] It was also reported that this fatigue resistance nature could be improved by decreasing the oxygen vacancies by the addition of Ti content.[167]Comparatively, $(Pb_{1-x}Ba_x)ZrO_3$ (PBZ), which is another well-known

ferroelectric material of simple perovskite structure, shows the better fatigue resistance that can be further improved by doping of Nb [168], which is suitable for memory application.
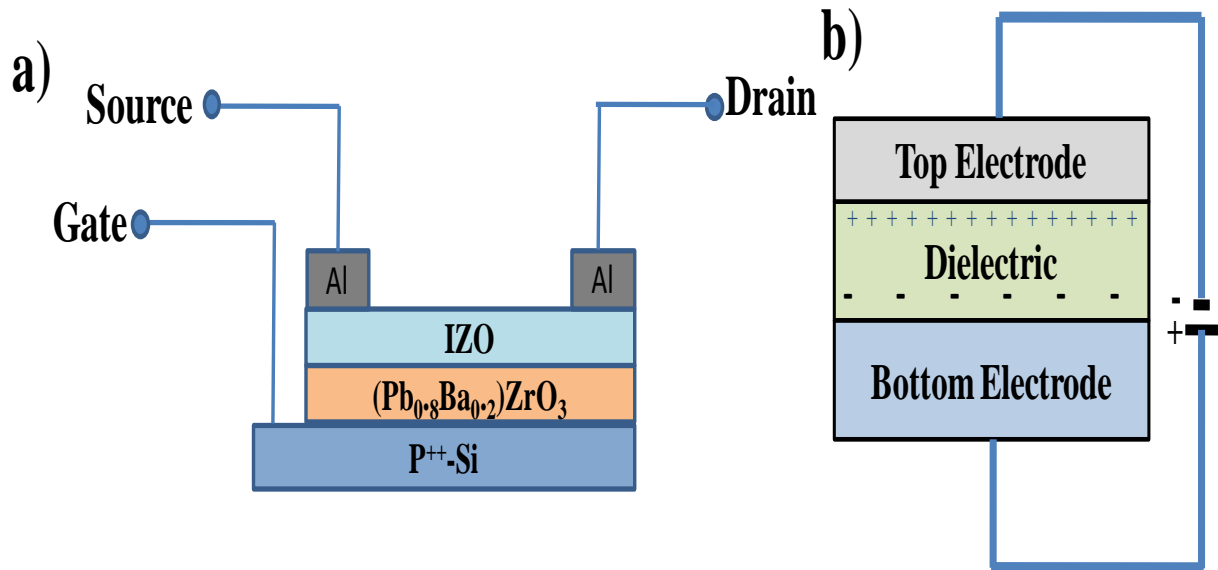

Figure 3.1: a) Schematic of solution-processed metal oxide TFT **b)** Polarization mechanism of the dielectric film under external bias.

In this Chapter, we use $(Pb_{1-x}Ba_x)ZrO_3$ (x = 0.2) as a gate dielectric for a thin-film transistor as it has a high dielectric constant and high fatigue resistance which is favorable for device performance and lifetime.[168] This PBZ has been prepared through cost effective-sol-gel method and deposited by spin coating method on a heavily doped Si substrate (p^{++} -Si). Indium zinc oxide (IZO) has been used as a channel semiconductor for bottom-gate top contact TFT. This device required < 5.0 V to operate which is a basic requirement for portable device applications.

3.2 Results and Discussion

3.2.1 Thermal Analysis-

The thermal behavior of sol-gel synthesized PBZ powder was investigated by thermogravimetric and differential thermal analysis (TGA/DTA) with a heating rate of 20˚C/min from room temperature to 900˚C in a nitrogen atmosphere as shown in **figure 3.2**. It was observed that there was an abrupt weight loss in $(Pb_{0.8}Ba_{0.2})ZrO_3$ at around 410˚C, which is mainly due to loss of moisture and volatile solvents. At the same time, the corresponding DTA peak shows the dehydroxylation and thermal decomposition of hydroxides. There is no significant weight loss in the temperature range from 550˚C to 850˚C. The exothermic peak Around 550˚C and 850˚C are associated with the crystallization of sol-gel powder of $(Pb_{0.8}Ba_{0.2})ZrO_3$. Based on this behavior, PBZ coated samples were annealed at 550˚C and 850˚C for the formation of the dense and pure polycrystalline thin film.
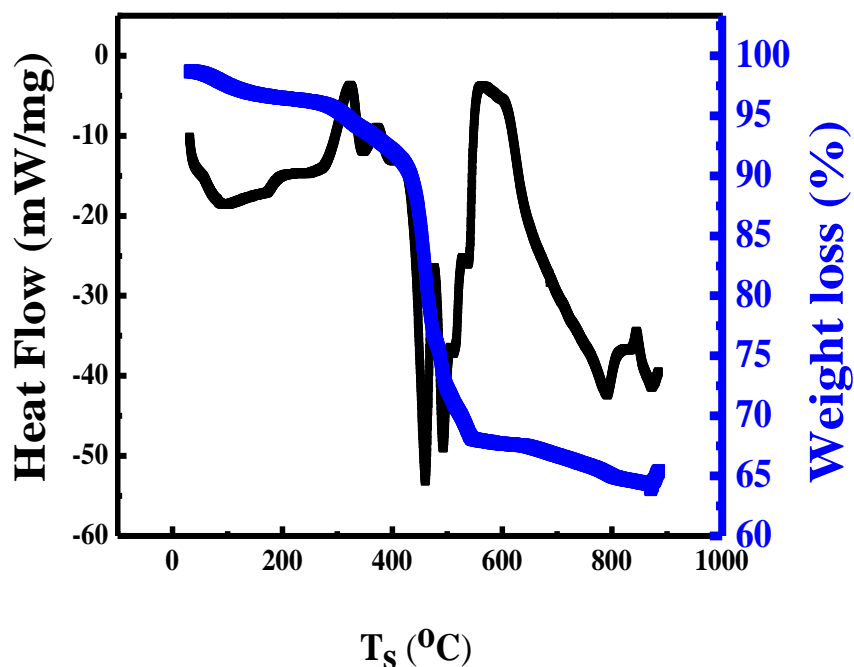

Figure 3.2: Thermal behavior of sol-gel synthesized PBZ Powder annealed at 830˚C.

3.2.2 Structural properties of the powder of $(Pb_{0.8}Ba_{0.2})ZrO_3$

To ensure the crystalline phase of $(Pb_{0.8}Ba_{0.2})ZrO_3$, XRD measurement was performed within the diffraction range from 20° to 70° which is shown in **figure 3.3**. For this measurement, the sol-gel-derived powder was heated at 850 °C for 2 h. The XRD data shows a clear $(Pb_{0.8}Ba_{0.2})ZrO_3$ crystal formation without any impurity phase which indicates that, at this temperature lead acetate, barium carbonate, and zinc acetate are completely converted into single-phase $(Pb_{0.8}Ba_{0.2})ZrO_3$.[169] The diffraction peaks at an angle around 38° and 43° that originated from the plane of reflections of (111), (200), indices stand for the cubic crystal phase. We preferred this crystalline phase of dielectric materials because of its higher capacitance than the amorphous phase. This higher capacitance dielectric thin film enables us to fabricate low operating voltage TFT.
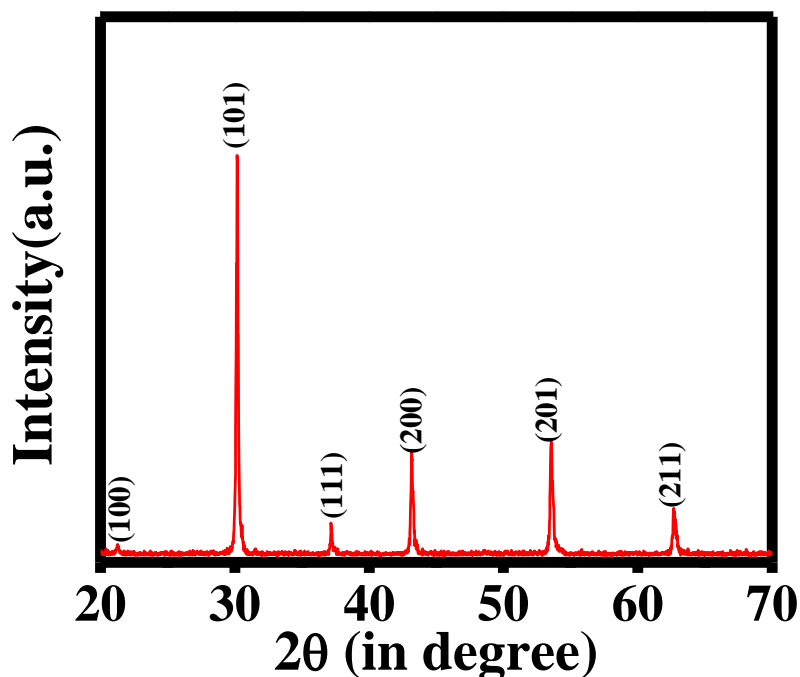

Figure 3.3:   XRD pattern of sol-gel synthesized PBZ powder annealed at 830˚C.

3.2.3 Optical properties of $(Pb_{0.8}Ba_{0.2})ZrO_3$ thin films

The optical transmission spectra of solution-processed $(Pb_{0.8}Ba_{0.2})ZrO_3$ thin film are shown in **figure 3.4**. For this measurement, a thin film of $(Pb_{0.8}Ba_{0.2})ZrO_3$ was deposited on a quartz substrate followed by an annealing temperature of 830°C. The optical transmission spectra elucidate that it has high transmittance of ~ 94% in the visible region (400–700 nm), which indicates the dielectric surface is very defective and impurity-free. Such a type of film is preferable to diminish the leakage current and improve the TFT performance.
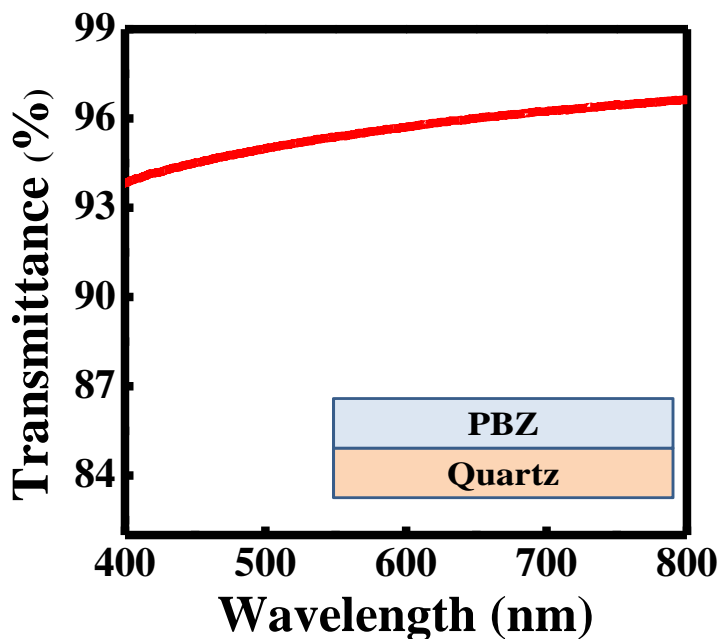

Figure 3.4: Optical transmittance spectra of PBZ thin film annealed at 830°C

3.2.4 Surface Morphology

This is well known that the surface roughness of the dielectric plays a very crucial role in the device's performance. Because a smooth dielectric surface provides fewer traps at the dielectric/semiconductor interface.[127] On the other hand, a rough

dielectric/semiconductor interface hinders the transportation of charge carriers in semiconductors, and hence the overall mobility of TFT reduces. Therefore surface morphology of p^{++} -Si/$(Pb_{0.8}Ba_{0.2})ZrO_3$ dielectric thin film annealed at 830 °C was investigated by atomic force microscopy (AFM) as shown in **figure 3.5**. The roughness of the dielectric is 4.6 nm which is comparable to other reported dielectrics for TFT.[170] The 3- D image of the dielectric film also reflects the same thing. Therefore it makes a smooth dielectric/semiconductor interface which is beneficial for the fabrication of high-performance TFT.
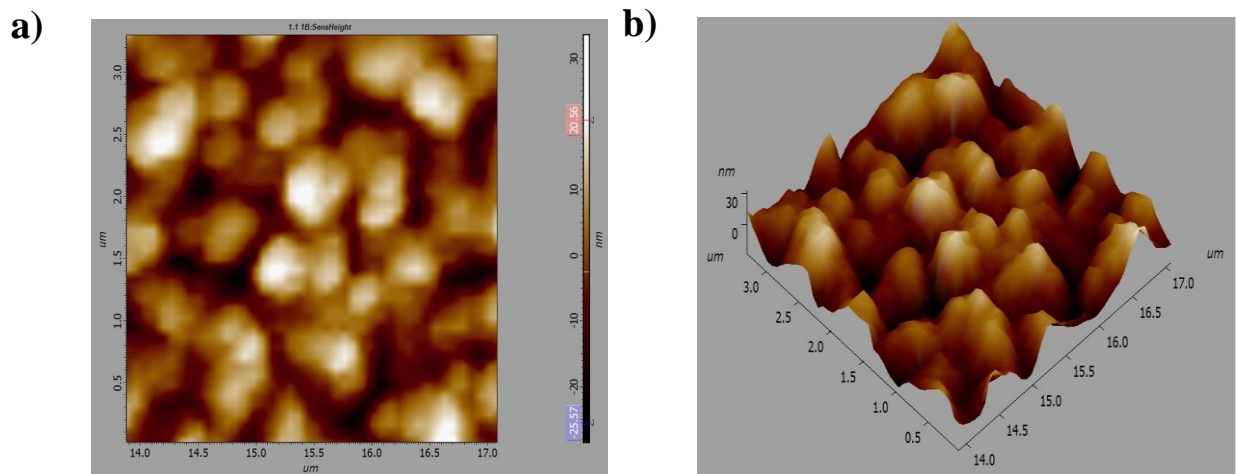

Figure 3.5:   (a) 2-D AFM images of PBZ film annealed at 830 °C (b) 3-D AFM images of PBZ film annealed at 830 °C

3.3 Device characterization

In a view to perceive, the dielectric properties of $(Pb_{0.8}Ba_{0.2})ZrO_3$ thin films have been studied in a metal-insulator-metal (MIM) device architecture (p^{++} -Si/ $(Pb_{0.8}Ba_{0.2})ZrO_3$/Al) to realize frequency-dependent capacitance (c-f) of the material. The current voltage (I-V) measurement has been performed in the same device to

understand the leakage property of the PBZ dielectric. The frequency-dependent capacitance (c-f) behavior of (p^{++}-Si/ ($Pb_{0.8}Ba_{0.2}$)ZrO_3/Al) is shown in **figure 3.6b**. As expected, the capacitance of ($Pb_{0.8}Ba_{0.2}$)ZrO_3 thin film decreased with increasing frequency because of a decrease in polarization response time. However, the capacitance value decreases slightly up to 10^5 Hz which is less than 5% of the capacitance value at 20 Hz. This variation is quite small and observed in most of the gate dielectric materials. However, above 10^5 Hz, other polarization effects like dipole orientation polarization fail to contribute, and subsequently overall capacitance drops. This phenomenon has been observed earlier in a similar class of materials [20]. The capacitance value of ($Pb_{0.8}Ba_{0.2}$)ZrO_3 thin film is 65 $nFcm^{-2}$ at 50 Hz, which is significantly larger compared to conventional thermally grown SiO_2 and other insulators. From a cross-sectional scanning electron microscope (SEM), the image of the p^{++} -Si/PBZ/IZO device **(figure-3.6 c)** shows the thickness of the dielectric layer is ~ 140 nm. Using capacitance value of 20 Hz calculated dielectric constant of this PBZ dielectric 12. Therefore, the synthesized dielectric by sol-gel method is suitable for low operating voltage TFT. After performing the current-voltage (I-V) measurements on metal-insulator-metal (MIM) device architecture, we assured that the leakage current of ($Pb_{0.8}Ba_{0.2}$)ZrO_3 thin film is very low which is because of its higher band gap and uniform film of our dielectric. The leakage current density at an operating voltage of 10 V is 1 $\mu A/cm^2$ .with a breakdown voltage of ~ 25 V which is much higher than the normal operating device > 5 V as shown in **figure 3.6 a**). Hence, solution-processed ($Pb_{0.8}Ba_{0.2}$)ZrO_3 is suitable to use as a gate dielectric for TFT fabrication.
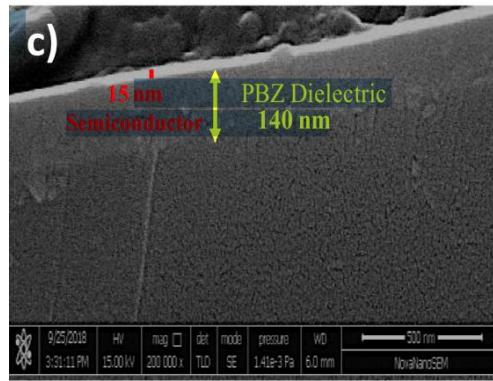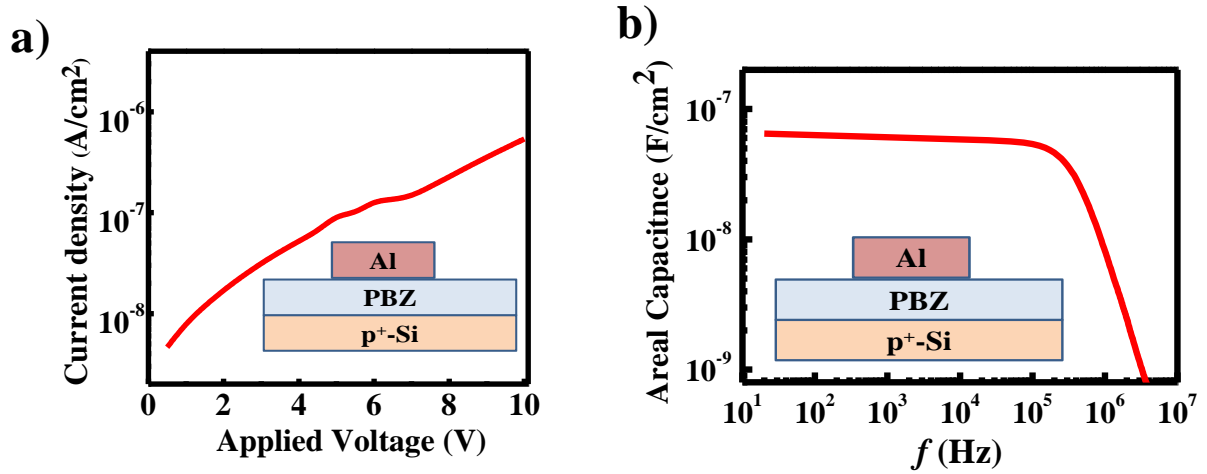
Figure 3.6: (a) Leakage current vs. applied voltage (b) capacitance vs. frequency (c–f) measurement with MIM device structure (c) cross-sectional scanning electron microscope (SEM) image of p^{++} -Si/PBZ/IZO device.

To make sure the worthiness of $(Pb_{0.8}Ba_{0.2})ZrO_3$ as a gate dielectric, bottom-gate top-contact TFT devices were fabricated on p+ -Si substrate with IZO as a channel layer. Al metal electrodes were used as a source and drain contact and deposited through a shadow mask to maintain channel width to length ratio 118 (W = 23.6 mm; L = 0.2 mm). The output and transfer characteristics of TFT that are measured under ambient atmosphere are shown in **figure 3.7**. The drain voltage was double swept from 0 V to 5 V and gate voltage from − 5 V to 5 V for an 830 °C annealed $(Pb_{0.8}Ba_{0.2})ZrO_3$ TFT device. From **figure 3.7**, it is clearly depicted that the device show n-channel transistor behavior with low-voltage (< 5 V) saturation. At the same time, these characteristics

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show negligibly small hysteresis behavior in both characteristics. There is no congregation at low V_{DS} which means there is good ohmic contact between a semiconductor, and Al electrode and device performance are not affected by contact resistance. It is also clear that saturation current is achieved below 3 V which is desirable for low-power electronics. The effective carrier mobility (μ) and sub-threshold voltage (SS) of TFT were calculated from the following equations;

$$I_D = \mu C \frac{W}{2L}(V_G - V_T)^2 \qquad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1)$$

$$SS = \left[\frac{d(log\ I_D)}{dV_G}\right]^{-1} \qquad \cdots\cdots\cdots\cdots\cdots \quad (2)$$

where I_D= saturation drain current, C = capacitance per unit area, V_G = gate voltage, and V_T = threshold voltage. By considering the capacitance of dielectric PBZ thin film at 50 Hz, the frequency is 65 nF cm^{-2}; the calculated mobility of TFT is 4.5 cm^{2}v^{-1}s^{-1} with an on/off ratio of 5×10^3 which is comparable to the previously published research work of the solution-processed TFT.[118] On/off ratio can be improved further by inserting another high-k dielectric layer either between the gate electrode and PBZ dielectric or active channel and PBZ dielectric layer.[154, 171] The value of subthreshold swing is 0.35 V/decade which is acceptable for solution-processed TFT.
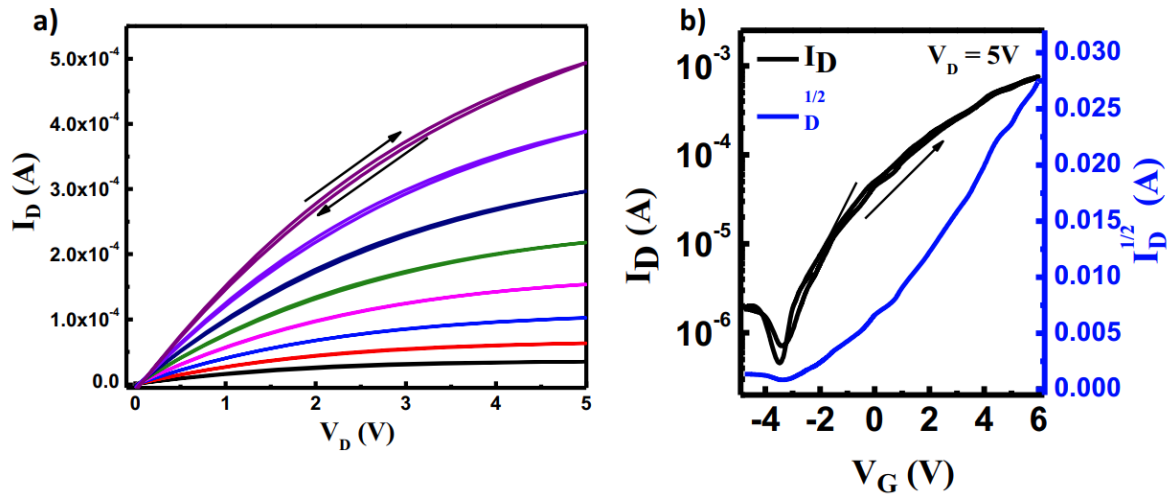
Figure 3.7: (a) output and (b) transfer characteristics of PBZ/IZO TFT

We have also checked our device repetitively, and after aging for 30 days, we did not find any significant variations in device performance which shows that the TFT is highly stable in an open atmosphere "Bias stress stability" is one of the best measurements of the device to check the stability of the device during applied bias in ambient atmosphere. Therefore, the stability test was performed with the same device. The figure shows the multiple transfer characterization for 30 min keeping 3 min at V_G = 5 V. The device with PBZ dielectric thin film shows no significant variation in transistor parameters such as on/off ratio, mobility, and subthreshold swing. These indicate that our dielectric and semiconductor are stable under the biasing and utilized as a gate dielectric in the thin-film transistor. **Figure 3.8** shows the multiple transfer characteristics of TFT for 30 min keeping an interval of 3 min at constant gate voltage (V_G) = 5 V.
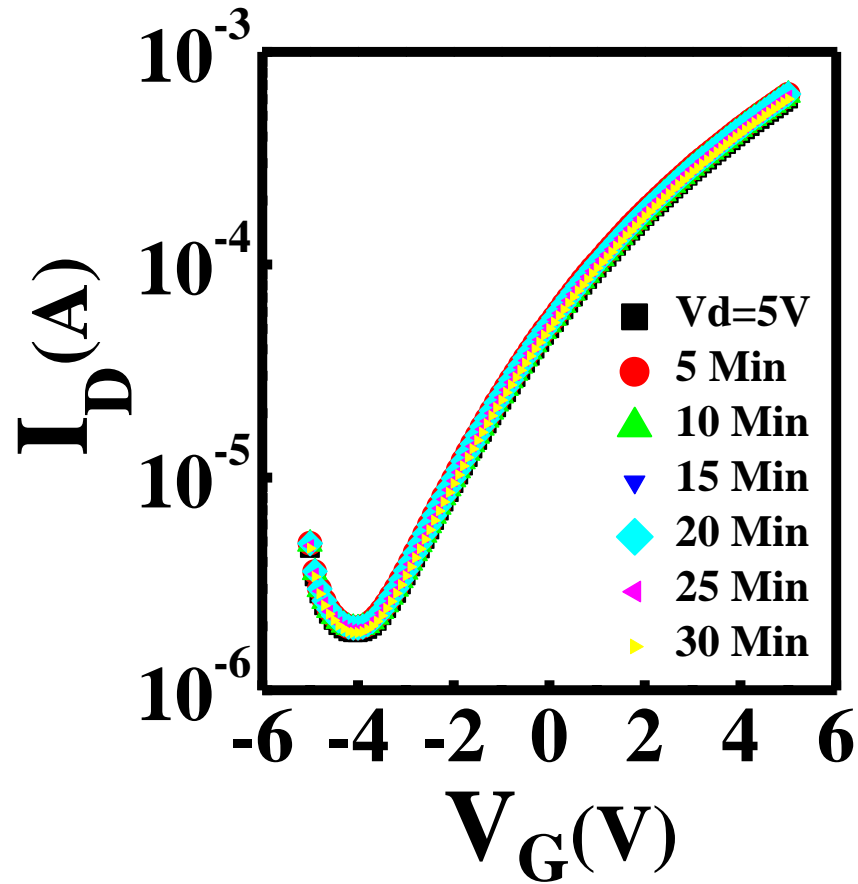
Figure 3.8: Operational Stability of the dielectric and evolution of the transfer curves of dielectric annealed at 830 °C (a) device structure PBZ/IZO TFT.

3.4 Conclusion

In summary, the $(Pb_{0.8}Ba_{0.2})ZrO_3$ thin film has been fabricated by the sol-gel route and successively used as a gate dielectric for the first time via solution-processed IZO TFT. The device displayed a low operating voltage (5 V), which can be used in low-power electronic devices. This sol-gel-derived film was annealed at 800˚C to achieve the crystalline phase of $(Pb_{0.8}Ba_{0.2})ZrO_3$. To conclude the optical and electrical properties

of this material, a thin film of $(Pb_{0.8}Ba_{0.2})ZrO_3$ has been fabricated on quartz and p+ -Si substrate at 800˚C. These measurements ensure us that the film is highly transparent in the visible region due to less scattering at the interface, and it shows high electrical insulating nature indicating $(Pb_{0.8}Ba_{0.2})ZrO_3$ as a suitable gate dielectric for TFT application. To realize the applicability of this dielectric thin film, solution-processed IZO TFT was fabricated by using $(Pb_{0.8}Ba_{0.2})ZrO_3$ dielectric. It is observed that the TFT requires only 5 V or less to operate the device as expected from a high capacitance dielectric. The device showed high effective electron mobility of 4.5 cm^2 v^{-1} s^{-1} and on/off ratio of 5×10^3. Therefore, this ferroelectric material-based TFT can be used in some microelectronic applications for portable electronics in the future.