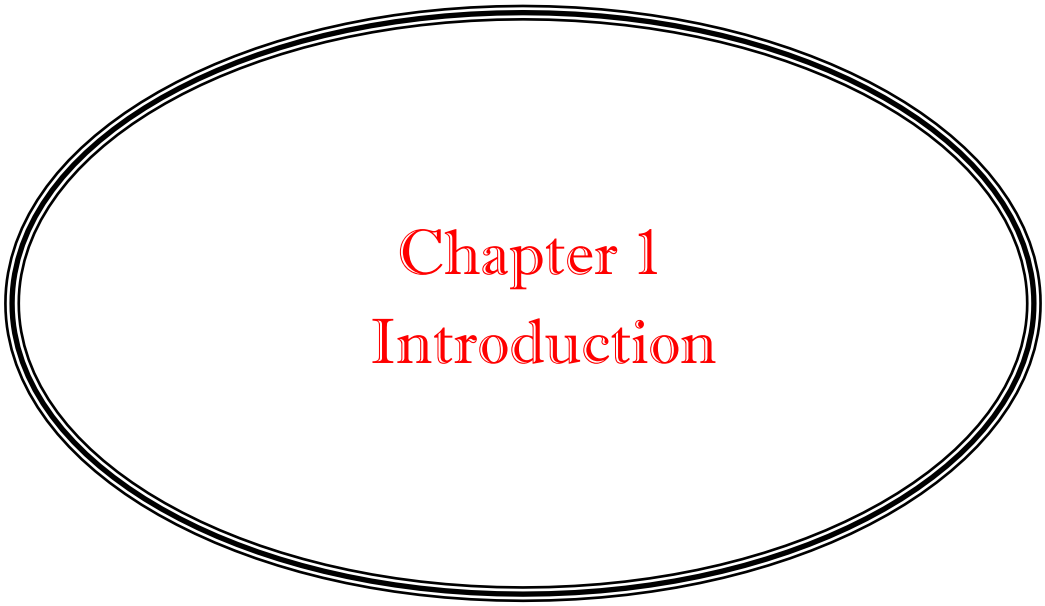


Chapter 1
Introduction

Chapter-1

1.1 Introduction

Oxide materials have a wide range of applications and give sufficient opportunities for scientists to investigate several fascinating phenomena that occur in oxide systems and interfaces. Because of the increased surface-to-volume ratio, the Nanoscale form of oxides adds a new level of previously discovered phenomena to the already wide spectrum of characteristics. Transparent electronics, optoelectronics, magneto electronics, photonics, spintronics, thermoelectric, piezoelectric, power harvesting, hydrogen storage, and environmental waste management are just a few of the uses for oxide electronic materials. However, it's still quite difficult to synthesize electronics-grade oxide materials that can fill the gap that requires for commercial application. Besides, the fabrication of metal oxide thin films, as well as converting them into specialized device architectures for certain applications required more systematic research. [1] Among different oxide electronic devices, thin-film transistor (TFT) is one key component that is used for different applications like invisible electronics, display technology, flexible electronics, sensor, etc. For TFT fabrication, it is required conducting electrodes, a semiconducting channel, and an insulating gate dielectric. All of these three components can be fabricated from different metal oxides. For the commercial application of metal oxide-based TFT, it requires development in all of these three areas.

In my Ph.D. thesis work, the goal is to develop a cost-effective sol-gel method to make a metal oxide-based dielectric for use in low operating voltage thin-film transistors (TFT). Particularly I have focused on developing low-voltage metal oxide semiconductor (inorganic) transistors utilizing sol-gel derived perovskite gate dielectrics. Because of the high dielectric constant (k) feature of perovskite materials, it’s possible to

fabricate low operating voltage TFT by using these materials which have been predicted in the number of literature in past. However, so far very limited publications have been reported on perovskite oxide-based metal oxide TFT which are fabricated by different physical vapor deposition (PVD) methods. In contrast, in my Ph.D. work, I have focused on a solution-based method for different perovskite metal oxide TFT fabrication. Besides, I've covered important TFT components, and various device architectures and studied TFT operating principles.

1.2 Different application areas of low operating voltage TFT

The area of metal oxides is approaching an exciting stage where major commercial applications are developing. However, the problems are in the deposition and processing of the materials, and the success of this technology is dependent on how effectively these obstacles are overcome.[1]Different applications of metal oxide TFT are summarized in **figure 1.1**.[1]A transistor is made up of three terminals: gate, source, and drain. An insulator known as a gate dielectric separates the source and drain electrodes from the gate. The drain current of a transistor is regulated by the gate electrode and travels through an active channel semiconductor layer between the source and drain electrodes. TFT performance is heavily influenced by the gate dielectric, active channel layer, and fabrication process. Thin-film transistors may be made using a variety of processes, including vacuum-based methods such as sputtering, molecular beam epitaxy (MBE), chemical, and atomic vapor depositions. Although vacuum-based techniques can deposit high-quality thin films, they are costly to implement. Furthermore, those vacuum-based deposition techniques' are insufficient for large-area electronics applications. Vacuum-based fabrication costs cannot be reduced to meet demand due to a combination of these two issues. The cost issue is not only limited to the advanced equipment used in the fabrication, but also to the cost of materials utilized

for the device. It's critical to find new, affordable, and plentiful materials for device fabrication in order to lower total fabrication costs. In the case of metal oxide semiconductor-based TFTs, for example, indium-based compounds are the most well-established active materials for TFT production, although there are clearly cheaper and more efficient alternatives. To minimize manufacturing costs, a non-vacuum-based solution-processed method must be developed. The development of that solution processing method for low operating voltage metal oxide TFT is the subject of this thesis study.

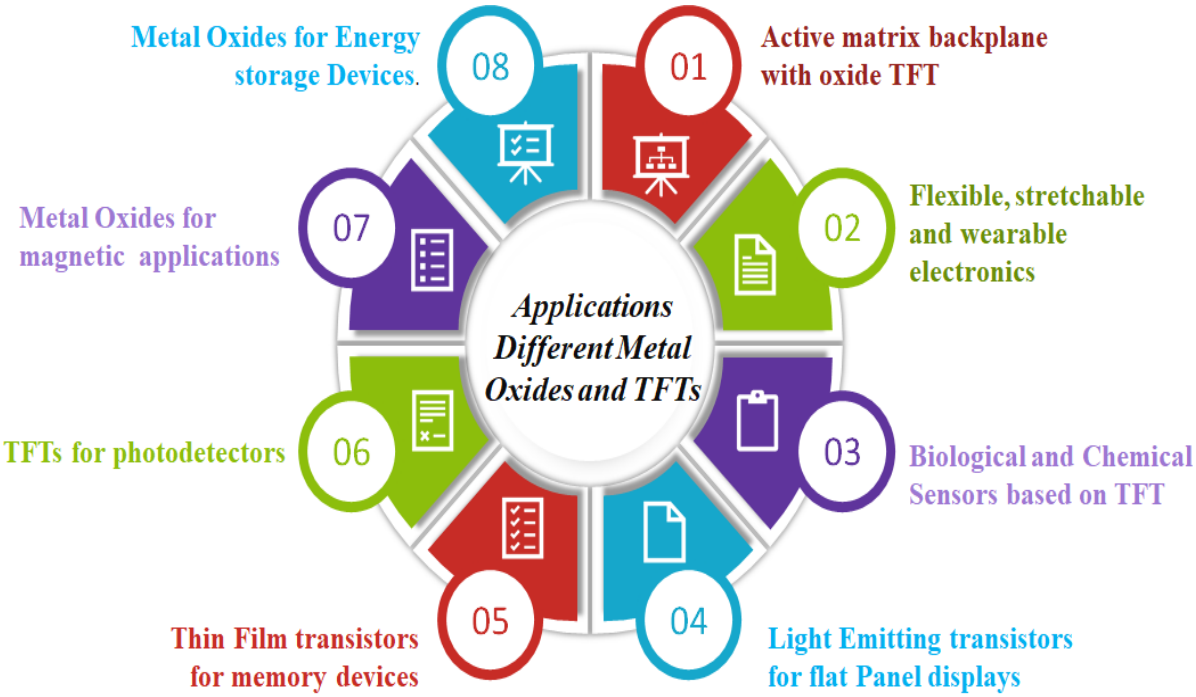


Figure 1.1: Depiction of Low voltage TFT utilization in various technologies by a circular info graph.[1]

1.3 Important components of TFT

TFTs are three-terminal field-effect devices similar to metal oxide semiconductor field-effect transistors (MOSFETs) and are frequently utilized in the display sector due to their simple architecture. TFTs, which are the fundamental components of these circuits, control the pixels in flat panel displays such as liquid crystal displays (LCD) and modern active-matrix organic light-emitting diodes (AMOLED). The performance of TFTs used in display circuits influences the development of HD advanced displays and the quality of these displays. In the display sector, n-type oxide and p-type organic TFTs have previously been adopted, and they have outperformed p-type oxide and n-type organic TFTs.[2, 3] The development of high-performance p-type oxide and n-type organic TFTs is required for the deployment of a complementary metal-oxide-semiconductor (CMOS) device that is compatible with low-power electronic applications in the future.

Transistors have been a single dominant characteristic in the microelectronics industry as a building block for logical circuits since their invention, and this has had an inventive impact on every area of human existence. Although J. E. Lilienfeld is often credited with inventing the first field-effect transistor, and the concept was patented in 1934[4-6], Paul K. Weimer at the Radio Corporation of America (RCA) laboratory reported the first functional TFT in 1960.[7] In the late 1960s, RCA reported the creation of the first TFT-based LCD (liquid crystal display).[7]Thin film transistors have three layers **[figure 1.2 a]** the semiconductor channel layer, the insulating dielectric layer, and metal electrodes. The source, drain, and gate electrodes regulate the source-drain current via the semiconductor channel layer, while the voltage supplied to the gate electrode controls the current through the semiconductor channel layer that acts

as an active channel in which charge carriers accumulate as shown in **figure 1.2 b**. The dielectric layer separates the gate electrode from the source-drain electrode, and the metal oxide semiconductor (MOS) structure functions like a capacitor.

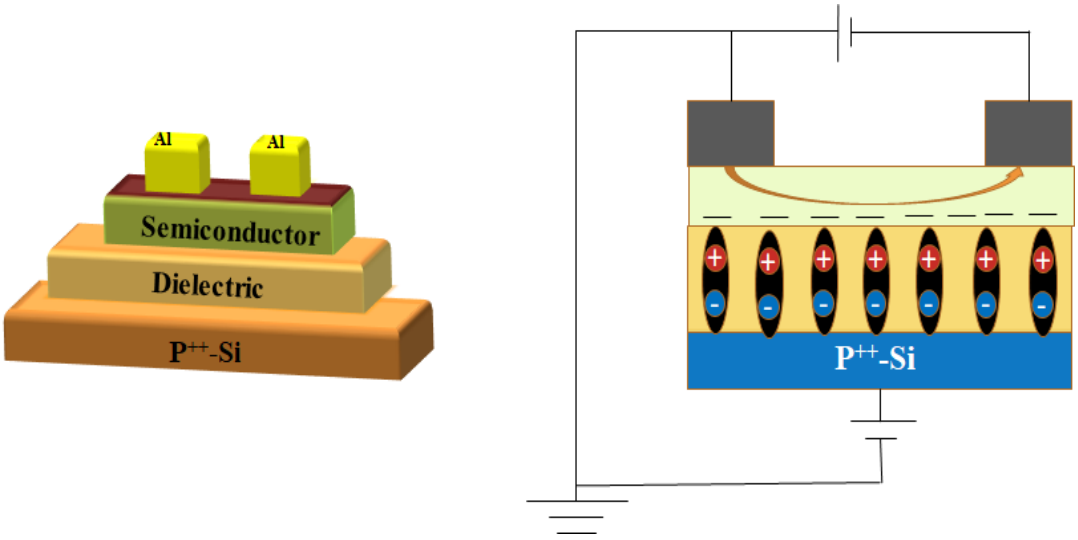


Figure 1.2: A schematic depiction of a) a TFT with a bottom gate and top contact configuration, and b) charge transportation in a TFT channel under an electric field.

1.4 Different device architectures of TFT

TFTs are categorized as coplanar (C) or staggered (S) depending on how the three electrodes are arranged (**figure 1.3**). In a coplanar arrangement, the source and drain electrodes, as well as the gate insulator, are all located on the same side of the channel. The source, drain, and insulator electrodes are on opposing sides of the channel in a staggered arrangement. TFTs are further divided into two categories based on the gate electrode's location., with top gate and bottom gate TFTs, respectively.[8]When the channel layer must be deposited with a high-quality crystal structure, the top-gate (TG) structure might be employed. The fabrication of highly oriented channel layers is possible because of highly orientated pre-deposited substrates like Si. When the

semiconductor channel layer requires high-temperature annealing operations, the TG structure is recommended, as this process may harm other layers in the bottom-gate (BG) structure. Because of the ease of production, the BG structure is the most widely utilized TFT structure. Before depositing the active semiconductor channel layer on top of it, the gate electrode and insulator were prepared first.[9] The majority of the researchers employed commercially available gate/insulator substrates, such as ITO and Si/SiO_2 substrates. The researchers can conveniently optimize the channel characteristics by depositing a channel layer on top of a well-defined gate/insulator substrate under different deposition conditions rather than altering the device structure, which is one of the advantages of this BG construction. Another benefit of this architecture is that the channel layer may need to be annealed at a certain temperature in a specific ambient gas, such as N_2 or air, in some instances. Because the channel layer is exposed to the environment, this structure makes it simple to do. The BG configuration also has a benefit when considering TFT display applications since the bottom gate electrode blocks the backlight. We used the BG/TC shape (**figure 1.3 c**) in this thesis because it delivers excellent performance and low contact resistance due to its larger effective area, which allows for easy charge injection into the active layer (**figure 1.2 b).**

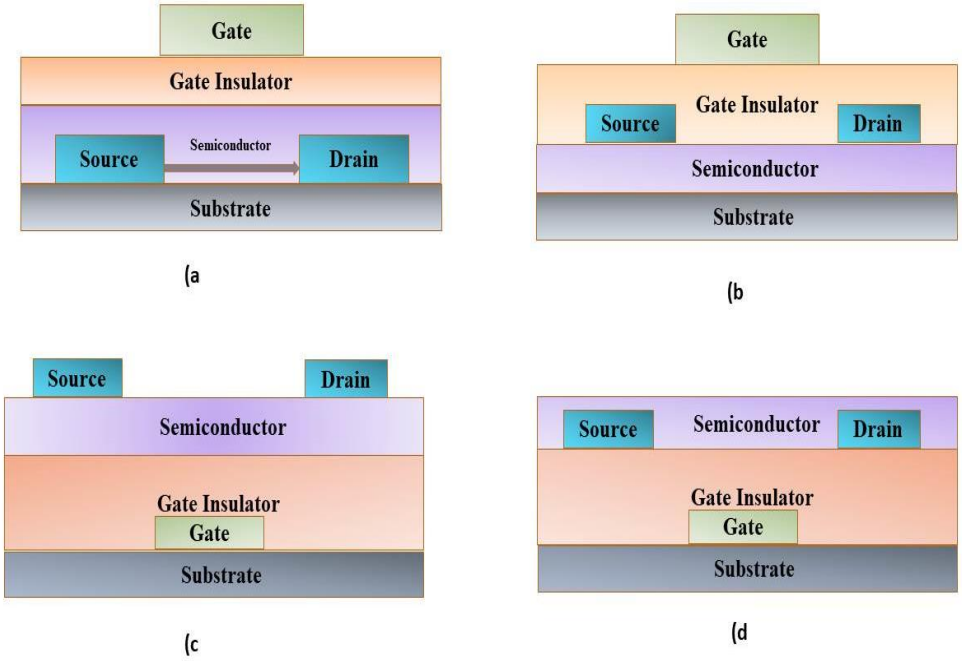


Figure 1.3: TFT Layouts: (a) Top-gate bottom-contact and (b) Top-gate top-contact (c) Bottom-gate top-contact; and (d) Bottom-gate bottom-contact.[10]

1.5 Working principle of TFT

In a TFT, gate voltage controls the conduction of charge carriers between the source and drain electrodes through a semiconductor channel layer. The parallel plate capacitor structure (MOS structure) made up of metal, semiconductor, and oxide dielectric provides for simple regulation of electron (hole) flow across the channel layer. The buildup of charge carriers near the semiconductor/insulator interface is done by modulating channel conductance with the applied gate voltage. Depending on whether the channel layer is n-type or p-type, electrons or holes will accumulate.[11]Because these two devices have similar features and functions, there has always been some confusion about the distinction between MOSFET and TFT. To form a conducting channel layer, appropriate gate voltages are used to produce an inversion layer of charges for MOSFETs and an accumulation layer of charges for TFTs.

The gate voltage and capacitance of an insulator are proportional to the accumulated charge carrier density. The drain voltage controls the drain current (I_D) in the active layer between the drain and source electrodes (V_D). A uniform density of charge carriers forms in the channel if V_D is very smaller than drain voltage (V_G). However, this charge accumulation changes to non-uniform nature with increasing drain voltage, and conducting channel near the drain electrode become narrower. During this period I_D increases linearly with drain voltage. However, when V_D becomes almost equal to (V_G-V_T), conducting channel becomes very narrow and its width can't lower with further increases in drain voltage which is commonly known as a pinch-off condition of TFT. Above pinch-off voltage, I_D doesn't vary much with V_D and becomes saturated, which is known as the saturation region of drain current.

1.6 TFT characterization and Extraction of important parameters

There are two different types of transistor characteristics, commonly known as output (I_D vs V_D) and transfer characteristics (I_D vs V_G). TFT's output and transfer characteristics are comparable to MOSFET's. From these data, all TFT parameters may be calculated. In most cases, the transfer characteristics are used to determine the TFT's overall performance. Because the drain current may be controlled by two separate voltages, drain voltage (V_D) and gate voltage (V_G), the current-voltage properties of a TFT are often represented in two ways. The output characteristics of a TFT are the change of I_D with V_D for constant V_G. The quality of TFT can be identified from the distinction of the linear and saturation regions of output characteristics, as well as the progressive improvement of I_D with V_G. The variation of I_D with V_G for constant V_D is referred to as the transfer characteristics of a TFT, and it provides all of the device's

important parameters, such as mobility, on/off ratio, subthreshold swing, and threshold voltage. **Figures 1.4 a and 1.4 b, c** show typical output and transfer curves for n-channel transistors respectively.

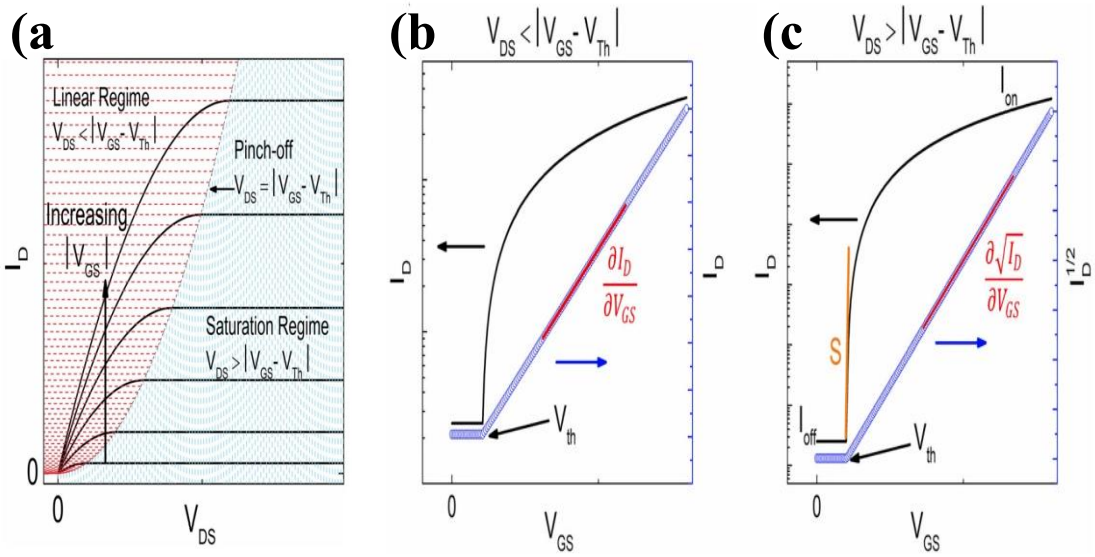


Figure1.4: a) output and b), c) transfer characteristics of an n-type oxide TFT.[12]

In the output characteristics, there are two types of operation regions: linear and saturation. The TFT operates like a resistor in the linear zone of operation, where the current flowing through the conductive channel is linearly dependent on the V_D. The application of V_G creates a conductive channel in the semiconductor, and the collected charges are spread evenly throughout the channel area.[13] With rising V_{DS}, a modest current between the source and drain electrode start flowing linearly. This area of operation occurs when $V_D \leq V_G - V_T$, where V_T is the threshold voltage. The current-voltage relationships in a TFT may be obtained using the gradual channel approximation ohmic current and determined analytically using equation (1), which leads to the linear region.[12, 13]

$$I_{D,Lin} = \frac{W}{L}\mu_{Lin}C_i(V_G - V_T - \frac{V_D}{2})V_D \quad \text{..... (1)}$$

Where $I_{D,Lin}$ is the drain current in the linear region, μ_{Lin} is the linear field-effect mobility, C_i is the capacitance per unit area of the gate dielectric, W and L are the width and length of the channel layer, and V_G,V_D,V_T are the gate voltage, drain voltage, and threshold voltage respectively.

The second operating zone of a TFT is the saturation region, which occurs when the drain voltage exceeds the gate voltage, i.e. $V_D \geq V_G - V_T$. The voltage drop across the gate dielectric at the drain electrode increases when the V_D is increased, thus reducing the field across the dielectric. As a result, the accumulation layer at the drain electrode gets thinner, resulting in a limited conductive channel. As a result, the current flowing between the drain and source electrodes is decreased, and the current flow is independent of V_G voltages. The pinch-off condition is defined as the depletion of charge carriers at the drain electrode, following which a steady current flows through the channel layer. The following relationship can be used to describe this kind of TFT operation.

$$I_{D,Sat} = \frac{W}{2L}\mu_{Sat}C_i(V_G - V_T)^2 \quad \text{..... (2)}$$

Where $I_{D,sat}$ is the drain current in the saturation region, and μ_{sat} is the saturation field-effect mobility.

In TFTs, there are two distinct modes of operation: depletion mode and enhancement mode. Even at 0 gate voltage, a tiny drain current runs across the channel layer in depletion mode. i.e., with a depletion mode TFT, the channel layer has a larger carrier concentration, therefore even at V_G=0 V, there is a conductive channel. TFTs with this mode of operation is employed in sensing applications. However, with V_G=0V, minimal drain current flows in enhancement mode TFTs, and this TFT is referred to as a

normally-off device. TFTs with a lower carrier concentration channel layer assist to realize these capabilities, and such TFTs are commonly utilized in standard display units and circuits.

1.6.1 Mobility of TFT Device

The carrier mobility of a TFT is one key parameter that indicates the charge transport efficiency in the semiconductor channel layer. For practical TFT applications, the mobility value should be as high as possible and it is dependent on multiple factors such as carrier scattering, the crystallinity of materials, band structure of semiconductor materials, contact potential of semiconductors, etc. Scattering of charge carrier is originated from surface roughness of gate dielectric, semiconductor/dielectric interface, and other defects of semiconductor channel. Depending on the V_D values, two types of mobility values may be retrieved from the transfer characteristics: linear field-effect mobility (lin: for small V_D) and saturation field-effect mobility (sat: for larger V_{DS}). The saturation mobility of a TFT is the most essential parameter in terms of application, and it is widely described in the literature.[9]Equations (3) and (4) make it simple to compute mobilities in linear and saturation regions. The following equation is used to extract mobility under any gate bias in the linear region:

$$\mu_{Lin} = \frac{L}{WC_iV_D}\left(\frac{\partial I_{D,Lin}}{\partial V_G}\right) \quad \text{.....(3)}$$

Similarly, the following equation is used to determine mobility under any gate bias in the saturation region:

$$\mu_{Sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{D,Sat}}}{\partial V_G}\right)^2 \quad \text{.....(4)}$$

1.6.2 on/off ratio of TFT device

The ratio of the maximum drain current to the minimum drain current is known as $I_{on/off}$, and it can be calculated using the transfer characteristics that can be seen in **figure 1.4**. The minimum current, also known as the off current, is determined by the sheath resistance of the semiconductor channel, the noise level of test equipment as well as leakage current through the TFT's dielectric. When using TFTs in circuits, the off current should be kept to a minimum to achieve low power dissipation.[14] In fact, the Ion/off ratio value represents the ideality of TFT switching properties. On/off, ratios for TFTs typically vary between 10^3 and 10^8.

1.6.3 Subthreshold Swing of TFT device

The required V_G to increase the I_D by one decade is known as the sub-threshold swing (SS) of a TFT that determines the switching speed of a TFT, or how quickly a transistor switches from an "off" to an "on" state. Smaller SS values (usually 0.1 to 0.5 V/decade) are always preferred since they reflect a faster transition from off to on state[15]. SS value of TFT can be determined by transfer curve using the following equation[14]:

$$\mathbf{SS} = \left[\frac{\mathbf{d(\log I_D)}}{\mathbf{dV_G}}\right]^{-1} \quad \text{.....(5)}$$

As it is proportional to interface trap density (N_{ss}^{max}) stated in the equation given below, subthreshold swing also indicates the superiority of the interface between dielectric and semiconductor.

$$\mathbf{N_{SS}^{max}} = \left[\frac{\mathbf{SS} \times \log \mathbf{e}}{\mathbf{kT/q}} - \mathbf{1}\right]\frac{\mathbf{C}}{\mathbf{q}} \quad \text{.....(6)}$$

Here SS is subthreshold swing, K is Boltzmann constant, T is absolute temperature, C is the capacitance of dielectric, and q is the elementary charge.

The lower the value of (N_{ss}^{max}) is always expected for a good quality TFT as trap less number of the carrier in the channel. Therefore, a lower value of N_{ss}^{max} implies better dielectric/semiconductor interfaces. The interface trap density is dependent on the dielectric layer's SS and capacitance, as shown in equation (6), expressed above. Carrier accumulation at the interface is proportional to the insulator's capacitance, implying that the higher the capacitance, the greater the accumulation.

1.6.4 Threshold voltage of TFT device

The threshold voltage is the lowest gate voltage that requires turning on the channel conduction. It can be determined from the transfer characteristics of the TFT is in enhancement or depletion mode based on the threshold voltage readings.[16] The enhancement mode TFT has positive V_T for the n-type channel layer, whereas the depletion mode TFT has negative V_T. By extrapolating the linear section of the $I_D^{1/2}$ vs V_G plot, V_T can be determined from the x-intercept.

1.7 High-k dielectric for low operating voltage TFT

The dielectric layer is one of the most important components in TFT that regulate the channel conduction of a TFT. A thinner dielectric layer is often desired to lower the working voltage of a TFT. However, if it is too thin, then it may develop pinholes which can introduce a larger gate leakage current. Besides, the tunneling action from thinner gate dielectric may intensify, resulting in increased leakage current through the layer. However, a higher-k dielectric material allows a greater number of charge accumulations in the channel with the same dielectric layer thickness and gate bias.

Therefore, using a high-k material, it is possible to use a thicker gate dielectric for that can reduces gate leakage current.

It has been observed that the lower band gap materials have a relatively higher dielectric constant. Therefore, higher dielectric constant materials may introduce more tunneling current (**figure 1.5 b)**. An ideal gate dielectric should have a larger band gap and higher k-value which is shown in the shaded area of **figure 1.5 a.**

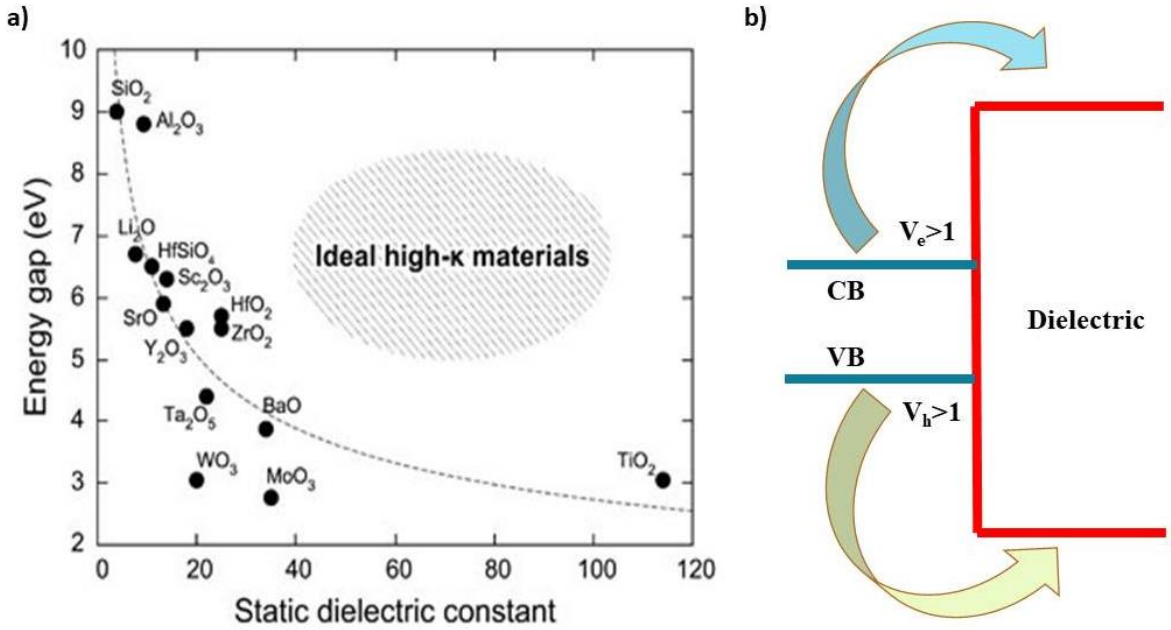


Figure 1.5: a) The dielectric constant and band gap of well-known oxides as measured experimentally. Also depicted is the optimal property area for dielectrics.[17] b) schematic diagram of band offset determining carrier injection in oxide band offset.

Several insulating materials have been characterized as gate dielectrics by sophisticated processing techniques for the development of microelectronics during the last decade, and are often employed for generating low operating voltage TFTs. These novel dielectrics can

be classified into a few groups such as; a) self-assembled monolayer (SAM)[18-20] b) self-assembled multilayer Nano dielectrics (SANDs) [21-23], c) high-k metal oxide dielectrics [24-28] d) dielectrics with nanostructured and Nano composite structures[29-32]e) ion-gel dielectrics[32-35] f) dielectrics made of polymer electrolytes ion-conducting oxide dielectrics[36-38], and g) ion-conducting oxide dielectrics.[39-42]SAM is a unique class of dielectric that is commonly employed for producing low operating voltage organic TFTs among the dielectrics mentioned above. It is also possible to produce mechanically flexible TFTs, in addition to the low operating voltage. SANDs are another preferred dielectric for the manufacture of organic and flexible organic TFTs, similar to SAM. Ion-gel dielectric has become more commonly employed in the manufacturing of organic TFTs, and its performance is even greater than that of SAM and SAND dielectrics. All three types of dielectrics, however, are not suitable for high-temperature annealed metal-oxide TFT manufacturing. High-k oxide dielectrics and ion-conduction metal oxide dielectrics are the finest choices for sol-gel metal oxide TFT manufacturing. A vast range of new dielectrics (HfO_2, Al_2O_3, ZrO_2, TiO_2, Y_2O_3, and Ta_2O_5, among others) have been reported as an alternative for the classic SiO_2 insulating layer (k = 3.9) in the field of metal oxide dielectrics, and most of them can be deposited by using a solution processing technique.[43-47] Electronically, these dielectric materials are exceptionally insulating and have a wide bandgap, in addition to having great ionic conductivity. This class of materials is a novel gate dielectric for low voltage TFT manufacturing due to the combination of these unique features. The dielectric constant in an inorganic dielectric usually fluctuates inversely to the bandgap, as seen in **figure 1.7 a).** The band offset of the dielectric materials concerning silicon should be more than 1 eV for gate dielectric applications, as shown in **figure 1.7 b)**. The selection of a high-k dielectric must meet a few further criteria as discussed below. [48]

1.8 Selection paradigm of High-k Dielectric

In addition to the scaling issue, when a dielectric material is used in a TFT structure, other aspects must be taken into accounts, such as low defect density, minimum interfacial trap sites, low fringing capacitance effect, and band engineering capability. Aside from the high-k, gate insulators for TFTs should have additional characteristics, such as a smooth surface, low leakage current, and a high breakdown field. [50, 49] In addition to these factors, kinetic stability, cost (depending on synthesis complexity), and material toxicity should also be considered when selecting an insulator.

1. **High permittivity:** The high dielectric constant is a major determining factor. High-k provides a thicker film with a higher capacitance density, reducing the device's leakage current.
2. **Thermodynamic stability:** The thermodynamic stability of dielectric is the second requirement. Because the metal oxide dielectric comes into direct contact with the active channel, it must not react with it.
3. **Kinetic stability:** It needs to be kinetically stable and suitable with semiconductor processing temperatures of up to 1000˚C.
4. **Band offsets:** To reduce charge injection into the semiconductor's bands, high-k insulators must operate as a gate dielectric with band offsets of greater than 1 eV with respect to the semiconductor.
5. **Interface quality**: Because dielectric materials come into close touch with channel semiconductors, they create a superior electrical interface. TFT is a dielectric-sandwich device with the gate electrode and semiconductor layer. As a result, the interface between the dielectric and the gate electrode (Si substrate) must be stable

and pure for a semiconductor to grow on the dielectric. To achieve a low trap density of the structure, it must form an excellent electric interaction with the material in the channel.

6. **Defects:** To ensure good device performance, the dielectric thin film's surface must have a very low defect density. An ideal dielectric should have a smooth surface to prevent undesired carrier scattering, which limits the device's effective mobility.

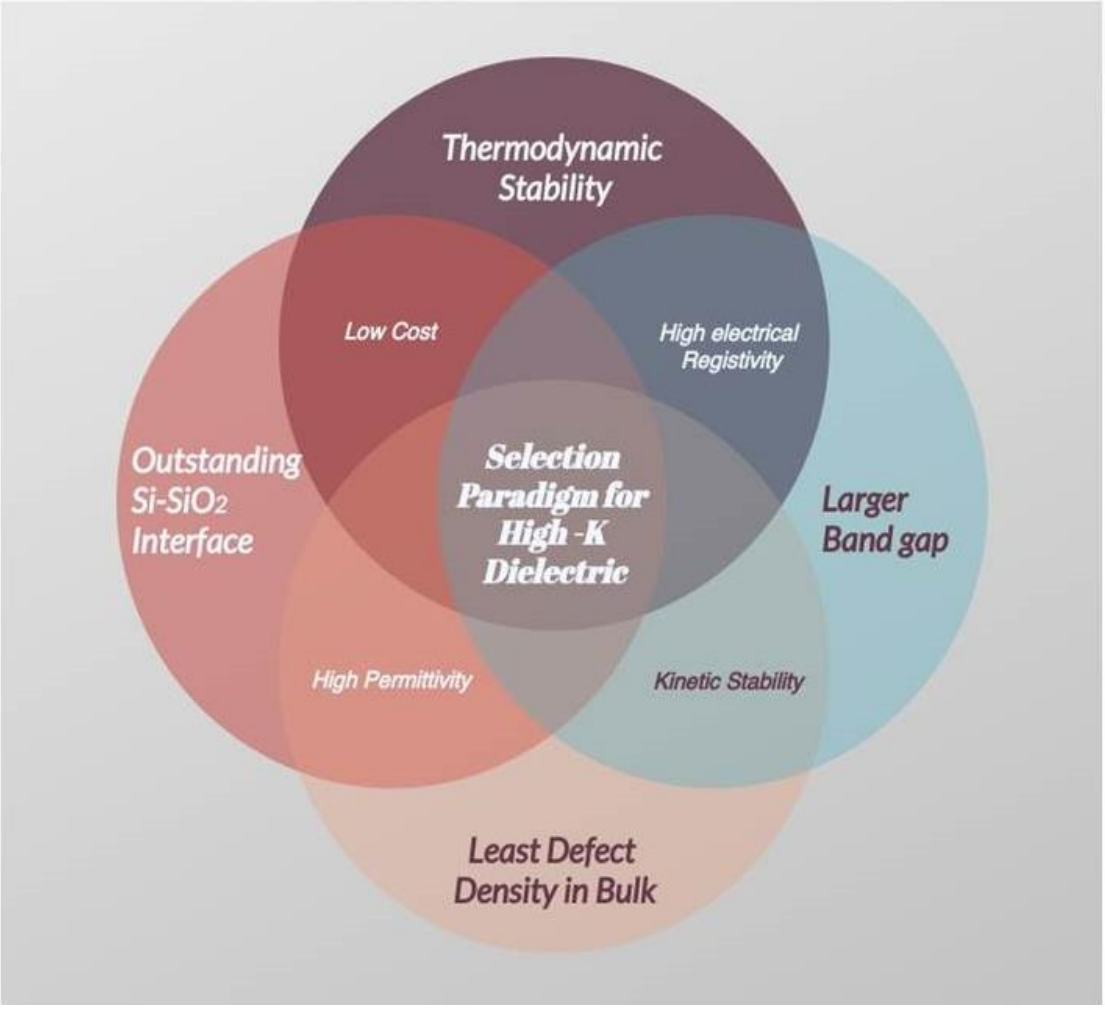


Figure 1.6: Selection paradigm of High-k Dielectric for TFTs.

1.9 Oxide Perovskite as gate dielectric for Thin Film Transistors-

Perovskite materials, particularly oxide and hybrid forms, have received a lot of interest in recent decades. Oxide perovskite materials have been studied as semiconductor and insulator layers for a long time, but hybrid perovskite materials, which combine the properties of inorganic and organic equivalents in a molecular-scale composite, have just lately come to light. In the latter situation, inorganic frameworks of metal halide octahedra are linked by strong covalent or ionic bonds, which ensure great charge carrier mobility and thermal stability. Their organic portions enable the fabrication of hybrid perovskite materials using a simple, low-cost, low-temperature technique while also inducing elastic characteristics in the material. Hybrid perovskites have been employed in a variety of applications due to their unusual physical features, including light-emitting diodes, solar cells, and photodetectors.[49]

Since the 1960s, SiO_2 has been used as a gate dielectric for complementary metal-oxide-semiconductor transistors.[50, 51] However, quantum mechanical processes in the semi-conductor industry limit microelectronic devices when reaching a tiny dimension, putting a stop sign in front of Moore's law. [51-56] Electrons can tunnel straight through gate insulators in metal-oxide-semiconductor field-effect transistors when SiO_2 thickness is <20 Å (only a few atomic layers), resulting in abnormally large gate leakage current (MOSFETs).[50, 53-56]As a result, device scaling necessitates the substitution of SiO_2 with oxides with high dielectric constants, which inhibit tunneling currents while preserving the electrical characteristics of an ultrathin SiO_2 sheet. The contact between these insulators and Si must be atomically specified, with no interfacial SiO_2 layer between Si and the insulator layer, to provide excellent FET performance.[50, 51]As dielectric insulators, multiple oxide perovskites (ABO_3) with

high dielectric constants have been reported, such as $SrTiO_3$ (STO)[57, 58] $CaHfO_3$,[59], $LaInO_3$,[60] $LaFeO_3$, [61] and $LaAlO_3$,.[62] It was reported that AO and ABO_3 molecules may grow epitaxially on Si.[50, 63-65]

Therefore, oxide perovskite materials, such as $SrTiO_3$ [57, 58]$CaHfO_3$, [59]$SrHfO_3$, [66]$LaInO_3$, [60], $LaFeO_3$,[61], and $LaAlO_3$,[62] can be employed as insulator layers in place of SiO_2 because of their higher dielectric constant than SiO_2, (the most widely used gate insulator).[51, 52] As a result, FET device sizes can be reduced even further.[51, 53, 55]

$SrTiO_3$ is the most commonly investigated dielectric gate material in FETs.[50, 53, 55, 57, 58, 67-71] due to multiple reason. At ambient temperature, STO has a relative dielectric constant of 300, increasing to several thousand at low temperatures, when the dielectric constant also becomes electric field dependent. In contrast, SiO_2 has a relative dielectric constant of 3.9.[72] For Si-based FETs, epitaxially grown STO was employed as the dielectric layer. [50, 53, 55]The formation of crystalline STO on single-crystal Si is difficult due to the formation of an undesired amorphous SiO_2 layer on the Si surface when exposed to oxygen, which restricts STO oxide heteroepitaxy on Si. In our work, we have successfully developed the crystalline STO by the sol-gel route and employed it in a thin film transistor as a gate electrode. The dielectric constant of oxide perovskite materials used as the dielectric layer in FET devices and the properties of these perovskite materials are listed in **table 1.1.** FeFET devices have received a lot of attention because they can be used to create nonvolatile active memory components. The essential principle is that electric polarisation in the ferroelectric layer induces depletion and buildup of carriers in the conductive layer; moreover, these states are

preserved due to the ferroelectric layer's remnant polarisation. [73] The number of charges induced by Ferro-electricity in the semiconductor is equal to the spontaneous polarisation of the ferroelectric layer. As a result, to produce a significant response, the number of carriers in the semiconductor should not be greater than the number of charges that the ferroelectric layer may generate.[74]

Table 1.1. The dielectric constant of these perovskite materials and the properties of FET devices employing oxide perovskite materials as the dielectric layer.[75]

Dielectric	**Semiconductor**	**Source and drain**	**Dielectric constant**	**μ_e [$cm^2V^{-1}s^{-1}$]**	**μ_h [$cm^2V^{-1}s^{-1}$]**	**I_{on}/I_{off}**	**V_T[V]**
$SrTiO_3$	Si		175	221	62		
$SrTiO_3$ (100)	Nb-STO(100)	Pt	270				
Mn-doped $Ba_{0.6}Sr_{0.4}TiO_3$			28				
Mg-doped $Ba_{0.6}Sr_{0.4}TiO_3$	ZnO	Al	22	16.3		$6.4x10^4$	2.8
$CaHfO_3$	Single crystal STO(100)	Al	12	04-0.5		10^5	6.8
$SrHfO_3$	Si(100)		19				
$LaInO_3$	La-doped $BaSnO_3$	4% La-doped $BaSnO_3$	38.7	90		10^7	
$CH_3NH_3PbI_3$	$InGaZnO_4$	Ti/Au/Ti	1000	12		10^5	0.69

Due to its application potential in several devices, such as a ferroelectric field-effect transistor (FeFET), perovskite ferroelectrics (e.g., $Pb(Zr_xTi_{1-x})O_3$] have sparked intense research. However, due to the diffusion of Pb and Ti into silicon and the creation of an intermediary silicate layer at the interface, the ferroelectric perovskite is not very compatible with a typical Si channel. As a result, a perovskite semiconducting channel has been used to create an all-perovskite FET structure. Watanabe et al.[75]presented an all perovskite FeFET with a gate insulator of (Pb, La)(Zr, Ti)O_3 and a semiconducting layer of $La_{1.99}Sr_{0.01}CuO_4$. The device was written and erased at a 7 V working voltage with a 1 s pulse width, resulting in a resistance modulation of about 10% and memory retention of >10 days at room temperature. Meanwhile, the usage of doped rare-earth

manganates as a semiconductor material in all perovskite FeFETs has been encouraged. This might be attributed to a variety of factors. First, doped rare-earth manganates (e.g., $La_{1-x}Ca_xMnO_3$) are often associated with high magneto resistive properties, and second, these materials are closely related to other ferroelectric perovskites in terms of lattice matching, permitting FeFET manufacturing.[74] The high magneto resistance is most likely due to spatial inhomogeneity caused by multiphase coexistence, which causes physical attributes to be perturbed externally.[57]

1.10 Metal oxide semiconductor

Metal oxide semiconductors have emerged as a significant contender for future electronic device development in recent years. They have high carrier mobility and transparency. Therefore, they're great for the latest portable electronic devices. Many research groups and industrialists around the world are enthusiastic about this material class, and some electrical products based on these new efficient metal oxide semiconductors have already hit the market. Since the first report on the development of high mobility amorphous oxide semiconductor InGaZnO (IGZO) TFTs in 2004, substantial research on these materials for the development of big area high definition flat panel displays has been conducted.[76] Many flat panel display (FDP) companies, including Samsung, LG, and Sharp, have previously created large-area active-matrix OLED displays based on IGZO.[2, 3, 77]Oxide TFTs have now been made using oxides of different metals, including In, Ga, Zn, and Sn, as well as alloy combinations. The most commonly used n-type channel materials for the construction of amorphous oxide semiconductor-based TFTs include indium gallium zinc oxide (InGaZnO), zinc indium oxide (ZnInO), zinc tin oxide (ZnSnO), zinc indium tin oxide (ZnInSnO), and others.[78-81] Because of

their cost-effectiveness, indium-free systems are highly sought. As a result, among the materials described above, zinc tin oxide (ZTO) is more advantageous and cost-effective for producing high-performance TFTs. All of the above-mentioned TFTs are based on n-type oxide materials, and producing p-type oxide TFTs with equivalent performance to n-type TFTs is difficult.

From a thin film transistors point of view, semiconductors can be categorized into two parts-1) inorganic semiconductors and 2) organic Semiconductors. Our work is focused on inorganic semiconductors, so we basically discuss about inorganic semiconductors in detail.

1.10.1 n-type oxide semiconductors

Metal oxide-based Semiconductors used for thin-film transistor application can be categorized into two parts-

1) **Binary oxide 2) multi-component oxide**. In addition to the wide band gap, these materials are optically transparent as well, in the visible region, which makes these a suitable candidate for transparent TFTs.

The first TFT was described in 1964, and it was made by evaporating SnO_2 as the channel layer on a bottom gate glass substrate.[82]the early TFT had poor performance because of the lack of saturation and a high off current. Even though the device could not be turned off, it was a significant achievement. thereafter, the first TFT based on ZnO as a channel was developed in 1968.[83]They also suffered from the same problems like lack of saturation and other poor device parameters. Metal oxide semiconductors are now being utilized in new display units, demonstrating their potential as future transparent flexible electronics alternatives.

i. Binary metal oxide semiconductors for TFT application

ZnO, SnO_2, and In_2O_3 are the most investigated binary oxide semiconductors for TFT applications.[84] Because of their inherent high conducting nature (10^{-2} S cm^{-1} to 10^3 S cm^{-1}) due to the presence of shallow imperfections inside the materials and high transparency owing to the wide bandgap, these transparent conducting oxides were greatly researched in the past. The electronic configuration of the heavy post-transition metal cations in these materials is $(n-1)d^{10}ns^0$ ($n\geq4$). Even though there is structural randomness, the spherical symmetry of s orbitals causes overlapping of nearby s orbitals. Even in the amorphous forms of metal oxide semiconductors, electron conduction is possible. The above three materials are still considered the foundation materials for amorphous oxide semiconductors for these reasons. The current research and development in oxide materials as TFT channel layers focuses on fine-tuning the deposition conditions to control the electrical conductivity of these oxides. Since the initial fabrication of fully transparent ZnO TFT by Hoffman et al. in 2003[85], the transparent TFT has grown via constant advancements in material and process technology. They used ion beam sputtering to create the TFT, which has saturation mobility of 2.5 cm^2V^{-1} s^{-1}, a high $I_{on/off}$ ratio of 10^7, and a 75 percent optical transmission. The increased performance was owing to the enhancement in Crystallinity of the ZnO channel layer, which was annealed at 800°C in an oxygen ambiance. The fundamental obstacle to the development of flexible electronics was the high-temperature processing of ZnO, and much research was devoted to lowering the processing temperature. Carcia et al.[86] were the first to build a ZnO TFT at ambient temperature in 2003. With field-effect mobility of >2 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 10^6, they achieved superior performance in TFT. Later, at a lower processing temperature, a successful demonstration of transparent ZnO TFT employing radio

frequency (RF) magnetron sputtering was reported. Fortunato et al. produced a high-performance ZnO TFT with high mobility at room temperature in 2004 [87]. thereafter many researchers have reported the progressive work on ZnO-based TFT with improved device performance. ZnO TFT manufacturing at room temperature is still undergoing active study to improve the characteristics for use in transparent flexible electronics.

Three years after the creation of the first ZnO TFT, another key binary oxide contender, indium oxide (In_2O_3), joined the field of TFT. Because of its large carrier concentrations ($>10^{19}$ cm^{-3}), In_2O_3 is typically utilized as a transparent conducting oxide. During the radio-frequency plasma accelerated reactive thermal evaporation of In_2O_3, Lavareda et al. examined the optimization of carrier concentration by changing the RF power and oxygen content.[88] They discovered that TFTs with field-effect mobility of 0.02 cm^2V^{-1} s^{-1} and an $I_{on/off}$ ratio of 10^4 performed reasonably well.

Presley et al. constructed the first enhancement-mode SnO_2 TFT in 2004 using RF magnetron sputtering and fast thermal annealing in O_2 at 600°C.[89] With channel layer thicknesses ranging from 10 to 20 nm, the devices were very transparent and performed well, with field-effect mobility of 2 cm^2V^{-1} s^{-1}. Another promising metal oxide contender, TiO_2-based TFT, was reported by Katayama et al.[90] in 2006, with field-effect mobility of 0.08 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 10^4. The goal of this report was to create a TiO_2 TFT with atomic-scale surface control for use in electrical and magnetic devices. Park et al. announced better TiOx active-channel TFTs produced by low-temperature plasma-enhanced atomic layer deposition (PEALD) in 2009, with 1.64 $cm^2V^{-1}s^{-1}$ field-effect mobility.[91]

The performance of thin-film transistors (TFTs) made using n-type binary oxide channel layers is summarized in the following table.

Table 1.2: Characteristics of TFT produced with n-type binary oxide channel layers.[9]

Binary oxide materials	**Technique**	**Mobility ($cm^2V^{-1}s^{-1}$)**	**I_{on}/I_{off}**	**year**	**Reference**
ZnO	Sputtering	>2	10^6	2003	[86]
ZnO	PLZ	1	10^5	2003	[92]
ZnO	Ion beam sputtering	2.5	10^7	2003	[85]
ZnO	Sputtering	27	$3x10^5$	2004	[87]
ZnO	ALD	21.3	10^7	2014	[93]
ZnO	PEALD	12	3.4×10^9	2018	[94]
InO_x	RF-PERTE	0.02	10^4	2006	[95]
In_2O_3	Ion-assisted deposition	120	10^5	2006	[96]
In_2O_3	Thermal Evaporation	34	10^4	2008	[97]
SnO_2	Sputtering	2	10^5	2004	[89]
TiO_2	PLD	0.08	10^4	2006	[90]
TiO_2	PEALD	1.64	10^5	2009	[91]
TiO_2	Sputtering	0.69	10^7	2011	[98]

ALD = Atomic layer deposition, PEALD = Plasma enhanced atomic layer deposition, PLD = Pulsed laser deposition, RF-PERTE = radio frequency plasma enhanced reactive thermal evaporation

ii. Multicomponent oxide semiconductors for TFT application

Transparent conducting oxides are well-suited for use in transparent electronics due to their inherent electronic structure. Due to the spherical symmetry of unoccupied s orbitals, they have strong conductivity even in their amorphous phase. Even though the materials are in a disordered form in the amorphous phase, electronic conduction occurs due to the overlap of s orbitals of nearby cations. The amorphous nature of semiconductor thin films is favored over crystalline films for use as TFT channel layers because the former may be easily formed at lower temperatures with good uniformity. The primary disadvantages of crystalline materials for the manufacture of transparent flexible TFTs are non-uniformity and high processing temperatures.

Mixing various semiconductors with different crystal structures is the simplest technique to create an amorphous state in semiconductors. Because of their unique electrical configurations, combining ZnO, SnO_2, and In_2O_3 has been widely used for the creation of amorphous oxide semiconductors. The performance of TFTs manufactured with multicomponent amorphous materials channel layers is summarized in **table 1.3.** Indium zinc oxide (IZO) and zinc tin oxide (ZTO) are the most prevalent and well-established multicomponent amorphous materials.[99-101]

ZnO and In_2O_3 are mixed to make indium zinc oxide. This compound has emerged as one of the most essential materials for use as transparent electrodes in flat panel display manufacture. IZO films outperform other indium-based amorphous semiconductors due to their high mobility (>20 $cm^2V^{-1}s^{-1}$) and uniformity. Despite the fact that IZO had great qualities, the researchers were looking for alternate materials to replace the pricey

indium in the channel layer of IZO TFTs. IZO thin films typically have a high electron concentration (>10^{17}), which makes lowering the concentration by changing the deposition conditions more difficult. Maintaining a minimum off current for the TFT is critical, and for this, the carrier concentration in the channel layer should be between 10^{13} and $10^{17}cm^{-3}$.[102, 103]

Table 1.3: Characteristics of TFT produced with n-type multicomponent oxide channel layers.[9]

Multicomponent oxide materials	**Technique**	**Mobility ($cm^2V^{-1}s^{-1}$)**	**I_{on}/I_{off}**	**year**	**Reference**
InZnO	Sputtering	20	10^8	2006	[104]
InGaZnO	PLD	9	10^3	2004	[76]
InGaZnO	Sputtering	12	10^8	2006	[105]
InGaZnO	Sputtering	35.9	$4.9x10^6$	2007	[106]
HfInZnO	Sputtering	10	10^8	2009	[107]
ZrInZnO	Sputtering	3.9	10^7	2009	[108]
AlSnInZnO	Sputtering	31.4	$2x10^9$	2010	[109]
SiInZnO	Sputtering	21.6	10^7	2010	[110]
SnInZnO	Sputtering	24.6	10^9	2009	[109]
SnInZnO	Sputtering	12.4	10^8	2008	[111]
ZnON	ALD	6.7	$9.4x10^7$	2007	[112]
ZnSnO	Sputtering	14	10^6	2005	[113]
ZnSnO	Sputtering	50	10^7	2005	[99]
GaZnSnO	Sputtering	24.6	10^6	2005	[113]

ZrZnSnO	Sputtering	8.9	$7.5x10^{8}$	2011	[114]
STO	Sputtering	5.9×10^{-2}	10^{5}	2016	[115]
PBZ	Sol-gel	4.5	5×10^{3}	2019	[116]
Li-Al_2O_3	Sol-gel	17	3.3×10^{4}	2020	[117]
Li_2ZnO_2	Sol-gel	23	6×10^{3}	2018	[118]
$LiAlO_2$	Sol-gel	25	3×10^{5}	2019	[119]
LITO	Sol-gel	5.6	10^{4}	2022	[120]

Nomura et al. achieved a reduction in carrier concentration by using an excellent doping process at room temperature in 2004 [76]. They lowered the carrier concentration (10^{17}) of IZO thin films with high mobility of 10 $cm^2V^{-1}s^{-1}$ by doping Ga into the IZO (IGZO) host matrix. Ga^{3+} has a high ionic potential, which helps to reduce carrier concentration by suppressing oxygen vacancies by strongly binding oxygen ions. IGZO is the most researched amorphous oxide semiconductor for TFT applications, and it has lately been adopted in smartphone display units. After seeing how well IGZO performed, researchers worked hard to develop new multicomponent amorphous oxide semiconductors by doping other metals (Hf, Zr, Mg, La, Sc, and Si) into the IZO host matrix.[76, 107, 121-123]

1.11 Solution-processed thin-film transistors-

Initially, vacuum-based technologies (e.g., sputtering and chemical vapor deposition) were used to fabricate oxide high films, which required extended processing durations in high vacuum settings for effective film deposition. Film densification sometime required post-deposition treatment at a reasonably high temperature. These approaches are not suitable for material deposition onto flexible substrates with vast areas and high

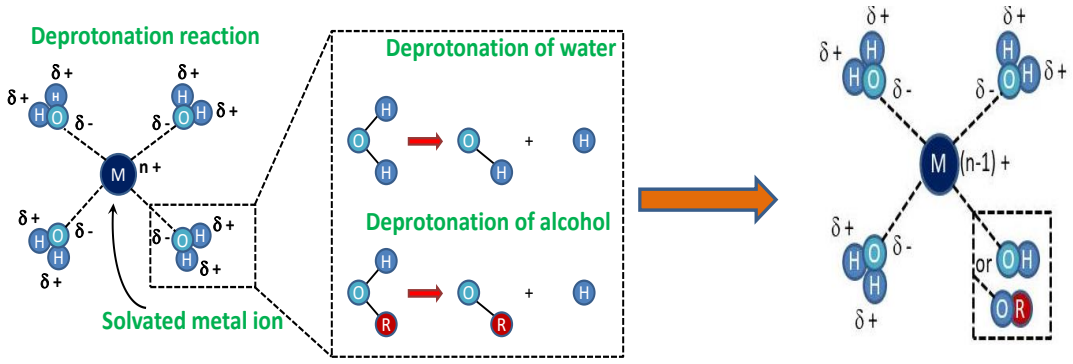
scalability due to these disadvantages. Using solution-based processing, the rapid development of film deposition methods has lately relieved this bottleneck. As a result, both academic and industrial researchers are focusing on low-cost, high-throughput solution-based deposition. By removing vacuum deposition processes and substituting them with printable precursor materials, solution-based fabrication reduces production costs significantly. By using solution techniques, such as spin/dip/spray/bar coating, drop-casting, and other printing procedures, high throughput oxide films may be made in a variety of ways. Therefore, developing solution-based deposition techniques, such as the sol-gel method, for low-cost mass manufacturing is essential. In **table 1.4**, the benefits of sol-gel processed oxide are outlined. Operational ease, pre-cursor preparation, position precision, throughput efficiency, and roll to roll (R2R) compatibility are all pros and disadvantages of each process and are compared in the following table-[11, 124-126]

Table 1.4: Comparison of printing and coating processes for film deposition[127]

Technique	**Spin**	**Spray**	**Bar**	**Ink-jet**	**Screen**	**Gravure**
Preparation of Ink	Easy	Average	Easy	Average	Demanding	Difficult
wastage of Ink	Remarkable	Considerable	Very less	X	X	Remarkable
Speed of the technique	–	Fast	Medium	Medium	Fast	Very fast
Non-contact process ability	✓	✓	X	✓		X
R2R compatible	X	✓	✓	✓	✓	✓

Metal alkoxides (M-(OR)z) and metal salts, such as chloride, acetates, sulfides, and nitrates, are dissolved in alcohol or aqueous solvent in a standard sol-gel technique. Metal alkoxides and alcohol derivatives are popular solution processing precursors due to a variety of advantages, including good solubility in organic solvents and a higher

likelihood to create metal oxides due to well-suited chemical reactivity, as well as an easy purification procedure.[128]Regardless, because metal alkoxides are chemically more reactive, they are often more expensive and more difficult to manage, resulting in a shorter shelf life. Therefore, metal acetates are also commonly utilized for different solution-processed depositions. In this material synthesis route, the metal cations lose a proton owing to the hydrolysis process after being treated with the solvent (e.g., H_2O or ROH) molecules, resulting in metal hydroxides as shown in **figure 1.7** depicts the formation of an M-O-M polymeric framework followed by a condensation process involving metal hydroxides via oxidation. The sol-gel approach produces three various types of products depending on the reaction temperature, duration, pH, and catalysts, such as sol, gel, and nanoparticles, as illustrated in **figure 1.8**. The precursor solution is coated, followed by post-annealing treatment, which (1) completes the condensation process by forming a MOM structure, (2) eliminates residues and impurities of secondary products and organic solvents via thermal decomposition, and (3) produces a dense oxide film by reducing unwanted voids in the film (densification process).[129, 130]By lowering defect states in solution-processed metal oxide dielectrics, it is possible to produce films with reduced surface roughness. These elements are critical in ensuring that the appropriate electrical insulation maintains its high-k value. In this technical context, solution-processed metal oxides are new materials that are being studied extensively for use as a multipurpose device building block, such as low voltage TFTs, in materials research and technology. Low operating voltage oxide TFTs, in particular, have sparked considerable attention as a potential material for active matrix light emitting diodes (AMLEDs), flat panel displays (FPDs), and optoelectronic applications such as light emitting transistors and phototransistors.[130-133]



(b) Hydrolysis reaction

(c) Condensation reaction

- $M^{n+} + X^- + ROH \text{ or } H_2O \equiv M\text{-}OH + ROH$
- $\equiv M\text{-}OR + H_2O$

$\equiv M\text{-}OH + HO\text{-}M \equiv M\text{-}O\text{-}M + H_2O$

$\equiv M\text{-}OH + RO\text{-}M \equiv M\text{-}O\text{-}M + ROH$

Figure 1.7: Steps in the chemical reaction of sol-gel a) A diagram depicting the deprotonation process between metal ions and solvent (H_2O or alcohol) molecules, which results in metal hydroxides. Examples of b) hydrolysis and c) condensation processes.[133]

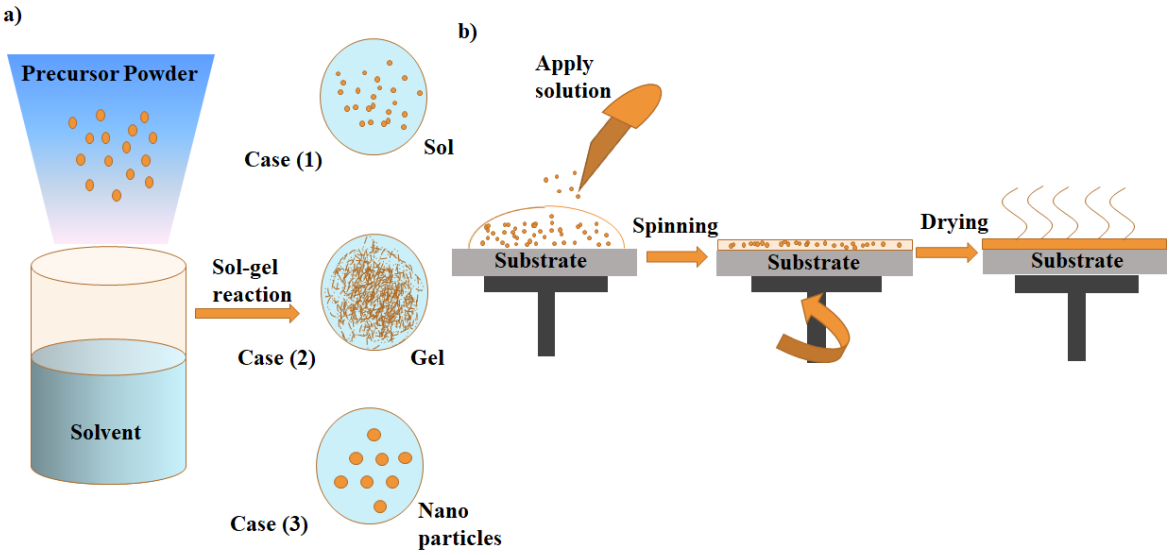


Figure 1.8: Solution-processed metal oxide thin film deposition schematic a) a depiction for densification of sol-gel thin films utilizing high-temperature annealing b) several types of end products such as sol, gel, and nanoparticles.

Furthermore, operating at low voltage makes portable electronics such as mobile phones, electronic tablets, laptops, and other low-power devices much more feasible. Many research groups worked hard to build low voltage metal oxide TFTs using the sol-gel method. Most binary oxide-based TFTs, such as HfO_2, TiO_2, Al_2O_3, and ZrO_2, have been reported for the enhancement of low voltage metal oxide TFTs, as stated in the dielectric section.[127, 134-143]**Table 1.5** summarizes the various solution-processed oxide gate dielectrics that have been employed as TFT gate dielectrics.[144, 145]

Table 1.5: Performance of binary oxide dielectric-based TFTs with Sol-gel Coating [127, 133]

Dielectric	Temperature[^oC]	d [nm]	C_i[nF cm^{-2}]	k	E_b[M V cm^{-1}]	Channel	μ_{FE} [cm^2 $V^{-1}S^{-1}$]	I_{on}/I_{off}
ZrO_2	350	139	138.2	21.7	-	IGZO	0.6	≈10^5
ZrO_2	500	70	-	22	-	MoS_2	50.1	≈10^3
ZrO_2	250	13.3	484	7.3	-	In_2O_3	10.78	≈10^6
ZrO_2	400	11	710	8.8	-	IZTO	14	≈10^7
ZrO_2	≈ 50	-	800	13	-	In_2O_3	1.65	≈10^5
ZrO_2	400	22	860	17.3	≈6	SnO	2.5	3x10^3
ZrO_x	300	40	450	23	-	IZTO	14.9	≈10^6
HfO_x	400	120	-	13	5.5	IGZO	13.1	≈10^7
HfO_x	300	65	190	≈14	-	ZTO	1.05	≈10^5
HfO_2	150	100	145	14.1	4.4	ZnO	1.17	≈10^6
HfO_x	500	17.1	650	12.4	9.2	IZO	36.9	10^9
HfO_x	350	25	435	12.7	≈7.5	ZTO	13.2	≈10^8
HfO_x	150	24	330	10	≈3.6	IGZO	43.9	10^6
YO_x	400	188	73.4	15.6	-	ZnO	45.5	≈10^6
YO_x	350	17	448	16.5	-	In_2O_3	15.98	6x10^6

YO_x	400	22.7	345.7	8.85	≈3.5	IZO	20.93	$2x10^5$
Gd_2O_3	500	100	146	14	-	IZTO	1.9	$6x10^3$
Sc_2O_3	350	23	460	12.1	≈9	IZO	27.7	$3x10^7$
GaOx	250	52	172	10.1	>2.5	In_2O_3	4.1	$≈10^5$
LiO_2	300	13	465	6.7	≈4.5	In_2O_3	5.69	$≈10^7$
MgO	500	16.2	330	7.5	-	In_2O_3	5.48	10^7
Yb_2O_3	600	14.9	508	8.6	-	In_2O_3	5.61	10^7
SrO	500	28.3	352.8	11.3	-	In_2O_3	4.98	10^6

Table 1.6: The summary of TFT parameters for spin-coated multicomponent or multilayered oxide dielectrics.[18]

Dielectric	Temperature[^oC]	d [nm]	C_i[nF cm^{-2}]	k	E_b[MV cm^{-1}]	Channel	μ_{FE} [cm^2 $V^{-1}S^{-1}$]	I_{on}/I_{off}
$HfSO_x$: La	325	192	-	9-12	4-6	IZO	1	$≈10^7$
AIPO (2:1)	800	155	-	4.8	≈5	ZnO	3.5	$≈10^6$
AlNaO (11:1)	600	75	2000	170	5.3	ZTO	28	$≈10^4$
YHfZnO	600	235	61.7	16.4	2.68	IGZO	0.29	$≈10^5$
AIPO (2:1)	300	180	-	5.2	≈6	IGZO	4.5	≈10
TaSrO (2:1)	700	100	-	36	-	IZO	0.24	5 x 10^6
ZrO_2:B	250	100	-	12.1	≈4	In_2O_3	39.3	$≈10^7$
AlZrO (9:1)	350	95	110	11.8	-	IZO	≈53	$≈10^6$
HfLaO (1:1)	500	60	178	22	=5	ZnO	1.6	10^6
AlZrO (2:1)	400	133	131	19.7	-	IHZO	18.1	10^7
MgTiO (3:2)	500	180	≈85	17.2	-	IZO	3.41	$6x10^6$
LaAlO (1:1)	600	100	≈100	11.5	>4	IGZO	11.1	$≈10^6$
AlZrO (19:1)	150	≈35	≈180	≈7.3	>7	IGZO	7.71	$2x10^9$
HfSiO (2:1)	500	105	91	10.8	2.9	ZTO	153	$3x10^7$
AlZrO (2:1)	500	60	123	8.3	-	ZTO	37	$≈10^6$
AlLaO (4:1)	200	92	128	9	>4	In_2O_3	≈5	$≈10^6$
AlYO (1:3)	400	37	443	19.5	≈5	IZO	52.9	$≈10^6$
HFO_x/AIO_x	400	85	≈150	-	-	ZTO	3.84	$≈10^5$
ZrO_x/AlO_x	180	≈35	≈235	≈9	-	ZnO	11	$≈10^4$
TiO_x/AlPO	350	150	-	8	>3.5	IGZO	3.2	$≈10^5$
ZrO/AlO/ZrO	350	250	45.8	14.8	≈3.4	IZO	3.27	$≈10^7$
LaTaO/BiNbO	550	190	-	90	-	IGZO	0.49	$≈10^7$

$LaZrO_x/SiO_2$	180	188	25	-	-	IZO	24.8	$4x10^7$
$ZrO_2/Al2O$,	150	39	279	12.3	8	ZnO	1.37	$4x10^6$
AIO/ZrO/AIO	350	61	95.6	-	2.42	IZO	4.51	5×10^5
$Al2O_2/ZrO_2$	≈150	49	115	8.53	-	IGZO	12.85	$≈10^8$

Materials with adequate high as well as wide E_g are required for low voltage and high-performance TFTs. High and large E_g were combined in the same gate dielectric using multi-component and multilayered inorganic dielectrics (**table 1.6**).[146-152]This inorganic dielectric offers a good dielectric-to-semiconductor contact, which is critical for TFT manufacturing at low voltage while retaining high performance.

Pal et al. introduce a new approach to fabricating low voltage metal oxide TFT by utilizing sodium beta-alumina (SBA) solid electrolyte thin film as gate dielectric through a cost-effective solution processing approach. The architectures of SBA, which is ion (Li^+, Na^+, and K^+) inserted into alumina dielectrics, are shown in **figures 1.9** a) and b). Because of ionic mobility and low leakage current, this 75-nm thick SBA insulator layer has a high areal capacitance of 2 μF/cm^2.[42] The deposited dielectric thin film had a rather high E_b of 5.3 MV cm^{-1} and a very high k value of 170.

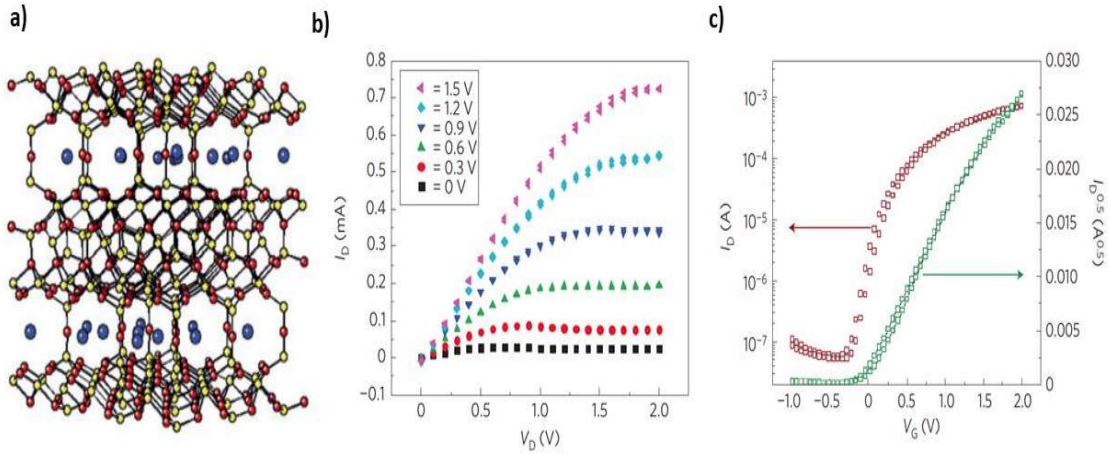


Figure 1.9: Ion-conducting metal oxide thin film transistor with solution processing a) A blue dot depicts the crystal structure of the SBA dielectric ion, while red and yellow colors represent oxygen and aluminum atoms, respectively. b) Output and c) Transfer Characteristics of ZTO Transistor with Sol-gel Coated SBA Dielectric Based TFT[42]

This high capacitance was attributed to a significant increase in polarisation achieved by displacement of an alkali ion in an electric field while maintaining a low leakage current due to a lack of electron transportation inside the dielectric material. **Figure 1.13** c and d show the output and transfer characteristics. SBA is an excellent alternative gate dielectric for low voltage TFTs with high mobility and a modest On/Off ratio, based on these features.[42, 127] Ion conducting SBA and related dielectrics provide the best performance among the several types of gate dielectrics for metal oxide TFT applications. This type of dielectric may be formed using a low-cost solution processing approach such as spin or dip coating followed by annealing.[41] The sodium beta-alumina (SBA) class of materials, on the other hand, demands a relatively high annealing temperature (830^{o}C), restricting substrate material accessibility. To address this problem, other ion-conducting dielectrics with lower crystallization temperatures like Li_5AlO_4,[153] $LiAlO_2$,[119], and Li_2ZnO_2[118] were investigated. All of the reported TFTs show operating voltage within 2.0 V with high carrier mobility and a high on/off ratio.

1.12 Scope and objective of present work-

Transparent metal oxide thin films have been used in a variety of applications like photodetectors, biosensors arrays, active matrix light-emitting diodes (AMLEDs), and light-emitting transistors because of their outstanding optical, electrical, and physical properties, including high transparency, excellent charge carrier mobility, adjustable energy band structure, good mechanical flexibility and durability, and excellent environmental and chemical stability. One of the most promising transistor technologies for future large-area flexible electronics is solution-processed metal oxide thin-film transistors (TFTs). Our work examines current developments in solution-processed metal oxide TFTs, such as n-type oxide semiconductors, oxide dielectrics, perovskite

oxide dielectrics, and ion-conducting dielectrics. Traditionally SiO_2 has been utilized as a gate dielectric for complementary metal-oxide-semiconductor transistors since the 1960s. However, quantum mechanical processes in the semiconductor industry limit microelectronic devices when they approach a Nanoscale level, putting Moore's law to a standstill. When the thickness of SiO_2 is 20 Å (just a few atomic layers), electrons can directly tunnel through gate insulators in metal-oxide-semiconductor field-effect transistors, resulting in unusually significant gate leakage current (MOSFETs). However, most of these TFTs require high operating voltages (40V) because of the low dielectric constant (k) of standard SiO_2 gate dielectric, restricting their usefulness to portable low power devices. As a result, device scaling involves the use of oxides with a high dielectric constant in place of SiO_2.

To resolve this critical issue, one primary goal of this thesis is to use a cost-effective sol-gel technique to deposit perovskite oxide and ion-conducting thin film for the application as a gate dielectric of a low operating voltage TFT. Furthermore, by combining this dielectric with a bilayer device structure, device performance may be enhanced, including improved subthreshold swing, fewer interface states, a higher on/off ratio, and, most importantly, a lower operating voltage. Overall, the thesis covers the creation of oxide perovskite and ion-conducting materials as a gate dielectric for high-performance, low-voltage TFTs using a cost-effective sol-gel approach. As a result of the aforementioned discussion in this chapter, the thesis is separated into main objectives that comprise these chapters.

The cost-effective solution process approach has been discussed in **Chapter 2** to synthesize dielectric and semiconductor materials. A spin coater is used to coat a thin film of dielectric and semiconductor that is utilized as a gate dielectric in a TFTs. This chapter further clarifies the materials and device characterization techniques.

In **Chapter 3**, it has been described how to develop PBZ dielectric using a solution-processing approach and how to use it as a gate dielectric in a metal-oxide TFT. Bottom-gate top-contact TFTs have employed solution-processed indium zinc oxide (IZO) as a channel semiconductor. For this device fabrication, a PBZ thin film is deposited on top of a heavily p-doped Si wafer (p^{++}-Si). This TFT requires a 5 V operating voltage to saturate the drain current, which is particularly advantageous for low-power electronics due to its lower operating voltage than a traditional SiO_2 gate dielectric device. With an on/off ratio of 5×10^3 and a subthreshold swing of 0.35 V/decade, this typical TFT has an exceptional electron mobility of 4.5 $cm^2V^{-1}s^{-1}$.

In Chapter 4, We have Discussed about a perovskite gate dielectric, $SrTiO_3$, which has been created and effectively employed for TFT production using a low-cost solution processing technique. The crystalline phase of $SrTiO_3$ was achieved by annealing this sol-gel-generated film at 750˚C. Thin films of $SrTiO_3$ were produced on quartz and p^{++}-Si substrates at 750˚C to assure the material's optical and electrical characteristics. Because of the low scattering at the interface, the film is extremely transparent in the visible area and has a high electrical insulating nature, indicating $SrTiO_3$ as a suitable gate dielectric for TFT applications. A solution-processed SnO_2 TFT was used to demonstrate the application of this dielectric thin film. The TFT only requires 2 V or less to run the device. The TFT has an electron mobility of 0.23 $cm^2V^{-1}s^{-1}$. Furthermore, the device has a high on/off ratio (10^4) and a low subthreshold swing (290 mV dec^{-1}).

In Chapter 5, We have Discussed that how, a perovskite gate dielectric, $BaTiO_3$, was developed and successfully used for TFT manufacturing. By annealing, this sol-gel produced film at 850˚C, and the crystalline phase of $BaTiO_3$ was attained. To ensure the material's optical and electrical properties, thin films of $BaTiO_3$ were grown at 850˚C on quartz and p^{++}-Si substrates. The film is exceptionally transparent in the visible area

and has a high electrical insulating nature due to the minimal scattering at the interface, indicating $BaTiO_3$ as a viable gate dielectric for TFT applications. The implementation of this dielectric thin film was shown using a solution-processed SnO_2 TFT. To operate the TFT, it simply needs 10 V or less. The electron mobility of the TFT is 0.028 $cm^2V^{-1}s^{-1}$. The gadget also features an on/off ratio of 25, as well as a low subthreshold swing (2.2 V dec^{-1}).

In **Chapter 6,** the high-performance solution-processed metal oxide thin-film transistor (TFT) fabrication technique has been discussed by utilizing Li_2SnO_3 gate dielectric. Like the earlier device, these metal oxide TFTs were also fabricated on heavily p-doped silicon (p^{++} -Si) substrate using a sol-gel technique. Besides, an n-type TiO_2 thin film is used as an electron donor to the semiconductor/dielectric interface to enhance the device's performance. Because of this additional TiO_2 layer, the overall leakage current has been reduced essentially enhancing the on/off ratio of the device. An optimized device with this Li_2SnO_3 dielectric and a TiO_2 gate interface shows electron mobility of 3.47 $cm^2V^{-1}s^{-1}$, an on/off ratio of 50, and a low leakage current of density 3.8 x 10^{-5} A/cm^2 under 5volt external bias, which can be suitable for using this film as a gate dielectric of a thin film transistor (TFT).