PREFACE

Thin film transistors (TFTs) are building blocks in nearly all varieties of electronics and professional display products, ranging from smartphones to big diagonal flat-panel TVs. Till now, a wider range of TFTs is manufactured from Si-based materials, such as crystalline silicon, polycrystalline silicon, amorphous silicon, silicon dioxide, silicon nitride, etc. On the other hand, non-silicon-based TFT can be fabricated from various semiconductors like metal oxide semiconductors, organic semiconductors, and different nanostructure materials which are gaining popularity due to their versatile features. Besides those non-conventional semiconducting materials development, a significant effort is given to developing high dielectric constant (high-k) material for gate dielectric application to overcome the limitation of the low dielectric constant of conventional SiO_2 gate insulators. Because of the low dielectric constant (k) of typical SiO_2 gate dielectric, most of those TFTs require high operating voltages (≥40V), restricting their use to portable low power devices. To meet the requirement for high-performance portable electronics (e.g., laptops, tablets, smartphones, and so on), fundamental electronics components like thin-film transistors (TFTs) need to drive at low operating voltage with low power consumption which requires the development of reliable high-k materials. Again for high yield production with lower cost, a solution-processed technique is preferable. Till now, several solution-processed high-k materials are developed for the application of gate dielectric of a TFT such as metal oxide, ion-conducting metal oxide, perovskite oxide, ion-gel, high-k organic polymer, organic-inorganic hybrid materials, etc. Among them, perovskite oxide materials not only have a high dielectric constant, but they may have good ferroelectric or ferromagnetic behavior that can make them more versatile for different technological applications. Instead, till now there are very limited publications on solution-processed perovskite oxide-based gate dielectric for the application of low operating voltage TFT. Therefore, a reliable technique is required for the development of solution-processed perovskite oxide thin film fabrication, and an in-depth study is necessary to explore the possibility to apply those materials for TFT fabrication.

In our thesis work, I have developed three different perovskite dielectrics ($Pb_{0.8}Ba_{0.2}ZrO_3$, $SrTiO_3$, $BaTiO_3$) through the sol-gel route and used them as a gate dielectric for metal oxide TFT fabrication. Apart from these perovskite dielectrics, an ion-conducting dielectric has also been developed through the sol-gel technique and used as that ion-conducting dielectric of a TFT. The operating voltages of these TFTs are highly reduced (<5V) in both cases due to the high dielectric constant of these perovskite oxide and ion-conducting oxide gate dielectric. Besides the low operating voltage of these TFTs, the overall performance of TFTs was reasonably good concerning earlier literature on solution-processed low operating voltage TFTs. The key findings of my thesis works that I presented in different chapters are mentioned briefly in the following sections.

In **Chapter 3**, it has been described how to develop PBZ dielectric using a solution-processing approach and how to use it as a gate dielectric in a metal-oxide TFT. Bottom-gate top-contact TFTs have employed solution-processed indium zinc oxide (IZO) as a channel semiconductor. For this device fabrication, a PBZ thin film is deposited on top of a heavily p-doped Si wafer (p^{++}-Si). This TFT requires a 5 V operating voltage to saturate the drain current, which is particularly advantageous for low-power electronics due to its lower operating voltage than a traditional SiO_2 gate dielectric device. With an on/off ratio of 5×10^3 and a subthreshold swing of 0.35 V/decade, this typical TFT has an exceptional electron mobility of 4.5 $cm^2V^{-1}s^{-1}$.

In Chapter 4, I have discussed about a $SrTiO_3$ perovskite gate dielectric, which has been synthesized and successfully employed for TFT fabrication using a low-cost solution processing technique. The crystalline phase of $SrTiO_3$ was achieved by annealing this sol-gel-generated film at 750˚C. A quartz substrate was used to study the optical property of $SrTiO_3$ thin film that indicates high transparency (>90%) of this film in the visible range, indicating the low scattering from the dielectric surface. Electrical conductivity and frequency-dependent capacitance were studied by using a MIM deice of device structure p++Si/$SrTiO_3$/Al. This study reveals that the $SrTiO_3$ thin film is quite insulating in nature and has a reasonably good breakdown voltage. Besides, it has a very high areal capacitance (~730 nF/cm^2) which is almost constant up to 10 kHz. A solution-processed SnO_2 TFT was fabricated by using this $SrTiO_3$ thin film to demonstrate its application as a gate dielectric of a TFT. This study shows that the TFT requires < 2 V volt external bias to run the device. The optimum TFT has an electron mobility of 0.23 $cm^2V^{-1}s^{-1}$ with on/off ratio $>10^4$ and subthreshold swing of 290 mV dec^{-1}.

In Chapter 5, I have explored the possibility of the use of sol-gel derived perovskite $BaTiO_3$ thin film as a gate dielectric of SnO_2 TFT in a similar way that has been discussed in chapter-5. In this case, $BaTiO_3$ film required an annealing step at 850˚C to form a crystalline phase of $BaTiO_3$. Like earlier devices, this TFT has also been deposited on a p^{++}-Si substrate. The film is exceptionally transparent in the visible area and has a high electrical insulating nature due to the minimal scattering at the interface, indicating $BaTiO_3$ as a viable gate dielectric for TFT applications. Although this TFT required a bit higher voltage (~5V) to run this device. The electron mobility of the TFT was 0.028 $cm^2V^{-1}s^{-1}$ with an on/off ratio of 25.

In **Chapter 6,** the high-performance solution-processed metal oxide thin-film transistor (TFT) fabrication technique has been discussed by utilizing Li_2SnO_3 gate dielectric. Like the earlier device, these metal oxide TFTs were also fabricated on heavily p-doped silicon (p^{++} -Si) substrate using a sol-gel technique. Besides, an n-type TiO_2 thin film is used as an electron donor to the semiconductor/dielectric interface to enhance the device's performance. Because of this additional TiO_2 layer, the overall leakage current has been reduced essentially enhancing the on/off ratio of the device. An optimized device with this Li_2SnO_3 dielectric and a TiO_2 gate interface shows electron mobility of 3.47 $cm^2V^{-1}s^{-1}$, an on/off ratio of 50, and a low leakage current of density 3.8 x 10^{-5} A/cm^2 under 5-volt external bias, which can be suitable for using this film as a gate dielectric of a thin film transistor (TFT).

At the conclusion of the thesis, there is a reference list of journals and books that were utilized to bind our thesis.