Chapter 6

Fabrication and Characterization of n-ZnO Nanowires (NWs)/p-Si Heterojunction Diodes

6.1 Introduction

Various features and advantages of different nanostructures, such as nanowires, nanorods, nanotubes, nanoparticles, nanobelts etc [Wang (2004), Lu *et al*. (2006), Jagadish and Pearton (2006)] of ZnO have already discussed in Chapter-1. Among different 1D nanostructures, the ZnO nanowires (NWs) have been a subject of study since the 1950s [Jagadish and Pearton (2006), Duan (2008), Chen *et al*. (2009)] due to their tremendous potential for developing high performance nanodevices for future generation sensing and detection applications [Lu *et al*. (2006), Wang (2008), Logeeswaran *et al*. (2011)]. The present chapter has been devoted to study the synthesis and characterization of the ZnO NWs on p-Si substrates by thermal evaporation method. The electrical characteristics of the resultant n-ZnO NWs/p-Si heterojunction diodes have been discussed in details. The outline of this chapter is as follows:

Section 6.2 describes the synthesis of ZnO NWs on the aluminium (Al) doped ZnO (AZO) seed layer coated p-Si substrates and fabrication details of the n-ZnO NWs/p-Si heterojunction diodes by thermal evaporation method. Section 6.3 includes the current transport mechanism across n-ZnO/p-Si heterojunction diode by Anderson model. Results and discussions related to the characterizations of the vacuum deposited ZnO films and resultant n-ZnO/p-Si heterojunction diodes have been presented in Section 6.4. The section 6.5 presents the conclusion and summary of Chapter 6.

6.2 Experimental Details

This section includes the details of the fabrication of the AZO seed layer, ZnO NWs on AZO coated p-Si substrates and metal electrodes for the ohmic contacts on the ZnO NWs and p-Si substrates for achieving the n-ZnO NWs/AZO seed layer/p-Si heterojunction diodes under study by thermal evaporation method as discussed in the following:

6.2.1 Synthesis of n-ZnO Nanowires (NWs) on p-Si Substrates

Boron doped p-Si <100> substrates were cleaned by standard Piranha-HF method as described earlier in Chapter 3. The cleaned p-Si substrates were washed properly by de-ionized water and placed in the thermal evaporation unit (model 12A4D of HINDVAC, India) with a base pressure of 10^{-3} mPa, conventional molybdenum boat (i.e. source) as the heating filament, source to target (i.e. substrate) distance of 18 cm as discussed in Chapter 3. A seed layer of 1% Al doped ZnO (AZO) of thickness ~50 nm was then uniformly deposited on the p-Si substrate by evaporation of AZO pallets kept in the molybdenum boat of the vacuum coating unit. For making AZO pellets of appropriate amount (by weight), suitable amounts of ZnO and Al (1%) powders were first thoroughly mixed by using agate mortar and pestle set. The AZO pellets were then prepared with the help of a hot pressure setup. The AZO coated substrates were processed for rapid thermal annealing in the Ar gas atmosphere for 20 minutes at temperature of 550 °C. The annealed AZO coated p-Si substrates were then placed in the thermal evaporation chamber for depositing a uniform layer of metallic Zn of ~300 nm on the AZO seed layer under the same growth conditions as used earlier for the AZO layer. The Zn filings (99.99 %) from the MERCK Ltd, Mumbai India were used as the source material in the molybdenum boat of the deposition unit. The AZO seed layer coated p-Si substrates with the thermally deposited metallic Zn layer on the AZO seed layer were then placed in the oxidation furnace to convert the Zn layer into the ZnO layer. The oxidation process took place in the O_2 gas atmosphere at 600 °C temperature for the duration of 60 minutes [Khanlary *et al*. (2012)]. The top surface of the AZO coated p-Si substrates were found to be covered with a white grey film of ZnO layer after the completion of the thermal oxidation of the metallic Zn layer. One set of samples was cooled down to the room temperature for the thin film characterization purposes while another set of samples were used for fabricating the n-ZnO thin film/AZO seed layer/p-Si based heterojunction diodes described in following.

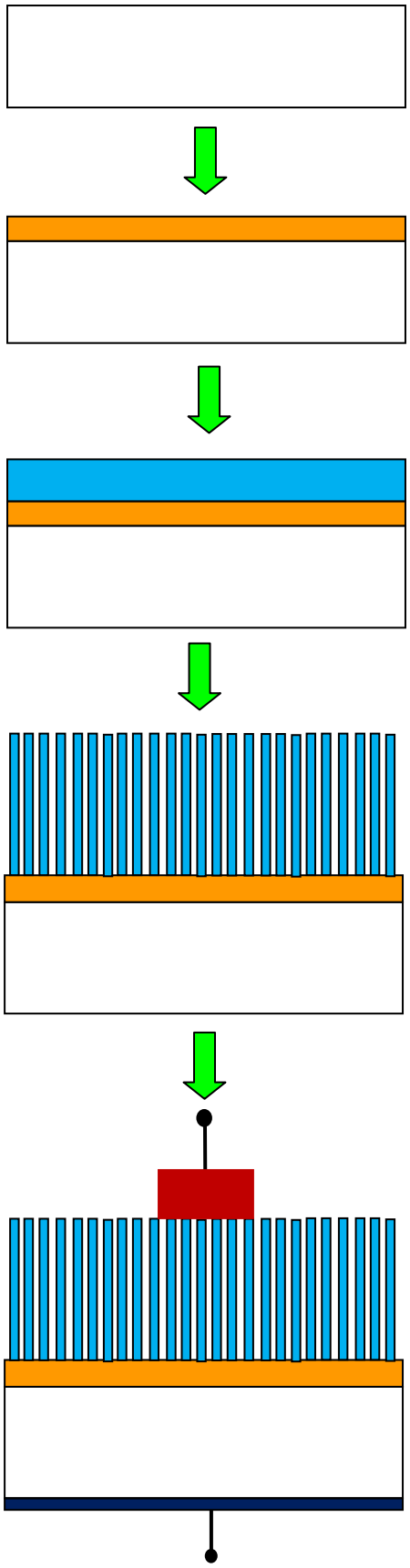

Figure 6.1: Schematic diagram of Al/Ti/n-ZnO NWs/p-Si /Al heterojunction diodes

6.2.2 Fabrication of n-ZnO/AZO/p-Si Heterojunction Diodes

The ohmic metal electrode (i.e. cathode) was fabricated by depositing Al/Ti (~80/70 nm) metal dots of 1mm diameter on the n-ZnO thin films side by the shadow mask techniques. Thus the effective area of each of the Al/Ti dots was fixed as $\sim 0.785\times10^{-2}\,cm^2$ which was expected to cover a large number of ZnO nanostructures under it. The anode electrode was fabricated by depositing Al metal (~80 nm) on the entire back surface side of the p-Si substrate by the thermal evaporation method under identical conditions as describe earlier. The entire fabrication process is schematically shown in Fig. 6.1.

6.3 Energy Band Diagram of the n-ZnO/p-Si Heterojunctions Diodes

The energy band diagram of the n-ZnO/p-Si heterojunctions under consideration has been shown in Fig.6.2. When the n-ZnO forms a junction with the p-Si in the n-ZnO/p-Si heterojunction diodes, the diffusion of electrons from the n-ZnO to p-Si will take place due to a concentration gradient at the heterojunction [Chirakkara and Krupanidhi (2012)]. This results in a positive space charge region in the n-ZnO near the junction, which, in turn, increases the conduction band energy thereby causing an upward band bending in the n-ZnO near the heterojunction interface. On the other hand, since the conduction band energy decreases in the p-Si, the downward band bending takes place in the p-Si side near the heterojunction interface as shown in the Fig.6.2 [Lee *et al*. (2010), Chirakkara and Krupanidhi (2012)]. Assuming the respective values of electron affinity of the ZnO and Si as $\chi_{ZnO}=3.7\,eV$ and $\chi_{Si}=4.05\,eV$ [Sze (1981), Majumdar and Banerji (2009)], the respective values of the conduction band offset and valance band offset at the p-Si/n-ZnO NWs heterojunction interface are calculated as $\Delta E_C=\chi_{ZnO}-\chi_{Si}=0.35\,eV$ and $\Delta E_V=\Delta E_g-\Delta E_C=2.353\,eV$ from the Anderson's model [Sze (1981), Mönch (2005)]. Clearly, the larger value of the valence-band offset than the conduction-band offset prevents the movement of holes from p-Si to n-ZnO [Sze (1981), Majumdar and Banerji (2009), Lee *et al*. (2010)] at the heterojunction interface. Thus, the current transport in the n-ZnO/p-Si hetrojunction diode considered in the present device can be determined predominantly by the flow of electrons from the n-ZnO NWs to the p-Si side of the heterojunction diodes [Dhananjay *et al.* (2007), Chirakkara and Krupanidhi (2012)]. The above mentioned mechanism can also be depicted from the Fig. 6.2.

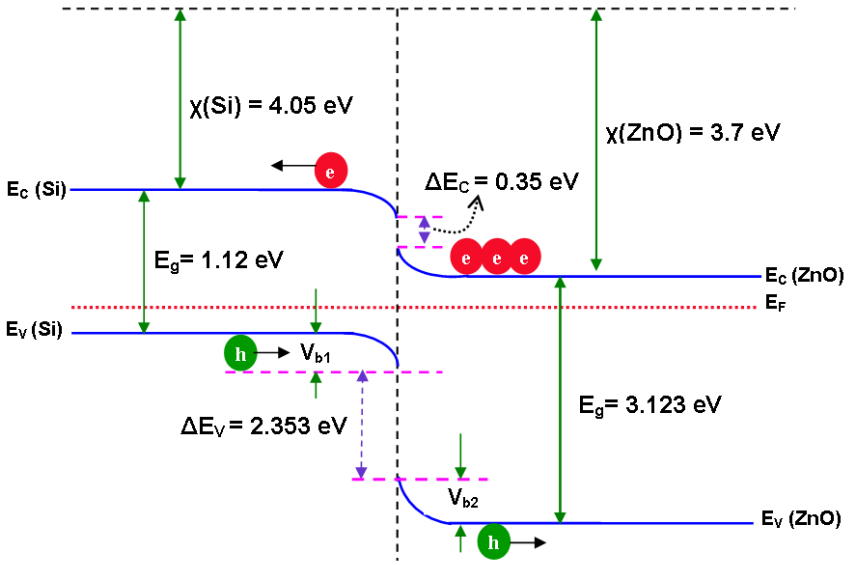

Figure 6.2: Energy band diagram of n-ZnO NWs/p-Si heterojunction diodes using Anderson's model

6.4 Results and Discussion

In this section we will first discuss the structural and optical characterizations of the ZnO thin films grown on AZO coated p-Si substrates by thermal evaporation method. Then we will analyze the measured C-V and I-V characteristics of the n-ZnO NWs/p-Si heterojunction diodes under considerations. The present section has been divided into following subsections.

6.4.1 ZnO Thin Film Characterization

The surface morphology, chemical composition and crystalline structure of the ZnO thin films grown on the AZO coated p-Si substrates have been studied by analyzing the FESEM images, EDS spectrum and XRD pattern respectively. The optical properties of the ZnO films under study have been investigated by using the room temperature PL spectrum.

6.4.1.1 Surface morphology

The FESEM images of the vacuum deposited ZnO thin films grown on the AZO coated p-Si substrate have been shown in Fig. 6.3 (a) and (b) at different magnification view. It is clear from the FESEM image shown in Fig 6.3 (a) that the whole surface of the p-Si

substrate is covered with large quantity of ZnO NWs with random orientations. The FESEM images with higher magnification level of 100 nm have shown in Fig.6.3 (b) presents a clear view of the ZnO NWs. The outer surfaces of the ZnO NWs are observed to be very smooth and clean throughout their lengths due to their large aspect ratio. The average diameter and length of the ZnO NWs are found to be in the range of ~ 40-100 nm and ~ 2-4 µm respectively.

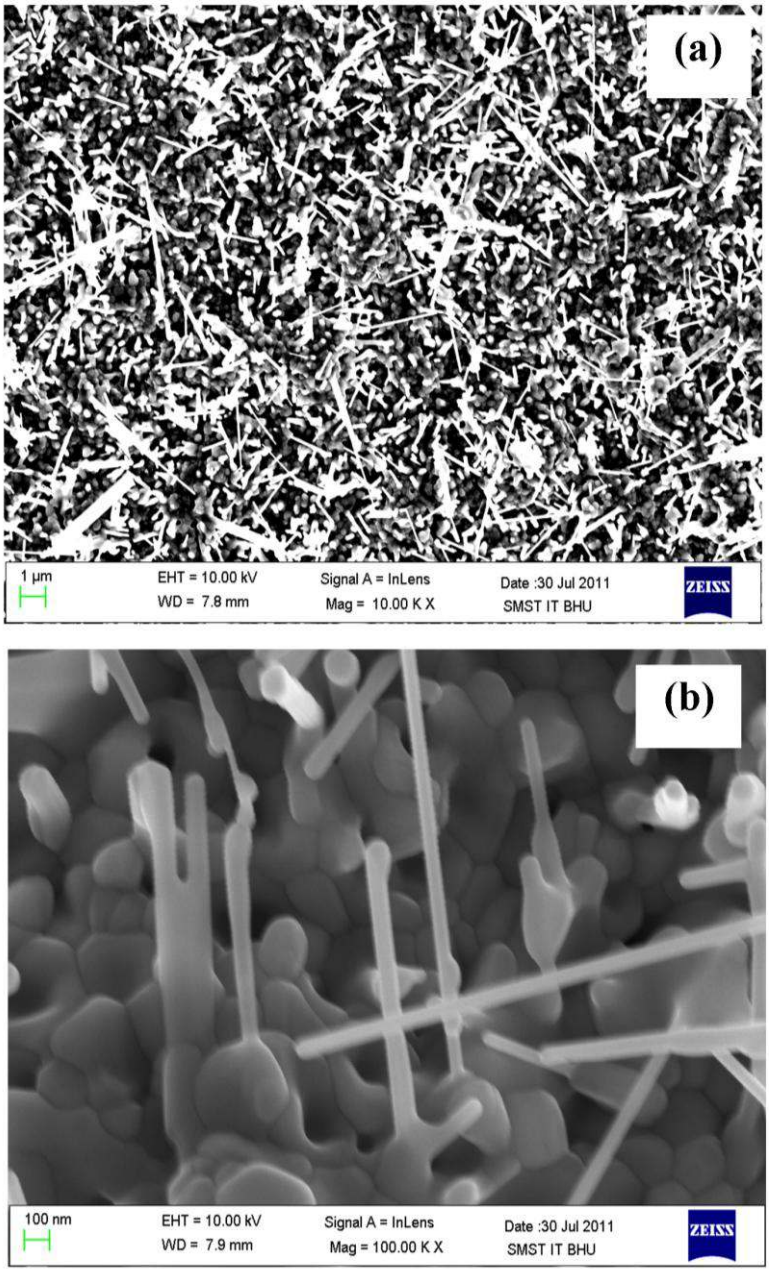

Figure 6.3: FESEM images (top view) of as-grown ZnO NWs on AZO seed layer coated p-Si substrates at different magnification view **(a)** 1µm **(b)** 100 nm

Some particle-like appearances on the substrate in Fig. 6.3 (b) may represent the ZnO NWs either not fully developed or at the start of their growth process. The possible reasons for such type of underdeveloped ZnO NWs may be the random distributions of temperature and oxygen flow throughout the sample during the oxidation process. However, it may be mentioned that no ZnO NWs structure was observed when the metallic zinc deposited directly on the p-Si substrate (i.e. without AZO seed layer) was oxidized [Singh *et al*. (2011)] to obtain the ZnO film on the p-Si substrate. Thus, it can be concluded that the AZO seed layer on the Si substrate acts as the perfect nucleation sites for promoting the growth of ZnO NWs on the p-Si substrates.

6.4.1.2 Chemical composition of ZnO NWs

The chemical composition of the as-synthesised ZnO NWs on p-Si substrates have been determined by the EDS spectrum shown in Fig.6.4. The EDS spectrum confirmed the presence of only zinc and oxygen elements in the film with a good quality of atomic percentage. Although a very small peak of Si is also present in the EDS spectrum due to the silicon substrate. The presence of another peak of carbon in the spectrum is due to the carbon tape used in the EDS measurement unit for sticking the sample. The higher percentages of zinc and oxygen elements in the spectrum as compared to the silicon confirm that the as-synthesised ZnO NWs were grown with very high density on the entire area of the substrate's surface. It may also be mentioned that the EDS results are well matched with the observations obtained from the FESEM images as discussed above.

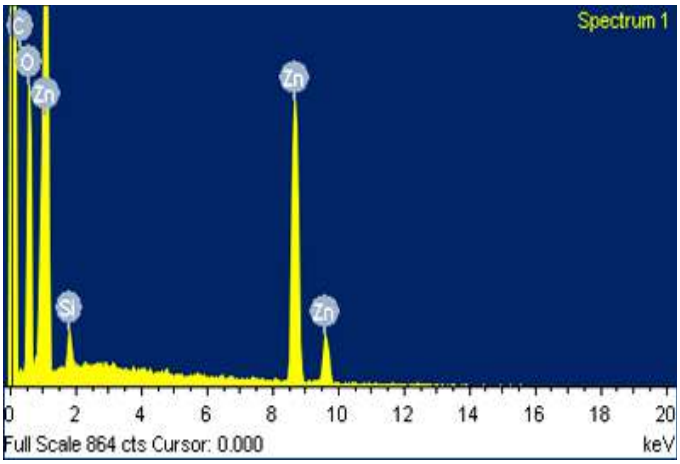

Figure 6.4: Typical EDS spectrum of ZnO NWs grown on p-Si substrates

6.4.1.3 *XRD pattern of ZnO NWs*

The XRD (18 kW Cu-rotating anode, model: XDMAX, PC-20, Rigaku, Tokyo, Japan) analysis of the as-grown ZnO NWs have been carried out in continuous scan mode with Cu Kα radiation with 2θ = 30-60^{o} as shown in Fig. 6.5. All the observed peaks at different diffraction planes (101), (002), (100), (110) and (102) with varying intensities are well matched with the hexagonal wurtzite structure of bulk ZnO as confirmed by JCPDS data card no. 36-1451 [JCPDS (1977), Jagadish and Pearton (2006)]. The peak of aluminum metal at 2θ =33.13 with diffraction plane (311) is also observed in the XRD spectrum due to presence of Al metal in the AZO seed layer [JCPDS (1977)]. No other peaks related to any metal or impurities are detected in the XRD pattern.

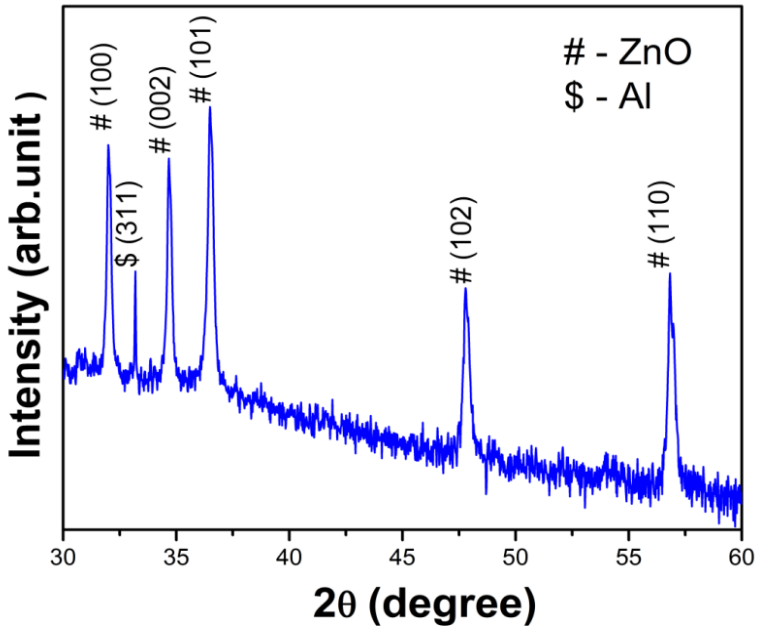

Figure 6.5: Typical XRD pattern ZnO NWs on AZO coated p-Si substrates

6.4.2 Photoluminescence Spectrum of ZnO NWs

The PL spectroscopy measurement (model: RPM 2000, Accent Optics, USA) has been carried out at room temperature in order to explore the possibility of the device for optoelectronic applications in the UV region. The PL spectrum of as-grown ZnO NWs on p-Si substrates have been shown in Fig.6.6. A strong near-band-edge emission (NBE) at wavelength of 397 nm is attributed to the recombination of free excitons through an exciton–exciton collision process [Liang *et al*. (2001), Djurišić and Leung (2006)]. The

near band edge emission (NBE) energy, say $E_{NBE}(\text{eV})$, of the ZnO film can be calculated by using the following relation

$$E_{NBE}(\text{eV}) = \frac{1240}{\lambda(nm)} \tag{6.2}$$

where $\lambda(nm)$ is the wavelength (in nm) at which the near band edge emission peak occurs in the PL spectrum.

The value of $E_{NBE}(\text{eV})$ is calculated as ~3.123 eV [Cha *et al.* (2008)] at $\lambda(nm) \sim 397\text{nm}$. In addition to the NBE peak, the PL also includes a weak but broad emission spectral region between ~450 to 550 nm. This weak and broad emission region consisting of blue-violet and green emissions at room temperature may be attributed to some native defect states, such as the oxygen vacancy (V_O), zinc interstitial (Zn_i) or zinc vacancy (V_{Zn}) etc present in the band gap of ZnO [Selim *et al.* (2007), Bayan and Mohanta (2011)]. It may be mentioned that the intensity of these defect emissions is very low as compared to that of the NBE emission.

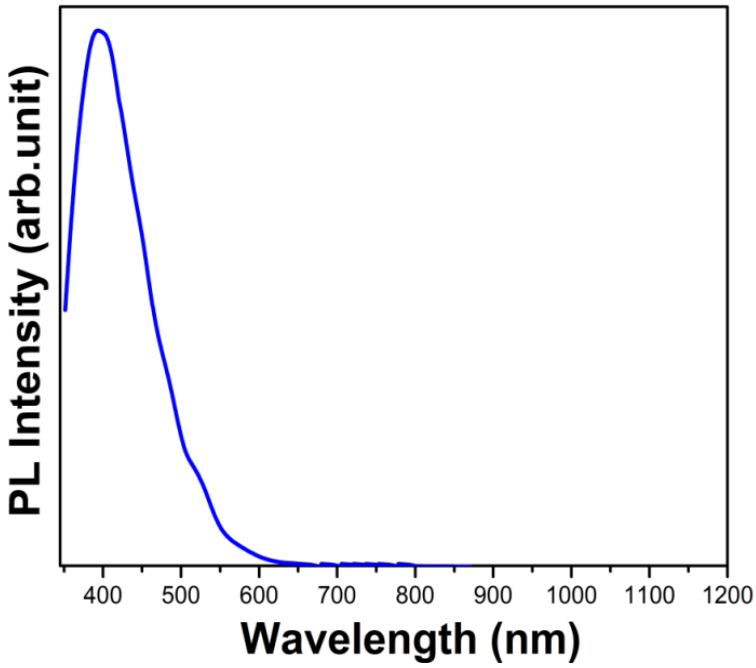

Figure 6.6: Room temperature PL spectrum of ZnO NWs grown on AZO coated p-Si substrates by thermal evaporation method

6.4.3 Analysis of Electrical Characteristics of n-ZnO NWs/p-Si Heterojunction Diodes

The electrical characteristics of n-ZnO NWs/p-Si heterojunction diodes have been determined by room temperature C-V characteristics and temperature dependent I-V characteristics as discussed in the following.

6.4.3.1 Capacitance-Voltage (C-V) characteristics

The reverse bias C-V characteristics of the n-ZnO NWs/p-Si heterojunction diodes measured at high frequency of 1 MHz have been analyzed in Fig.6.7 with a computer controlled impedance analyzer (HP-4284A, LCR meter) at room temperature. It may be mentioned here that the interface states at high frequency measurements of 1MHz cannot follow the ac signal and consequently do not contribute appreciably to the capacitance of heterojunction diodes [Perlmant and Feucht (1964), Chattopadhyay and Haldar (2001]. Since only the electron can participate in the conduction of current in the device (as discussed in the energy band diagram of heterojunction diodes in Section 6.3), we can represent the p-Si/n-ZnO NWs heterojunction as an one sided p^+-n abrupt heterojunction. Thus, the C-V characteristics of n-ZnO NWs/p-Si heterojunction diode can be described by following relation as already mentioned in Chapter 1 and 3 [Sze (1981), Chirakkara and Krupanidhi (2012)]

$$\frac{A^2}{C^2} \approx \frac{2\left(V_{bi} - V - \frac{kT}{q}\right)}{qN_D\varepsilon_{ZnO}} \tag{6.4}$$

where C and V_{bi} are the capacitance and built-in potential at the n-ZnO NWs/p-Si heterojunction, A is the junction area, and, N_D and ε_{ZnO} are the donor concentration and permittivity of the ZnO film. The measured values of C and A^2/C^2 have been plotted against the applied bias voltage as shown in Fig.6.7 (a) and 6.7(b) respectively. Eq. (6.4) shows that A^2/C^2 versus V characteristic should follow a linear relation and $A^2/C^2 = 0$ at $V = V_{bi} - kT/q$. Thus, extrapolating the linear segment of the A^2/C^2 versus V curve to the applied voltage axis as shown in the Fig. 6.7(b), the value of the built-in potential V_{bi} is determined as 0.55V. Using the slope (say, m) of the linear

segment of A^2/C^2 versus V plot, the value of N_D is calculated as 1.54×10^{15} cm^{-3}.

The value of the barrier height from the C-V characteristics at the n-ZnO NWs/p-Si heterojunction interface can be estimated as ~0.75 eV. Note that the experimental value of the barrier height estimated from the C-V measurement is a bit higher than its theoretical value of 0.72 eV obtained by the energy difference between the work functions of Si (i.e. ~ 4.97 eV) and ZnO (i.e. ~ 4.25 eV) [Chirakkara and Krupanidhi (2012)].

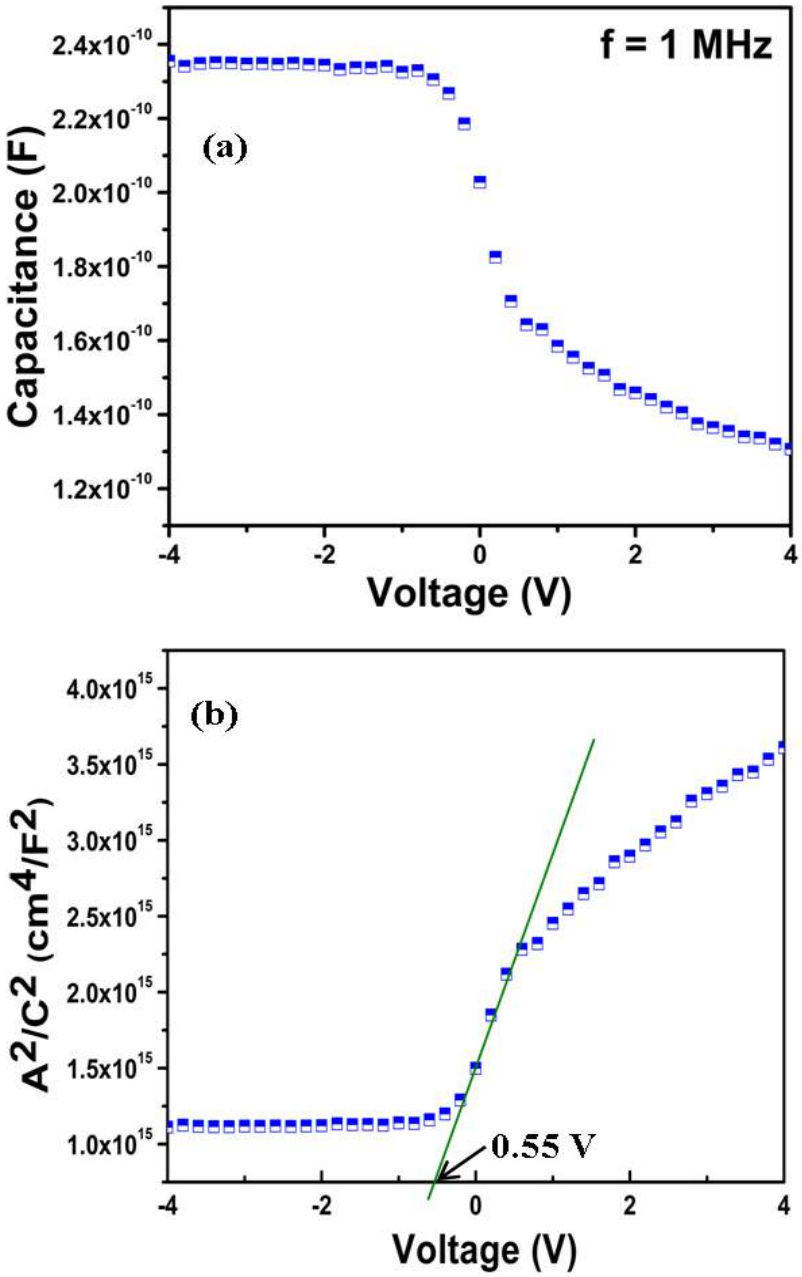

Figure 6.7: Room temperature reverse bias **(a)** C-V characteristics **(b)** A^2/C^2 vs. V characteristics of n-ZnO NWs/p-Si based heterojunction diodes

The depletion width at the n-ZnO NWs/p-Si heterojunction is calculated by using the following relation [Sze (1981), Majumdar and Banerji (2009)]:

$$W_D = \sqrt{\frac{\varepsilon_{ZnO}(V_{bi} - V)}{qN_D}} \tag{6.7}$$

Eq. (6.7) gives the value of the depletion width as $W_D \sim 0.40$ μm.

6.4.3.2 Temperature-dependent current-voltage (I-V-T) characteristics of n-ZnO NWs/p-Si heterojunction diodes

The temperature-dependent I-V characteristics of the n-ZnONWs/p-Si based heterojunction diodes have been investigated by using the semiconductor parameter analyzer (Agilent B1500A) in the voltage range from -2 to +2 V for different temperatures ranging from 300 to 423 K. Fig. 6.8 shows the temperature dependent I-V characteristic curves of the n-ZnONWs/p-Si heterojunction diode measured by applying negative potential to ZnO and positive potential to p-Si. During the measurements, the sample was kept in the dark condition.

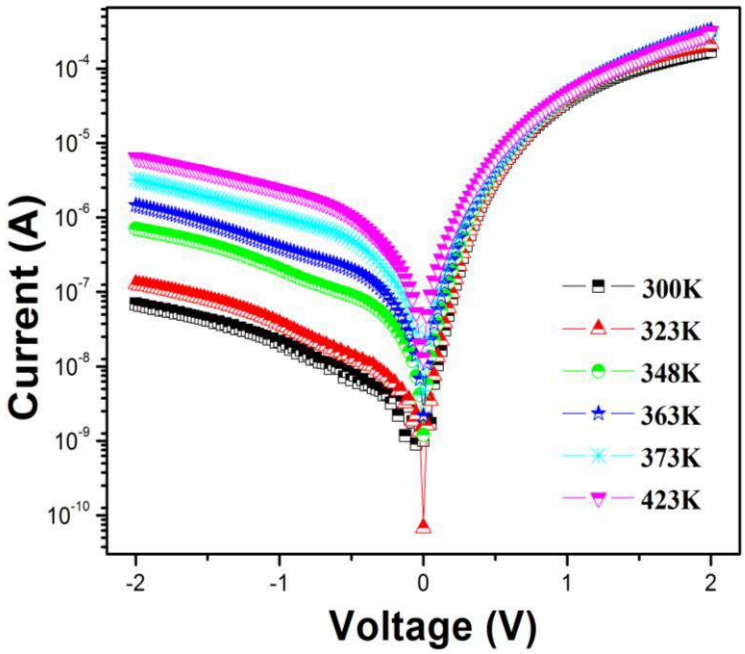

Figure 6.8: Temperature-dependent I-V characteristics of n-ZnO NWs/p-Si heterojunction diodes measured in the temperature range 300 to 423K.

Assuming the commonly used thermionic emission theory for the current transport mechanism at heterostructures, the I-V characteristics at n-ZnO NWs/p-Si heterojunction

diodes can be described in the similar manner as that of the Schottky contacts and can be given as [Sze (1981), Majumdar and Banerji (2009)]:

$$I = I_0\left\{= AA^*T^2\, exp\left(-\frac{q\phi_{B,eff}}{kT}\right)\right\} exp\left(\frac{qV}{\eta kT}\right) \tag{6.8}$$

where η is the ideality factor (defined as $\eta = (q/kT)\{dV/d(\ln I)\}$ and I_0 is the reverse saturation current, A is the diode contact area, $32 Acm^{-2}K^{-2}$ (for $m_e^* = 0.27m_0$) is the effective Richardson constant of ZnO [Sze (1981), Chirakkara and Krupanidhi (2012)] and $\phi_{B,eff} = (kT/q)ln(AA^*T^2/I_0)$ is the effective barrier height at zero bias. Eq. (6.8) clearly shows that the reverse saturation current is nearly proportional to the square of the temperature which makes the I_0 highly temperature dependent as observed in Fig. 6.8. It is also observed from Fig. 6.8 that the I_0 is slightly non-saturating with the reverse bias voltage. This can be attributed to the phenomenon of barrier height inhomogeneity at the n-ZnO NWs/p-Si heterojunction interface in the similar manner as explained by Yildiz *et al*. (2008) for their Al/SiO_2/p-Si Schottky diodes. For the inhomogeneous distribution of $\phi_{B,eff}$ across the entire interface of the n-ZnO NWs/p-Si heterojunction, the I_0 may be dominated by the carriers flowing through the low-barrier height patches which are controlled by potential at the saddle points. When the reverse bias is increased, the potential at the saddle points is decreased thereby making the I_0 slightly non-saturated with the applied reverse bias [Tung (1992), Yildiz *et al*. (2008), Korucu *et al.* (2013)]. However, the saturated downward curvature in the temperature dependent I-V characteristics at forward bias region can be attributed to the large surface state density near the bottom of the conduction band and the series resistance of the device [Yildiz *et al*. (2008), Faraz *et al*. (2012)]. It may be mentioned that, since the Pd/n-ZnO Schottky contact considered in Chapter-3 is also a heterojunction between the metal and ZnO, we can follow the same analysis techniques described in Chapter-3 for estimating the experimental values of the I_0, $\phi_{B,eff}$ and η from the temperature-dependent measured I-V characteristics over the temperature range of 300-423K of the n-ZnO/p-Si heterojunction diodes shown in Fig.6.8. The computed parameters are listed in Table. 6.1. The reverse saturation current at the n-ZnO NWs/p-Si heterojunction diodes increases with temperature from 300 to 423K in a similar manner as for the conventional diode due to increase in the thermally generated

minority carriers in the depletion region of the p-n junction diode [Sze (1981), Majumdar and Banerji (2009)]. From Table.6.1 it is observed that the zero bias barrier height of the n-ZnO NWs/p-Si heterojunction is increased from 0.73 to 0.95 eV whereas the ideality factor is decreased from 2.13 to 1.51 as the operating temperature increases from 300 to 423 K.

Table 6.1 Temperature-dependent electrical parameters of n-ZnONWs/p-Si heterojunction diode with temperature range from 300 to 423 K

T (K)	I_0 (A)	$\phi_{B,eff}$ (eV)	η
300	9.80×10^{-9}	0.73	2.13
323	1.42×10^{-8}	0.78	1.93
348	3.86×10^{-8}	0.82	1.84
363	6.17×10^{-8}	0.84	1.76
373	1.15×10^{-7}	0.85	1.72
423	1.97×10^{-7}	0.95	1.51

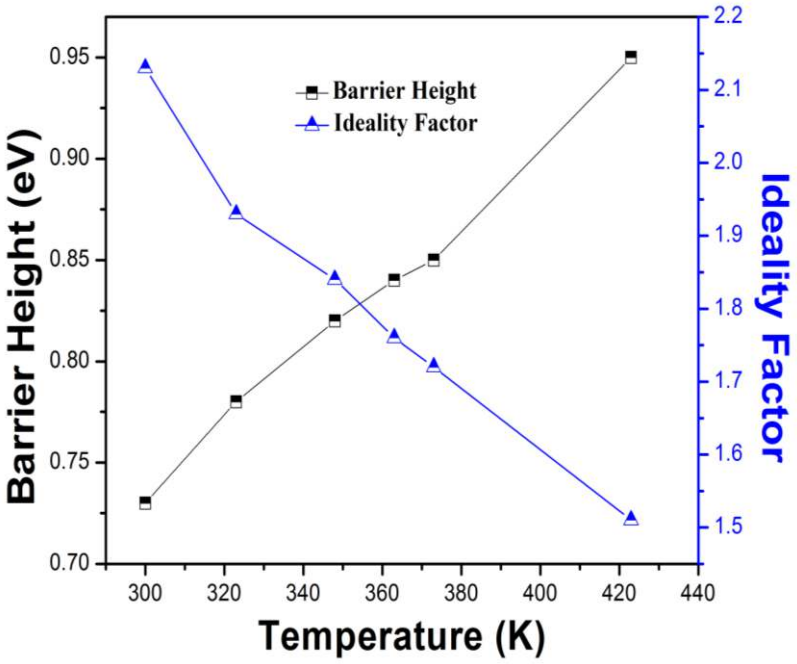

Figure 6.9: Variation of barrier height and ideality factor with temperature

The variation of barrier height and ideality factor with temperature is shown in Fig.6.9. The larger value (i.e. $\eta > 1$) of the ideality factor than its ideal value of unity (i.e. $\eta = 1$) is attributed to the recombination of electrons and holes in the depletion region and/or due to the increase in diffusion current by increasing applied voltage [Sze (1981)]. The values of the ideality factor are found to be in the range 1.5 – 2.31 with the lowest value being at the highest temperature. To examine the existence of the barrier height inhomogeneity [Werner and Güttler (1991), Tung (1992), Schmitsdorf *et al*. (1997)] at the n-ZnO NWs/p-Si heterojunction diode, it is required to express the zero-bias effective barrier height and ideality factor as a function of temperature. Figure 6.10 shows the variation of $\phi_{B,eff}$ as a function of η along with its least-squares fit. The linear fit clearly confirms the observation of Schmitsdorf *et al*. (1997).

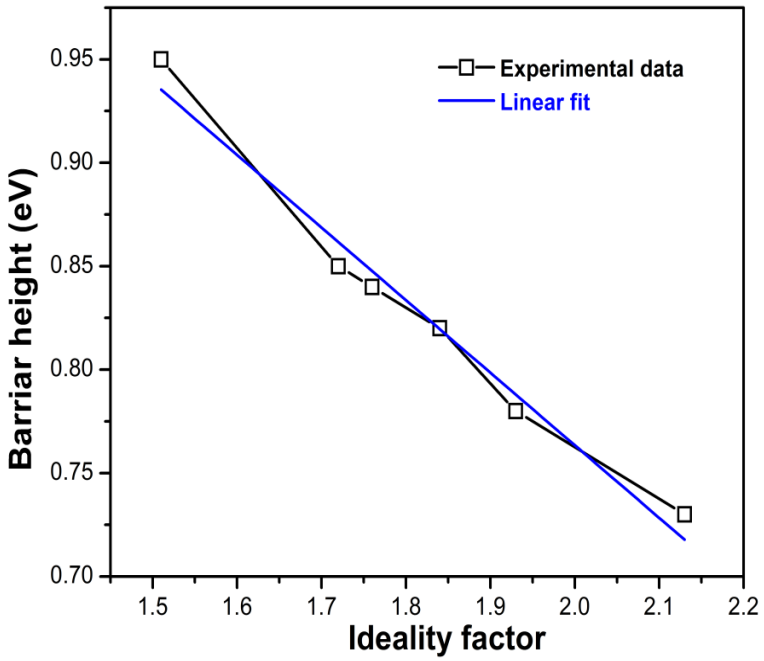

Figure 6.10: Variation of barrier height with ideality factor

Thus, in order to characterize the temperature dependent electrical characteristics of the n-ZnONWs/p-Si heterojunction diodes by using the thermionic emission model, it is required to express the zero-bias effective barrier height and ideality factor as a function of temperature by taking the effect of barrier spatial inhomogeneity [Werner and Güttler (1991)] into consideration as described in the following.

6.4.3.3 Effect of barrier inhomogenity on the barrier height, ideality factor and Richardson constant of n-ZnO NWs/p-Si heterojunction diodes

Since the Schottky junction is also a heterojunction as mentioned earlier, the barrier inhomogeneity phenomenon is also expected in the n-ZnO/p-Si heterojunction interfaces [Werner and Güttler (1991), Chirakkara and Krupanidhi (2012)] similarly as that existing at the Pd/ZnO thin film interfaces discussed in Chapter-3. Thus, we can use the same methodology (described for the Pd/ZnO thin film Schottky junction in Chapter-3) for investigating effect of the barrier inhomogeneities on the electrical characteristics of the n-ZnO NWs/p-Si heterojunction diodes under consideration. In this study, we have also used the Gaussian distribution function [Werner and Güttler (1991), Mtangi *et al*. (2009), Chirakkara and Krupanidhi (2012),] with a standard deviation σ_0 around a mean barrier height $q\phi_{B0,m}$ for describing the random variation of the spatial barrier heights across the n-ZnO NWs/p-Si heterojunction as considered previously in Chapter-3 for the Pd/ZnO thin film based Schottky diodes grown on n-Si substrates. We have used the subscript '0' to denote the zero-bias (i.e. thermodynamic equilibrium condition) of the junction.

Now, following the similar methodology described by Werner and Güttler [Werner and Güttler (1991)], we obtain the following relations [Chirakkara and Krupanidhi (2012)]:

$$\phi_{B,eff}(T) = \phi_{B0,m}(T=0) - \frac{q\sigma_0^2}{2kT} \tag{6.9}$$

$$\left(\frac{1}{\eta(T)} - 1\right) = \rho_1 - \frac{q\rho_2}{2kT} \tag{6.10}$$

$$\phi_{B,m}(V) = \phi_{B0,m} + \rho_1 V \tag{6.11}$$

$$\sigma^2(V) = \sigma_0^2 + \rho_2 V \tag{6.12}$$

where $\eta(T)$ is temperature-dependent ideality factor, $\phi_{B,m}(V)$ is the bias-dependent mean barrier height (in volt), $\sigma(V)$ is bias-dependent standard deviation, and ρ_1 and ρ_2 are voltage coefficient which may be dependent on temperature (T) and quantify the voltage deformation of barrier height distribution [Chirakkara and Krupanidhi (2012)]. Using the experimental values of $\phi_{B,eff}$ and η for different temperatures (Table. 6.1), the plots of

$\phi_{B,eff}(T)$ versus $q/2kT$ and $\left(\eta^{-1}(T)-1\right)$ versus $q/2kT$ have been shown in Fig. 6.12 along with their respective least-squares linear fit curves described by

$$\phi_{B,eff} \approx 1.44 - 0.03748(q/2kT) \tag{6.13}$$

$$\left(\eta^{-1}(T)-1\right) \approx 0.11 - 0.0339\,(q/2kT) \tag{6.14}$$

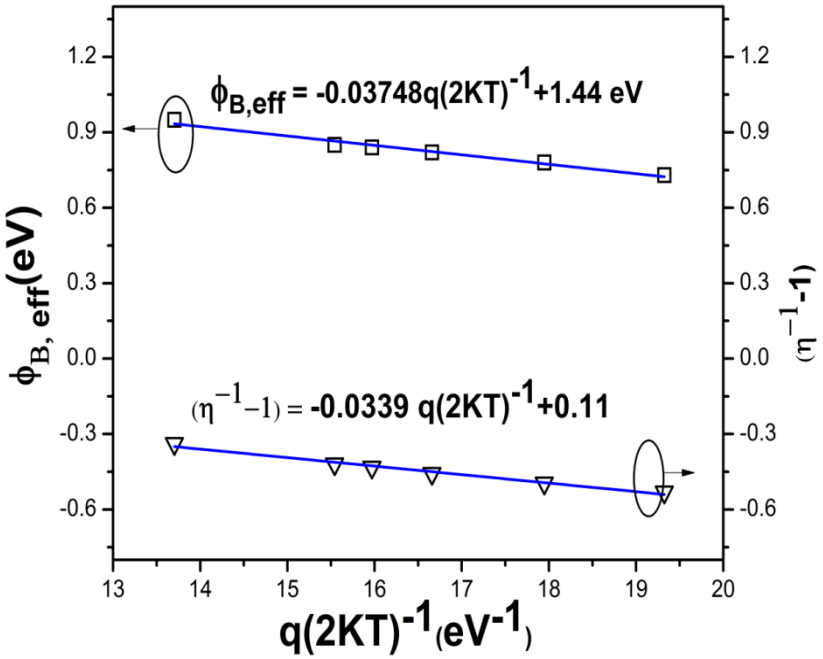

Figure 6.11: The $\phi_{B,eff}(T)$ and $\left(\eta^{-1}(T)-1\right)$ versus $q/2kT$ plot for determination of different electrical parameters.

By comparing Eq. (6.13) with Eq. (6.9), we obtain $\phi_{B0,m}$ = 1.44V and $\sigma_0^2 = 0.03748$ V at 0°K. The standard deviation σ_0 is a measure of the barrier inhomogeneity and hence the lower value of σ_0 corresponds to lower inhomogeneity of the barrier height distribution at the heterojunction interface. Using the above values in Eq. (6.13), we can obtain the value of the effective zero-bias mean barrier height at room temperature as $\phi_{B,eff}\left(T = 300°K\right)$ = 0.715 V which is very close to its theoretical value of 0.72 eV as discussed earlier [Romero *et al*. (2004), Dhananjay *et al*. (2007)]. Similarly, comparing Eq. (6.14) with Eq. (6.10), we can estimate the values of $\rho_1 = 0.11$ and

$\rho_2 = -0.0339\,\text{V}$. Using the above estimated values of ρ_1 and ρ_2 in Eq. (6.9), the value of the ideality factor can be determined at any desired temperature. The bias dependent characteristics of the mean barrier height and the standard deviation can be determined by using both the values of ρ_1 and ρ_2 in Eqs. (6.11) and (6.12) respectively. Following the methodology discussed in Chapter-1 and Chapter-3, we will now investigate the effect of barrier inhomogeneity on the determination of Richardson constant $\left(A^*\right)$ of ZnO by plotting the typical Richardson plots with and without considering the barrier inhomogeneity phenomenon as discussed below.

(a) Richardson constant without barrier inhomogenity

As we have already mentioned in Chapter 1 and 3 that the Richardson constant can be calculated by using the following relation

$$ln\left(\frac{I_0}{T^2}\right) = ln\left(AA^*\right) - \frac{q\phi_{B,eff}}{kT} \tag{6.15}$$

Fig. 6.12 shows the plot of $ln\left(I_0/T^2\right)$ versus q/kT, which deviates from its ideal linear nature due to the barrier inhomogeneity effect [Chirakkara and Krupanidhi (2012)]. The linear approximation of the experimental data (blue line) is also shown in Fig. 6.12. The experimental value of the A^* is thus obtained from the intercept (on the vertical axis) of the linear fit as $\sim 9.75\times10^{-8}\,Acm^{-2}K^{-2}$ which is much lower than the theoretically predicated value of $A^* = 32\,Acm^{-2}K^{-2}$ for n-ZnO [Chirakkara and Krupanidhi (2012)]

(b) Modified Richardson constant with barrier inhomogenity phenomenon

The modified Richardson plot by taking Gaussian distribution of barrier heights at the n-ZnO NWs/p-Si heterojunction into consideration can be described by the following relation as used in Chapter-1 and Chapter 3 for Schottky diodes structure [Chirakkara and Krupanidhi (2012), Al-Heniti *et al.* (2011a)]:

$$ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2{\sigma_0}^2}{2(kT)^2}\right) = ln\left(AA^*\right) - \frac{q\phi_{B0,m}(T=0)}{kT} \tag{6.16}$$

The modified Richardson plot (i.e. $ln\left(I_0/T^2\right) - q^2{\sigma_0}^2/2(kT)^2$ versus q/kT) plot) is

shown in Fig.6.13 along with its least square fit.

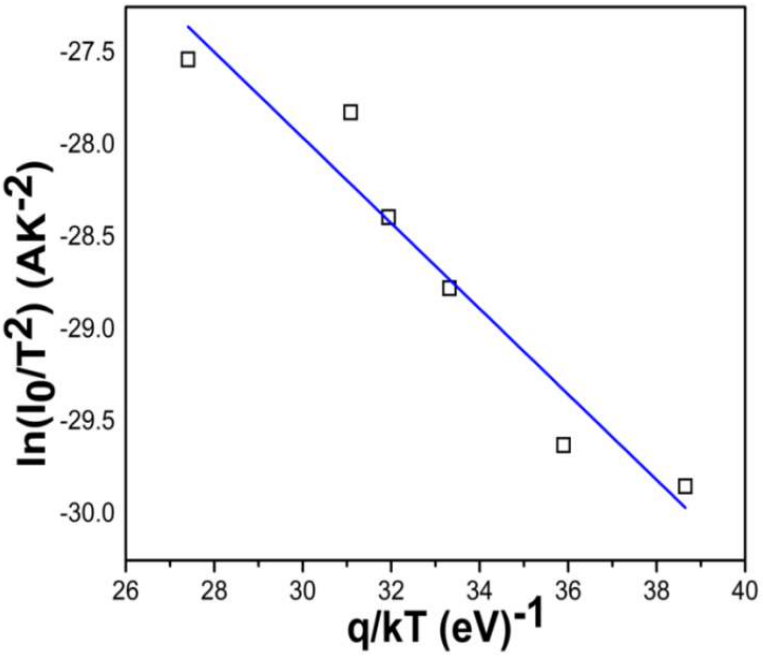

Figure 6.12: Richardson plot without barrier inhomogeneity taken into account

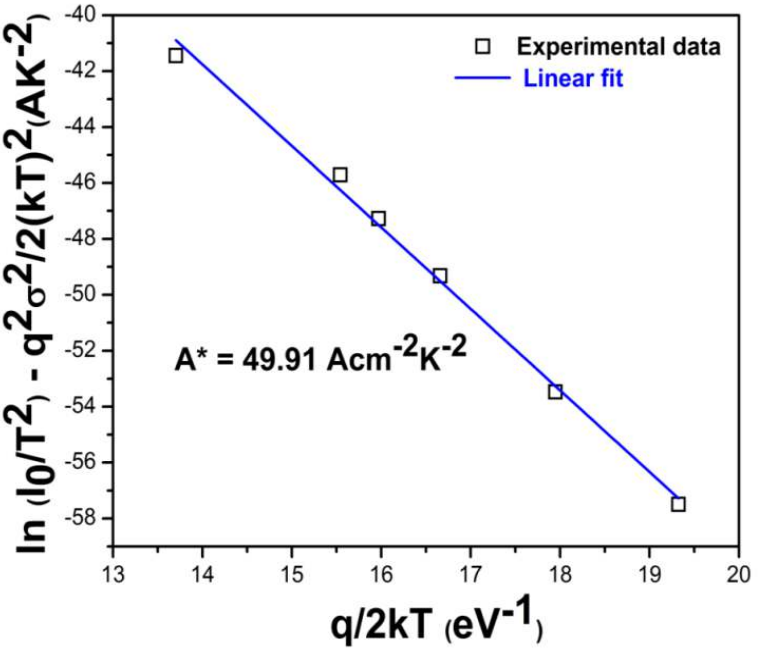

Figure 6.13: The Modified activation energy plot for calculation of Richardson constant by taking Gaussian distribution of barrier heights into consideration

Note that the modified plot is of the desired straight line nature whose intercept value at the vertical axis can be equated to $ln\left(AA^*\right)$ to determine A^* for a given diode area A. Using $A \sim 0.785\times10^{-2}$ cm^{-2}, the calculated value of A^* is found to be $\sim A^* \sim 49 Acm^{-2}K^{-2}$. Note that the value of the Richardson constant is drastically improved from an unrealistic value to a practical value when the barrier inhomogeneity phenomenon is taken into consideration. However, further improvement is required to obtain the Richardson constant closer to its theoretical value of $32 Acm^{-2}K^{-2}$.

6.4.3.4 Distribution of interface states at n-ZnO NWs/p-Si heterojunction diodes

To demonstrate the interface quality of n-ZnO NWs/p-Si heterojunctions diode, the density of interface states has been calculated as a function of the interface state energy [Romero *et al*. (2004), Das *et al.* (2010a)]. In general, the interface states are introduced due to oxidation of semiconductor surfaces, incomplete covalent bonds and chemical reactions during fabrication processes. Such defects produce a large density of interface states which are continuously distributed in the energy within the forbidden gap and cause leakage currents to flow [Chattopadhyay and Haldar (2001), Brillson *et al*. (2007), Das *et al.* (2010a)]. The density of interface states $\left(N_{ss}\right)$ can be extracted from I-V and C-V characteristics by using the following relation [Das *et al.* (2010a), Faraz *et al*. (2012)]

$$N_{ss} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}\{\eta(V)-1\}-\frac{\varepsilon_s}{W_D}\right] \tag{6.17}$$

where N_{ss} is the effective density of interface states, $\eta(V)$ is the voltage dependent ideality factor, W_D is the estimated space charge width from the $C-V$ measurements (described by Eq.(6.7)), δ is the thickness of the interfacial layer, ε_i is the permittivity of interfacial layer.

The voltage dependent ideality factor have been calculated by using the following relation [Faraz *et al*. (2012)]

$$\eta(V) = \frac{qV}{kT\,ln\left(\frac{I}{I_0}\right)} \tag{6.18}$$

The calculation of N_{ss} is very complex due to the interfacial layer since neither ε_i nor δ is known. Assuming $\delta = 0.5\,nm$ and ε_i as that of the free space as considered by Das *et al.* [Das *et al.* (2010a)], the energy of interface states (E_{ss}) with respect to the bottom of the conduction band (E_c) can be given by

$$E_c - E_{ss} = q(\phi_e - V) \tag{6.19}$$

where

$$\phi_e = \phi_{B,eff} + \left[1 - \frac{1}{\eta(V)}\right]V \tag{6.20}$$

is the voltage dependent barrier height.

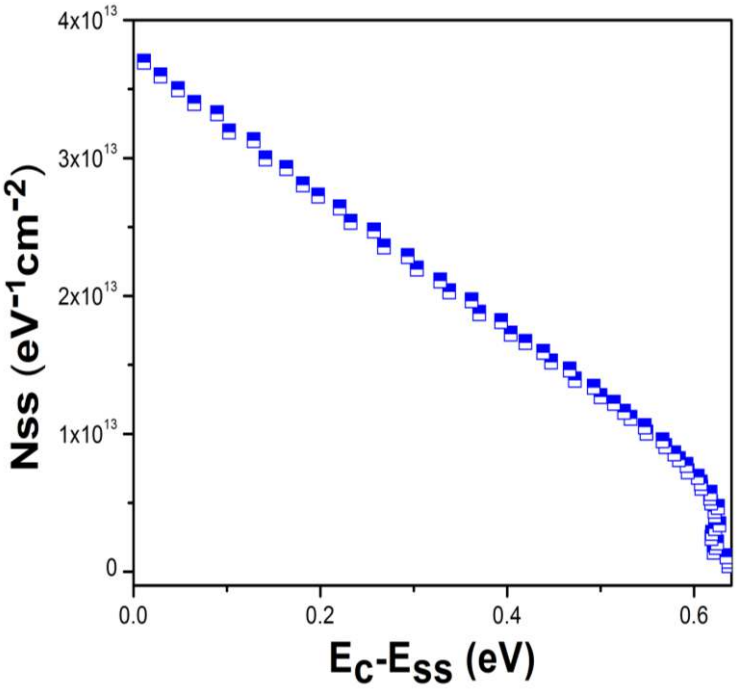

Figure 6.14: The distribution of interface states at n-ZnO NWs/p-Si heterojunction diodes

Fig. 6.14 shows decrease in the interface state density from 3.18×10^{13} eV^{-1} cm^{-2} to 4.59×10^{11} eV^{-1} cm^{-2} with an increase in $E_c - E_{ss}$ from 0.10 eV to 0.63 eV below the conduction band edges. The trend clearly shows that the density of interface states near the middle of the bandgap of ZnO semiconductor is nearly negligible as compared that near the bottom of the conduction band. This implies that there is no possibility of the pinning of Fermi level in the n-ZnO NWs/p-Si heterojunction diodes considered in the present work.

6.5 Summery and Conclusion

In the present Chapter, n-ZnO NWs have been synthesized on AZO coated p-Si substrates by thermal oxidation of vacuum deposited Zn at optimized temperature of 600 °C for duration of 60 minutes. Then the temperature-dependent I-V characteristics of the resultant n-ZnO/p-Si heterojunction diodes have been analyzed for the temperature range of 300-423K taking the barrier inhomogeneity phenomenon into consideration. Some of the significant observations of this Chapter are given below:

- The FESEM image of the ZnO thin film obtained by the oxidation of the thermally deposited metallic Zn on the AZO seed layer coated p-Si substrates confirms the growth of uniformly distributed ZnO NWs.
- The XRD analysis confirms a highly crystalline nature with a hexagonal wurtzite crystal structure of the ZnO NWs grown on the AZO seed layer under consideration.
- The PL spectrum of ZnO NWs exhibits a main peak of near band edge (NBE) emission at wavelength of 397 nm.
- The room temperature C-V characteristics and temperature-dependent I-V characteristics of the n-ZnO NWs/p-Si heterojunctions have been analyzed over the temperature range of 300-423 K.
- The barrier height estimated from the C-V measurements is found to be 0.75 eV which is very close to its theoretical value of 0.72 eV.
- The value of $\phi_{B,eff}$ is estimated to be 0.715 eV at room temperature which is very close to its theoretical value of 0.72 eV. The estimated value of the Richardson constant is observed to be improved from unrealistic value of $\sim 9.75\times10^{-8}\,Acm^{-2}K^{-2}$ to a more realistic value of $A^{*} \sim 49\,Acm^{-2}K^{-2}$ after taking barrier inhomogenity phenomenon into consideration.
- The interface state density is decreased from 3.18×10^{13} eV^{-1} cm^{-2} to 4.59×10^{11} eV^{-1} cm^{-2} with an increase in $E_c - E_{ss}$ from 0.10 eV to 0.63 eV below the conduction band edges. The trend clearly shows that the density of interface states near the middle of the bandgap of ZnO semiconductor is nearly negligible as compared that near the bottom of the conduction band.