Preface

CMOS scaling is responsible, for high end superfast computation and as the mankind is evolving the need of faster data gathering, analyzing and mining are some of the prominent areas which requires these functionalities. The standardization of CMOS scaling or one can say the growth of electronic industry is set upon the basic law suggested by the Gordan Moore, widely regarded as Moore's law. However, CMOS scaling is approaching to its fundamental limit imposed by side effects such as: SCEs, gate-oxide tunneling and increase in source/drain parasitic resistance. These aforementioned problems can be resolved by applying suitable device design engineering such as: gate dielectric engineering, channel engineering, gate electrode material engineering and source/drain engineering. Among all these device engineering techniques source/drain engineering improves drivability performance significantly without disturbing existing channel and gate parameters. This property of source/drain engineering applied on SCE immune gate- underlap structure has been a subject of intense research for the future generation VLSI/ULSI technology.

Analytical model for subthreshold characteristics in terms of potential distribution, threshold voltage, subthreshold swing and subthreshold current is an important aspect of any CMOS device. These parameters also helps to determine the effects of scaling on the switching performance of the device apart from understanding the working physics behind it. TCAD simulation of non-classical MOSFET structure is very helpful in understanding device behavior without fabrication. This thesis presents a detailed theoretical and simulation based study of the subthreshold characteristics as well as On state behavior of some non classical underlap USJ MOSFET structures. The effect of variation of channel-source/drain junction abruptness on subthreshold characteristics of underlap USJ DG MOSFET and consequence of change in source/drain elevation and side spacer material on both DG and GAA USJ MOSFET structures are studied in detail as briefly discussed below.

Chapter-1 introduces the impact of gate engineering, channel engineering and source/drain engineering techniques on different non-classical MOS transistors used for sustaining future generation scaling in the IC technology. Detailed literature survey covering research work done on non-conventional MOSFETs applying different types of source/drain engineering like recessed source/drain, raised source/drain and ultra shallow junction (USJ). It is observed from the literature that the performance (in terms of reduced SCEs and improved drivability) of the MOSFETs can be improved by combining the gate underlap, ultra shallow junction and source/drain elevation in the MOS transistors. Finally, the scopes of the thesis are outlined at the end of this chapter.

Chapter-2 presents unified models for the two-dimensional (2D) potential distribution, threshold voltage, of USJ Gate Underlap DG MOSFETs. Impact of channel-source/drain junction abruptness (straggle parameter of the lateral Gaussian doping profile in the source/drain region), underlap length, gate length, channel thickness and oxide thickness on the surface potential and threshold voltage have been investigated in details. Drain induced barrier lowering (DIBL) and loss of switching speed due to the DIBL have also been investigated. All the theoretical results have been compared with the ATLAS^{TM} TCAD data for the validation of the proposed theoretical model considered in this chapter. Finally validity of the proposed model has been verified by comparing it with the simulation data obtained by using the commercially available ATLAS^{TM} 2D device simulation software.

Chapter-3 deals with the modeling and ATLAS^{TM} based simulation of the subthreshold swing and subthreshold current USJ Gate Underlap DG MOSFETs. The effects of doping profile parameters and other device parameters on the threshold voltage, subthreshold current and subthreshold swing characteristics of the device are discussed in detail. Finally validity of the proposed model has been verified by comparing it with the simulation data obtained by using the commercially available ATLAS^{TM} 2D device simulation software.

Chapter-4, presents an ATLAS^{TM} TCAD based investigation of the combined effects of ultra shallow junction and source/drain elevation on the drivability performance of the non-abrupt ultra-shallow-junction (USJ) gate underlap DG MOSFETs. Effects of four different types of side spacer dielectrics namely Air, SiO_2, Si_3N_4 and HfO_2 on the current drive of the device have been studied in detail.

Chapter-5 considers a TCAD simulation based simulation study to investigate effects of drain/source elevation height (h_{SD}) and side spacer dielectric (between the gate and source/drain region) on the drivability performance of the non-abrupt gate-all-around (GAA) MOSFET structure. Quantitative effects of source/drain elevation height (h_{SD}) and side spacer dielectric materials (Air, SiO_2, Si_3N_4 and HfO_2) on the drivability performance of the device have been studied in the similar manner as discussed in Chapter-4 for USJ DG MOSFETs.

Chapter-6 presents the overall conclusion of the thesis drawn from the results presented in the previous chapters. Finally, some future scopes of work in the related area of research considered in the present thesis have been briefly outlined at the end of this chapter.