AUTHOR'S RELEVANT PUBLICATIONS

Journals:

[1] **K. Singh**, M. Kumar, E. Goel, B. Singh, S. Dubey, S. Kumar, and S. Jit, "Analytical Modeling of Potential Distribution and Threshold Voltage of Gate Underlap DG MOSFETs with a Source / Drain Lateral Gaussian Doping Profile," *J. Electron. Mater.*, vol. 45, no. 4, pp. 2184–2192, 2016.

[2] **K. Singh**, S. Kumar, E. Goel, B. Singh, M. Kumar, S. Dubey, and S. Jit, "Subthreshold Current and Swing Modeling of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile," *J. Electron. Mater.*, vol. 46, no. 1, pp. 579–584, 2016.

[3] **K. Singh**, S. Kumar, E. Goel, B. Singh, S. Dubey, and S. Jit, "Effects of Elevated Source/Drain and Side Spacer Dielectric on the Drivability Optimization of Non-abrupt Ultra Shallow Junction Gate Underlap DG MOSFETs," *J. Electron. Mater.*, vol. 46, no. 1, pp. 520–526, 2017.

[4] **K. Singh**, S. Kumar, E. Goel, B. Singh, and S. Jit, "Effects of Source / Drain Elevation and Side Spacer Dielectric on Drivability Performance of Non- Abrupt Ultra Shallow Junction Gate Underlap GAA MOSFETs," *Indian J. Phys. (under revesion)*, 2017.