Chapter 6

Conclusion and Future Scope

6.1 Introduction

The basic purpose of this thesis is to investigate the impacts of some source/drain engineering techniques namely graded S/D-channel junction (i.e. USJ) and source/drain elevation height on the performance of some non-classical gate-underlap MOS structures. The Chapter-1 presents the introduction, literature survey and scopes of the present thesis. Chapter-2 has been devoted to the analytical modeling of the channel potential and threshold voltage of the USJ gate-underlap DG MOSFETs while, the Chapter-3 reports the analytical modeling of the subthreshold current and subthreshold swing of the DG MOS structure considered in Chapter-2. In Chapter-2 and Chapter-3, we have analytically investigated the effects of the gate-underlap length and the straggle parameter of the Gaussian doping profile used in the source and drain regions on the subthreshold characteristics of the DG MOS structures with no source/drain (S/D) elevation. Chapter-4 and Chapter-5 present the ATLAS™ TCAD based simulation study for investigating the effects of S/D elevation height and dielectric spacer materials between gate-source and gate-drain regions on the drivability performance of the USJ gate-underlap DG-MOSFETs and cylindrical GAA MOSFETs, respectively. The present

chapter is devoted to summarize some important results of various chapters of this thesis as given in the following.

6.2 Summary and Conclusion

Chapter-1 discusses a brief introduction to IC technology, CMOS scaling and non-classical CMOS device structure. Various non-classical MOSFET structures obtained by employing different modifications in the bulk MOSFET structures have been briefly discussed. A brief review of some important state-of-the-art research works related to the performance optimization of subthreshold and drivability characteristics of some non-classical ultra shallow junction (USJ) multiple-gate MOSFETs with gate overlap/underlap structures have been discussed. Review of the non-classical MOSFETs obtained by employing S/D elevation height engineering has also been presented. The literature survey has shown that there are ample opportunities in investigating the subthreshold and drivability characteristics of USJ gate-underlap DG MOSFETs with and without employing the S/D elevation height engineering. There is also enough scopes for investigating the combined effects of USJ and S/D elevation height on the drivability performance of cylindrical GAA MOSFET structures. Based on the literature survey, the scopes of the present thesis have been outlined in the last section of this chapter.

Chapter-2 has been dedicated to the source/drain-channel junction abruptness dependent analytical modeling of the subthreshold potential distribution and threshold voltage of the gate-underlap DG MOSFETs with a Gaussian doping profile in the S/D region. Modeling has been done under the assumption that source/drain-channel junction is formed where source/drain Gaussian doping concentration becomes equal to the degenerated doping

value N_{de} $\left(2.7\times10^{19}\,cm^{-3}\right)$. Otherwise, the channel is assumed to be uniformly doped $1\times10^{16}\,cm^{-3}$. The parabolic potential approximation and conformal mapping techniques have been used to solve the 2D Poisson's equation for obtaining the potential distribution functions in different channel regions. Finally, the potential distribution function has been used to modeling the threshold voltage of the USJ gate-underlap MOSFET under study. Variations of the potential distribution and threshold voltage for different values of σ_L and gate-underlap length have been carried out. It is shown that that the SCEs can be controlled by changing the value of straggle parameter (σ_L) of the Gaussian profile of the S/D region and gate-underlap length. A reasonable agreement of the model results with the ATLAS^{TM} TCAD simulation data has confirmed the validity of the proposed model. The study thus demonstrates that σ_L and gate-underlap length can be used as two additional parameters for optimizing the threshold voltage of the device under consideration.

Chapter-3 presents the analytical modeling of the subthreshold current and subthreshold swing characteristics of the symmetric USJ gate-underlap DG MOSFETs with a Gaussian doping profile in the S/D region already considered in Chapter-2. The diffusion is considered to be the dominant phenomenon for the current transport mechanism in subthreshold regime operation of the proposed device. The potential distribution model proposed in the Chapter 2 has been utilized for developing the present subthreshold current model. The subthreshold swing model has been developed by using the concept of the effective conduction path parameter. The subthreshold current is increased with σ_L

due to the reduction in the effective channel length. For a fixed value of σ_L , the subthreshold current is increased with decreased channel length, decreased gate-underlap channel length, increased oxide thickness and increased channel thickness. The subthreshold swing is found to be increased with the decrease in the channel length as well as underlap length due to the increase in the short-channel effects. However, subthreshold swing is found to be reduced by increasing the abruptness of source/drain-channel junction. Thus proper tuning of σ_L and L_{ul} with the other geometrical parameters like L_G , t_{ox} and t_{si} helps in optimizing subthreshold swing and switching loss of the USJ gate-underlap DG MOSFET under consideration. The close agreement of the proposed model results with the ATLAS^{TM} simulation data has been observed.

Chapter-4 reports an ATLAS^{TM} based TCAD simulation study for investigating the effects of S/D elevation height (h_{SD}) and dielectric spacer materials on the drivability, transconductance and output conductance. Four different types of dielectrics namely Air, SiO_2, Si_3N_4 and HfO_2 have been considered in the regions between the gate and source and, gate and drain regions. In case of lower permittivity side spacer dielectrics (i.e. Air and SiO2), the off-state drain current I_{off} is reduced with increased elevation height (h_{SD}) due to band-to-band tunneling phenomenon. However, when the permittivity of the side spacer dielectrics is increased (by using Si_3N_4 and HfO_2), I_{off} is affected by the elevation height due to band-to-band tunneling (BTBT) and gate induced drain leakage (GIDL) phenomena. In case of Si_3N_4, BTBT dominates over the GIDL for lower values of h_{SD} while the GIDL dominates over the BTBT for higher h_{SD} values. However, the GIDL

dominates over the BTBT in case of HfO_2. Overall increase in the values of I_{on} and I_{on}/I_{off} ratio are achieved by increasing the permittivity of the side spacer dielectric and/or increasing the elevation height (h_{SD}). This study shows that the elevation height and permittivity of the side spacer dielectric provide additional flexibility in optimizing the drivability performance of the USJ gate-underlap DG MOSFETs under study.

In **Chapter-5**, we have investigated the effects of the elevation height and dielectric spacer on the drivability performance of the USJ gate-underlap GAA MOSFET structure in the similar manner as considered in Chapter-4. Four different dielectrics namely Air, SiO_2, Si_3N_4 and HfO_2 have also been used in the present study. For all the four side spacer dielectrics, increase in I_{on} and decrease in I_{off} are observed for increased values of h_{SD} thereby increasing I_{on}/I_{off} ratio. The maximum ~3000 % improvement in the I_{on}/I_{off} ratio is observed for the HfO_2 with $\sigma_L = 7\,\text{nm}$ and $h_{SD} = 30.5$ nm which is much greater than the corresponding maximum value of ~516% observed for the DG MOS structure with HfO2 as dielectric spacer, $\sigma_L = 7\,\text{nm}$ and $h_{SD} = 9.5$ nm) studied in Chapter 4.

6.3 Future Scope of Work

Since research is a never ending continuous process, there are ample opportunities to derive future scopes of research from the present thesis. Some of them are listed below:

- A continuous drain current model valid in all regimes of the device operation for short-channel USJ GU DG MOSFET can be worked out.
- A capacitance model of short-channel USJ GU DG MOSFET could be proposed.
- Besides the DG MOSFETs, there is also scope for developing analytical models for the subthreshold and On-state characteristics of USJ GU GAA MOSFETs with and without S/D elevation.
- The modeling concept presented in this thesis for USJ GU DG MOSFET can also be extended for USJ based other non-classical MOSFET structures like the junctionless field effect transistors (JFETs), tunnel field effect transistors (TFETs), Ring MOSFETs etc.
- A continuous drain current model valid in all regimes of the device operation for short-channel USJ based gate-underlap DG and GAA MOSFET structures with both the recessed S/D and elevated S/D features can be carried out.
- Analog and RF study of the short-channel USJ based elevated source/drain gate-underlap DG and GAA MOSFET structures can be carried out.
- Equivalent circuit models of the USJ based elevated source/drain gate-underlap DG and GAA MOSFET for both the low and high frequencies could be very useful for the design and simulation of the USJ based elevated source/drain gate-underlap DG and GAA MOSFET based analog and digital circuits.
- The fabrication and testing of a USJ based elevated source/drain gate-underlap DG and GAA MOSFET can be considered.