Chapter 5

Effects of Elevated Source/Drain and Side Spacer Dielectric on the Drivability Performance of Non-Abrupt Ultra Shallow Junction Gate Underlap GAA MOSFETs

5.1 Introduction

We have observed in Chapter-4 that the combined effects of drain/source elevation height engineering and graded S/D-channel junction engineering can be explored for improving drivability performance of the ultra shallow junction (USJ) gate-underlap DG MOSFETs. The objective of the present chapter is to investigate whether the improvement in the drivability performance of the USJ gate-underlap DG MOSFETs studied in Chapter-4 can be achieved in the Gate-All-Around (GAA) MOSFETs. It is already discussed in Chapter-1 that GAA MOSFET is one of the promising non-classical MOS transistor structures with better control over the SCEs than other multiple gate MOS structures (Chen & Tan 2014). Further, the circular GAA MOS structure is normally preferred over the quadruple GAA MOS structure due to its reduced SCEs owing to reduced corner effects (Song *et al.* 2006). In view of the above, the present chapter has been devoted to report an ATLAS^{TM} TCAD based simulation study for investigating the effects of S/D elevation height and dielectric spacer dielectric on the drivability performance of the non-planer USJ gate-underlap GAA MOSFET in the similar manner as considered for the DG MOSFET in Chapter-4. We have restricted our study for investigating the effects of

elevation S/D height and four different side spacer dielectrics namely Air (relative dielectric constant $(\varepsilon_r = 1)$), SiO_2 $(\varepsilon_r = 3.9)$, Si_3N_4 $(\varepsilon_r = 7.5)$ and HfO_2 $(\varepsilon_r = 20)$ on I_{on}, I_{off} and I_{on}/I_{off} ratio the circular GAA MOSFETs under consideration. The layout of this chapter can be given as follows.

In Sec. 5.2, the details of device structure and models used for TCAD simulation have been discussed. Section 5.3 presents some TCAD results and discussions related to I_{on}, I_{off} and I_{on}/I_{off} ratio. Finally, the major observations have been summarized in Sec.5.4.

5.2 Device Structure and Simulation Details

The schematic of the cylindrical gate ultra-shallow junction gate-underlap elevated source/drain MOSFETs structure used for simulation in the ATLAS^{TM} 3D TCAD simulator is shown in Fig 5.1(a). To approximate the USJ (i.e. non-abrupt S/D-channel junction), the Gaussian doping profile $N_{sd}(x) = N_{sdp}\exp(-x^2/2\sigma_L^2)$ with $N_{sdp} = 10^{20}\,cm^{-3}$ as the peak doping concentration and σ_L as the straggle parameter (Nandi et al. 2013) has been used in the S/D region as considered Chapter-4. Symbolic notations L_G $(18\,nm)$, W_{SP} $(20\,nm)$, W_{SD} $(25\,nm)$, L_{ul} $(10\,nm)$, t_{si} $(7\,nm)$, σ_L and t_{ox} $(1\,nm)$ are the gate length, Underlap channel length, side spacer thickness, source/drain thickness, silicon channel diameter, doping lateral straggle and gate oxide thickness of the device respectively. Fig 5.1(b) shows the S/D Gaussian doping profile variation with different lateral straggle σ_L in the proposed device structure. It is important to note that the elevated source/drain electrodes are formed over the uniformly doped source (i.e. the region between

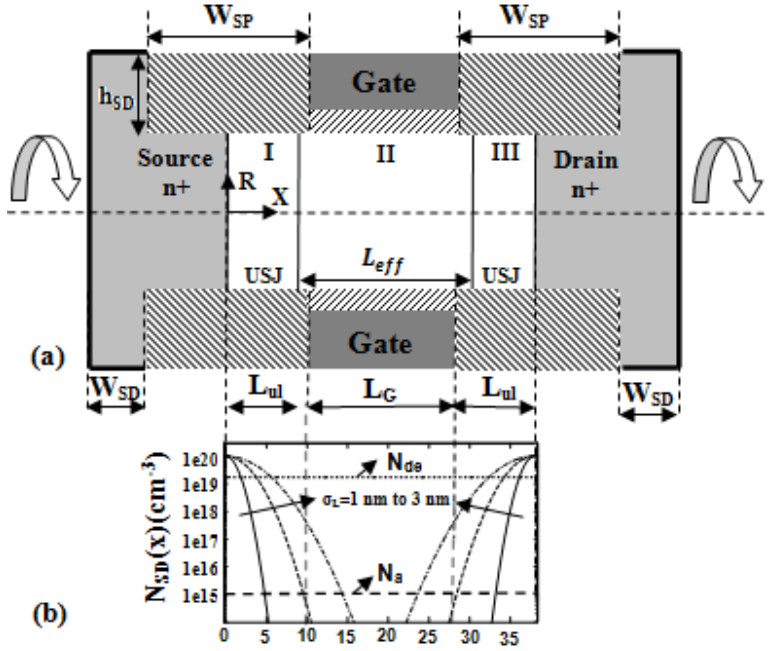

Fig 5.1 (a): Schematic view of the underlap elevated source/drain GAA MOSFET with following device parameters: source/drain width, $W_{SD} = 25\,\text{nm}$, gate-underlap length, $L_{ul} = 10\,\text{nm}$, gate length, $L_G = 18\,\text{nm}$, gate side spacer length, $W_{SP} = 20\,\text{nm}$, gate oxide thickness, $t_{ox} = 1\text{nm}$, and channel thickness, $t_{si} = 7\,\text{nm}$; **(b):** Dimensions of various channel regions used for simulation along with the lateral doping profile in the source/drain extension region for different values of straggle parameter σ_L.

$x = -(W_{SD} + W_{SP} - L_{ul})$ and $x = 0$) and drain (i.e. the region between $x = L_G + 2L_{ul}$ and $x = L_{ul} + L_G + W_{SD} + W_{SP}$) with a doping concentration of $1 \times 10^{20}\text{cm}^{-3}$ as considered in the conventional MOS devices for S/D contacts with low parasitic source and drain resistances. Two Gaussian doped regions are introduced in the underlap gate regions I and III with the peak doping ($1 \times 10^{20}\text{cm}^{-3}$) of the Gaussian profile placed at $x = 0$ and $x = L_G + 2L_{ul}$ at the source and drain sides respectively as shown in Fig 5.1(a). The

objective of introduction of such Gaussian doped regions at the ends of the uniformly doped source and drain regions in underlap- gate regions is to convert the abrupt source-channel and drain-channel junctions into the ultra-shallow graded junctions by reducing their junction depths. Since a doping concentration beyond $2.7 \times 10^{19} cm^{-3}$ can make Si into a degenerated material (Nandi *et al.* 2013), two degenerate Gaussian doped regions with concentration greater than or equal to $2.7 \times 10^{19} cm^{-3}$ will exist in the vicinity of $x = 0$ and $x = L_G + 2L_{ul}$ in the underlap gate region which effectively extend the source and drain regions towards the gate and reduce the effective channel length of the device. Thus, the proposed structure provides additional flexibility in terms of the source/drain elevation height, spacer dielectric constant and Gaussian doping profile parameters for controlling the drivability characteristics of the device while maintaining low parasitic source and drain resistances same as those of the conventional MOS devices. The standard drift-diffusion (DD) model together with the *fermi* model (classical Fermi-Dirac statistics of the carrier distribution), *srh* model (Schottky-Read-Hall recombination), *aug* model (Auger recombination) and *quantum* model (quantum mechanical effects) have been used in the ATLAS simulator for simulating the proposed device structure. The tungsten (work function $\varphi_M = 4.7$ eV) has been used as the gate material.

5.3 Results and Discussion

Variation of I_{on} and I_{off} as a function of source/drain elevation h_{SD} $(0.0 \text{ nm} \rightarrow 30.5 \text{ nm})$ for different side spacer dielectric materials, Air, SiO_2, Si_3N_4 and HfO_2 has been shown in Fig 5.2(a), Fig 5.2(b), Fig 5.2(c) and Fig 5.2(d) respectively. The rare phenomenon of

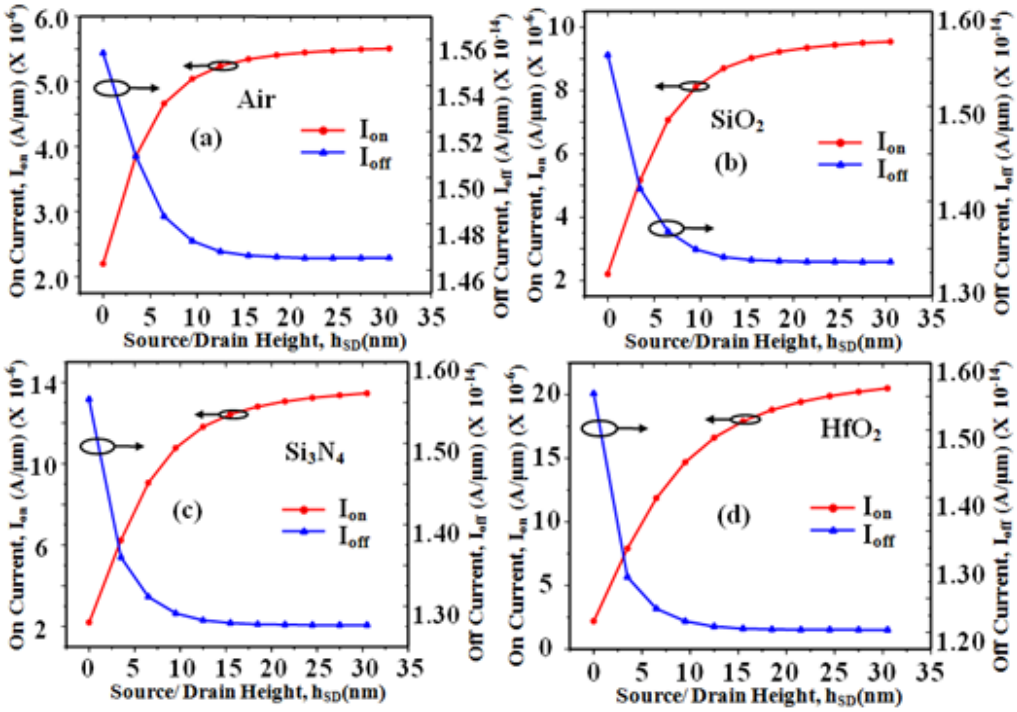

Fig 5.2: Drain current variations as a function of elevation height h_{SD} :**[Left]** On current versus h_{SD} plot for $V_{DS} = 1.0$ V and $V_{GS} = 1.0$ V; **[Right]** Off current versus h_{SD} plot for $V_{DS} = 1.0$ V and $V_{GS} = 0.0$ V for the four side spacer dielectrics namely Air (a), SiO_2 (b), Si_3N_4 (c) and HfO_2(d).

increase in I_{on} ($V_{GS} = 1.0$ V and $V_{DS} = 1.0$ V) and decrease in I_{off} ($V_{GS} = 0.0$V and $V_{DS} = 1.0$V) with solo increase in h_{SD} is observed in the proposed structure for all the above mentioned side spacer materials. The increase in h_{SD} , decreases overall source/drain resistance which results in increase of I_{on}. As this effect is dependent on on-state current (I_{on}) magnitude thus more dominant in the on-state of the device. Simultaneously, in subthreshold region the increase in the h_{SD} lowers the electric field at drain channel interface which leads to decrease of band to band tunneling in the device

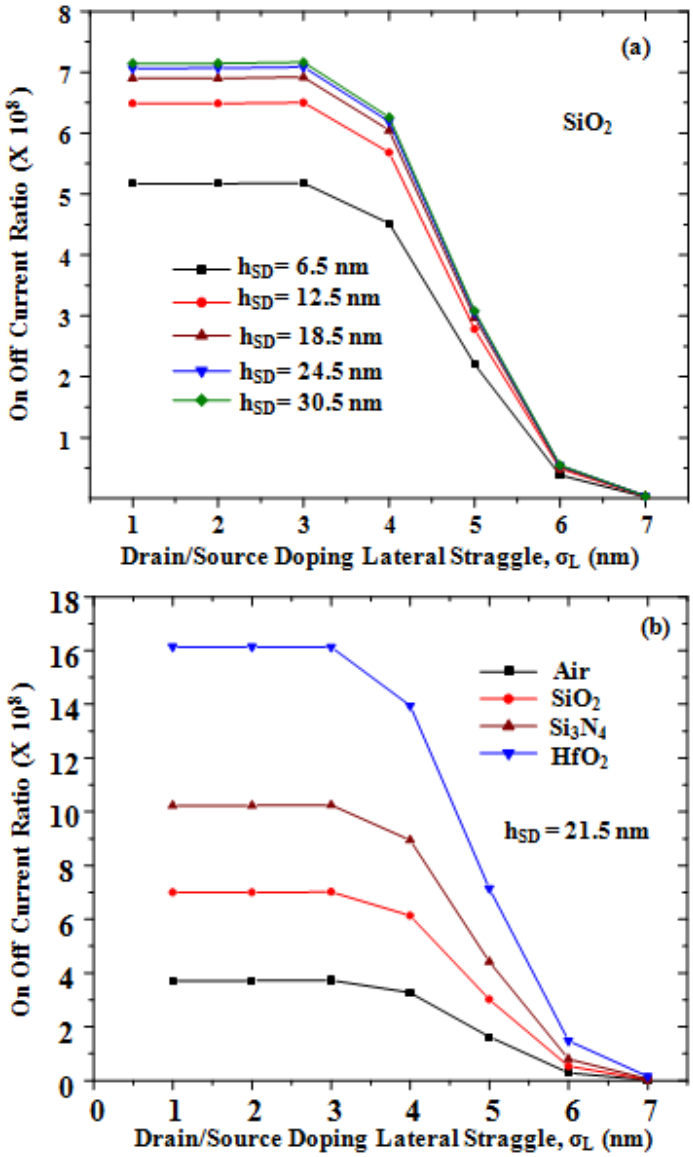

Fig 5.3(a): Drivability characteristics for SiO_2 spacer dielectric: I_{on}/I_{off} ratio versus the lateral straggle σ_L of the drain/source Gaussian doping profile for different h_{SD} values and **(b):** Variation of I_{on}/I_{off} ratio as a function of σ_L for different side spacer dielectric materials but with a fixed value of $h_{SD} = 2.15\text{nm}$.

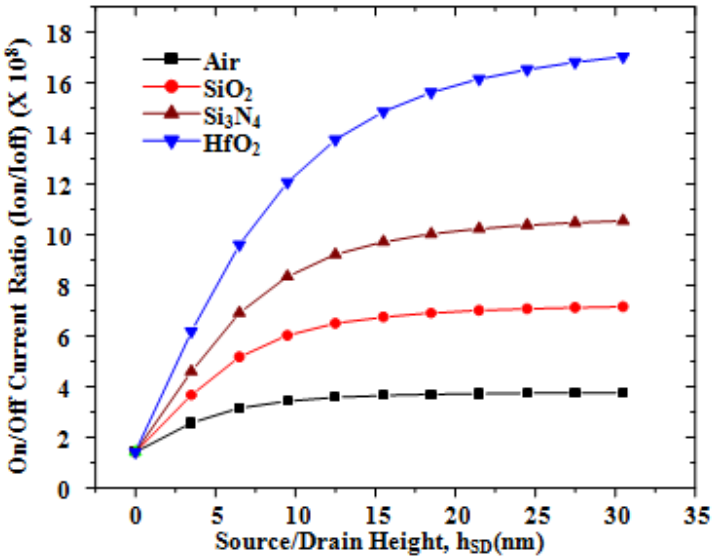

Fig 5.4: Variation of I_{on}/I_{off} ratio as a function of the drain/source elevation height h_{SD} for different side spacer dielectrics under study.

which in turn lowers the I_{off} (Zhang *et al.* 2003). As the magnitude of side spacer dielectric constant is increased, the gate originated electric field confinement increases towards the underlap channel region. This strengthens the coupling between gate and channel in the strong inversion region resulting in enhancement of I_{on} . While in subthreshold region, major gate originated electric field is captured in the high-k side spacers than in overlap gate oxide. Thus, the weak gate control (due to subthreshold region) in the overlap channel region further reduces and results in decrease of I_{off} .Fig 5.3(a) illustrates plot of I_{on}/I_{off} ratio versus σ_L (for different h_{SD} values from $(6.0\text{ nm} \rightarrow 30.5\text{ nm})$ in the step size of 6 nm) with SiO_2 as side spacer dielectric. Fig 5.3(b) demonstrates I_{on}/I_{off} ratio versus σ_L for fixed $h_{SD} = 21.5$ nm and different spacers (Air, SiO_2, Si_3N_4 and HfO_2). Fig 5.3(a) and Fig 5.3(b) reflects a common information

Table 5.1: (GAA) Percentage change in I_{on}/I_{off} value at different h_{SD} wrt I_{on}/I_{off} value at h_{ref} ($h_{ref} = h_{SD} = 0$ nm). $\left[\%\left(I_{on}/I_{off}\right) = \frac{\left(I_{on}/I_{off}\right)\big|_{h_{SD}} - \left(I_{on}/I_{off}\right)\big|_{h_{REF}}}{\left(I_{on}/I_{off}\right)\big|_{h_{REF}}} \times 100\right]$

h_{SD} (.nm)	% (I_{on}/I_{off}) at $\sigma_L = 1$ nm				% (I_{on}/I_{off}) at $\sigma_L = 4$ nm				% (I_{on}/I_{off}) at $\sigma_L = 7$ nm			
	Air	SiO_2	Si_3N_4	HfO_2	Air	SiO_2	Si_3N_4	HfO_2	Air	SiO_2	Si_3N_4	HfO_2
3.5	080.67	158.47	224.37	335.7	083.19	160.37	225.12	333.3	270.95	280.98	397.7	783.8
6.5	122.07	265.28	388.17	578.2	125.13	268.17	389.98	577.3	356.59	461.48	685.3	1505.0
9.5	141.81	324.80	489.43	752.5	145.22	328.63	492.92	751.6	397.27	564.18	866.3	2028.4
12.5	152.09	358.43	550.60	870.9	155.71	362.85	555.44	869.5	418.61	624.46	979.5	2378.4
15.5	157.48	376.71	586.06	949.4	161.22	381.58	591.81	947.0	430.49	659.50	1048.1	2598.5
18.5	160.60	387.58	608.20	1002.7	164.44	392.72	614.34	999.9	437.72	681.30	1091.9	2742.7
21.5	162.60	394.54	622.53	1040.2	166.45	399.70	629.08	1036.4	442.41	695.61	1121.3	2840.7
24.5	163.90	399.09	632.50	1066.9	167.80	404.48	639.17	1063.3	445.63	705.48	1141.8	2910.1
27.5	164.80	402.44	639.60	1087.2	168.75	407.84	646.42	1083.2	447.94	712.59	1156.7	2961.3
30.5	165.46	404.83	644.90	1102.7	169.48	410.31	651.91	1097.9	449.65	717.87	1168.0	3000.0

that, the increase in lateral straggle (σ_L)deteriorates the I_{on}/I_{off} ratio. On the other hand, with increase in h_{SD} and the value of side spacer dielectric constant; the I_{on}/I_{off} ratio increases, which reflects the benefit of using elevated source/drain (with high-k side spacer material) over non abrupt structures. Table 5.1 shows percentage variation in I_{on}/I_{off} ratio with respect to non- elevated structure, for Air, SiO_2, Si_3N_4 and HfO_2 as side spacer at different values of σ_L and h_{SD}.Consistent increase in percentage I_{on}/I_{off} ratio is observed in the Table 5.1. with increase in h_{SD}, σ_L and ε_{sp} of side spacer. Best improvement is observed with the HfO_2 (~3000 % at $\sigma_L = 7$ nm & $h_{SD} = 30.5$ nm) which is much higher than best percentage improvement by other side spacers Air (~449 %), SiO_2 (~717 %) & Si_3N_4 (~1068 %). And magnitude wise maximum value of I_{on}/I_{off} ratio is also with HfO_2 (~1.7×10^9 at $\sigma_L = 1$nm & $h_{SD} = 30.5$ nm) which is again much higher than other side spacers Air (~3.7×10^8), SiO_2 (~3.7×10^8) & Si_3N_4 (~1.05×10^9) . The drain current(I_{DS}) versus gate voltage (V_{GS}) [Left] and Transconductance (g_m)

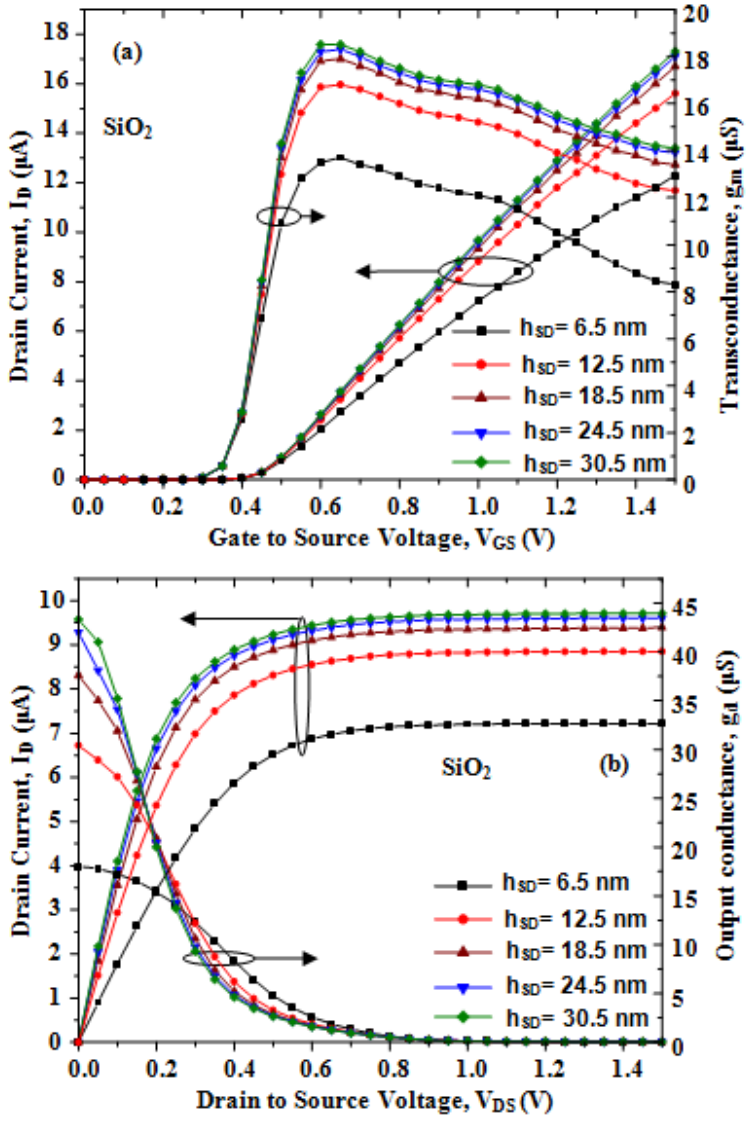

Fig 5.5(a): Variations of drain current and transconductance with respect to the gate to source voltage for different h_{SD} values but for the fixed spacer dielectric SiO_2 and straggle parameter $\sigma_L = 4\,nm$; **(b):** Variations of drain current and output conductance due to the drain to source voltage for different h_{SD} values but for the fixed spacer dielectric SiO_2 and straggle parameter $\sigma_L = 4\,nm$

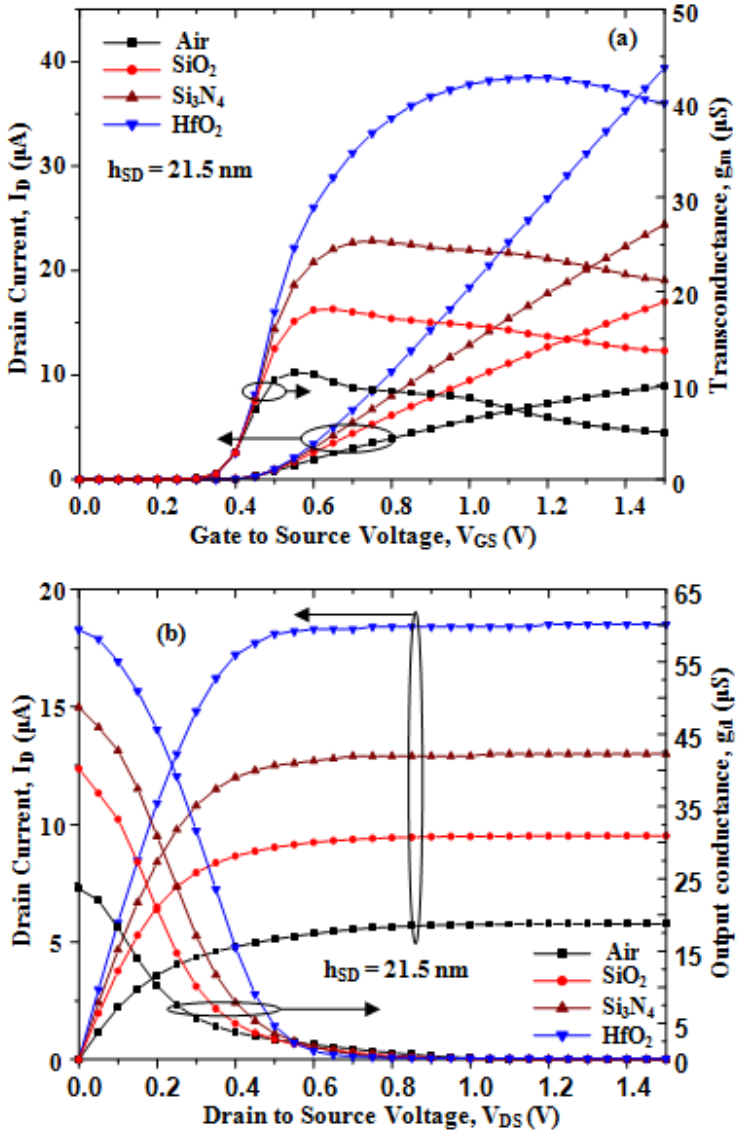

Fig 5.6(a): Plots of drain current and transconductance as functions of the gate to source voltage for the four different side spacer dielectric materials namely Air, SiO_2, Si_3N_4 and HfO_2 and $h_{SD} = 21.5\,nm$; **(b):** Variations of the drain current and output conductance due to the drain to source voltage for the four dielectric spacer materials Air, SiO_2, Si_3N_4 and HfO_2 with a fixed $h_{SD} = 21.5\,nm$.

versus V_{GS} [Right] have been shown in Fig 5.5(a) whereas Fig 5.5(b) shows the drain current(I_{DS}) versus drain voltage (V_{DS}) [Left] and output conductance g_d [Right] versus the V_{DS} characteristics for a fixed value of $\sigma_L = 4\,\text{nm}$,SiO_2 as spacer dielectric and different values of h_{SD} . In both the Figures a consistent increase in the magnitudes of I_{DS} , g_m and g_d with the increase in the h_{SD} has been observed. Fig 5.6 (a) shows I_{DS} versus. V_{GS} [Left] and g_m versus V_{GS} [Right] graphs while the I_{DS} versus V_{DS} [Left] and g_d versus V_{DS} [Right] characteristics have been shown in Fig 5.6 (b) for fixed values of $\sigma_L = 4\,\text{nm}$ and $h_{SD} = 21.5\,\text{nm}$ but for different spacer dielectrics under study. Consistent increase in the magnitudes of I_{DS} , g_m and g_d with the increase in spacer dielectric permittivity ε_{sp} (Air $\rightarrow$ HfO_2) is observed.

5.4 Conclusion

A detailed TCAD based simulation study for investigating the effects of S/D elevation height (h_{SD}) and four different dielectric spacers (namely Air, SiO_2, Si_3N_4 and HfO_2 in the gate and S/D regions) on the drivability, transconductance and output conductance of USJ GAA MOSFET have been reported in this chapter. It is observed that the I_{on}/I_{off} ratio of the device can be significantly improved by increasing h_{SD} and permittivity of the spacer dielectric material. While the I_{off} is reduced with increased h_{SD} by the band-to-band tunneling for lower permittivity spacer dielectrics Air and SiO_2, I_{off} it is noted to be increased significantly for higher permittivity spacer dielectrics Si_3N_4 and HfO_2 due to

the dominance of the GIDL phenomena over the band-to-band tunneling. Among the four spacer dielectrics under study, increase in I_{on} and decrease in I_{off} is only observed for the entire increased values of h_{SD} in case of SiO_2 spacer dielectric confirms that band-to-band tunneling is the dominant phenomena for all values of h_{SD}. However, both the I_{on} and I_{on}/I_{off} ratio are improved by using higher permittivity spacer dielectrics. Further, while I_{on} is increased with the straggle parameter σ_L of the Gaussian profile in the source/drain region, the overall I_{on}/I_{off} ratio is decreased with increased σ_L. Moreover, the transconductance and output conductance characteristics are also improved with the increased value of h_{SD} for different spacer dielectric materials. In brief, the elevation height of the source/drain regions, permittivity of the side spacer dielectric and σ_L can be explored as additional parameters for optimizing the drivability as well as other performance parameters of the sub-20nm non-abrupt GAA MOSFETs structure under consideration.