Chapter 4

Effects of Elevated Source/Drain and Side Spacer Dielectric on the Drivability Optimization of Non-Abrupt Ultra Shallow Junction Gate-underlap DG MOSFETs

4.1 Introduction

In the last two chapters, we have investigated the subthreshold characteristics of ultra shallow junction gate-underlap DG MOSFETs with a lateral Gaussian doping profile at the source/drain region to reduce the abruptness of the source-channel and drain-channel junctions.It has been shown that the source/drain (S/D) doping profile parameters as well as gate-underlap length can be explored as the additional parameters for optimizing the subthreshold characteristics such as the threshold voltage, subthreshold current and subthreshold swing of the gate-underlap DG MOSFETs. It is already discussed in Chapter -1 that while the source/drain doping profile engineering can be used for subthreshold performance optimization of the MOS transistors (as discussed in the previous two chapters) (Nandi, Saxena, and Dasgupta 2013), the source/drain elevation engineering can be used for controlling the ON-state I_{on} drain current and I_{on}/I_{off} current ratio of the MOS devices (Shenoy *et al.* 2003), (Chen *et al.* 2013). Further, the drivability of the MOS transistors are also observed to be dependent on dielectric spacer material between the elevated source and gate, and elevated drain-gate regions. In view of the above, this chapter has been devoted to present a ATLAS^{TM} TCAD based

simulation study for investigating the combined effects of S/D elevation height, say h_{SD}, and permittivity of four different side spacer dielectrics namely Air (relative dielectric constant $(\varepsilon_r = 1)$), SiO_2 $(\varepsilon_r = 3.9)$, Si_3N_4 $(\varepsilon_r = 7.5)$ and HfO_2 $(\varepsilon_r = 20)$ on the On-state current I_{on} ,off-state current I_{off} and On-to-Off current ratio I_{on}/I_{off} of the gate-underlap elevated source/drain DG MOSFETs with a lateral Gaussian doping profile in the S/D region as considered in the previous chapters. The outline of this chapter is given as follows:

In Sec.4.2, the details of the proposed device structure and models used in the ATLAS^{TM} TCAD software for proposed structure simulation have been discussed. Section 4.3 presents the results and discussions related to the effects of elevation height and dielectric spacers on I_{on}, I_{off} and I_{on}/I_{off} ratio of the elevated DG MOSFET structure under study. Finally, Sec 4.4 outlines the summary and conclusion of this chapter.

4.2 Device Structure and Simulation Details

The schematic of the symmetric ultra-shallow junction gate-underlap elevated source/drain DG MOSFET structure considered in the present study is shown in Fig. 4.1. The symbols L_G $(18\,\text{nm})$, W_{SP} $(20\,\text{nm})$, L_{ul} $(10\,\text{nm})$, t_{si} (7 nm), σ_L and t_{ox} (1 nm) are the gate length, side spacer length, underlap channel length, silicon film thickness, lateral straggle and gate oxide thickness of the device, respectively. Figure 4.1(b) shows the dimensions of various regions of the channel used for simulation along with the Gaussian

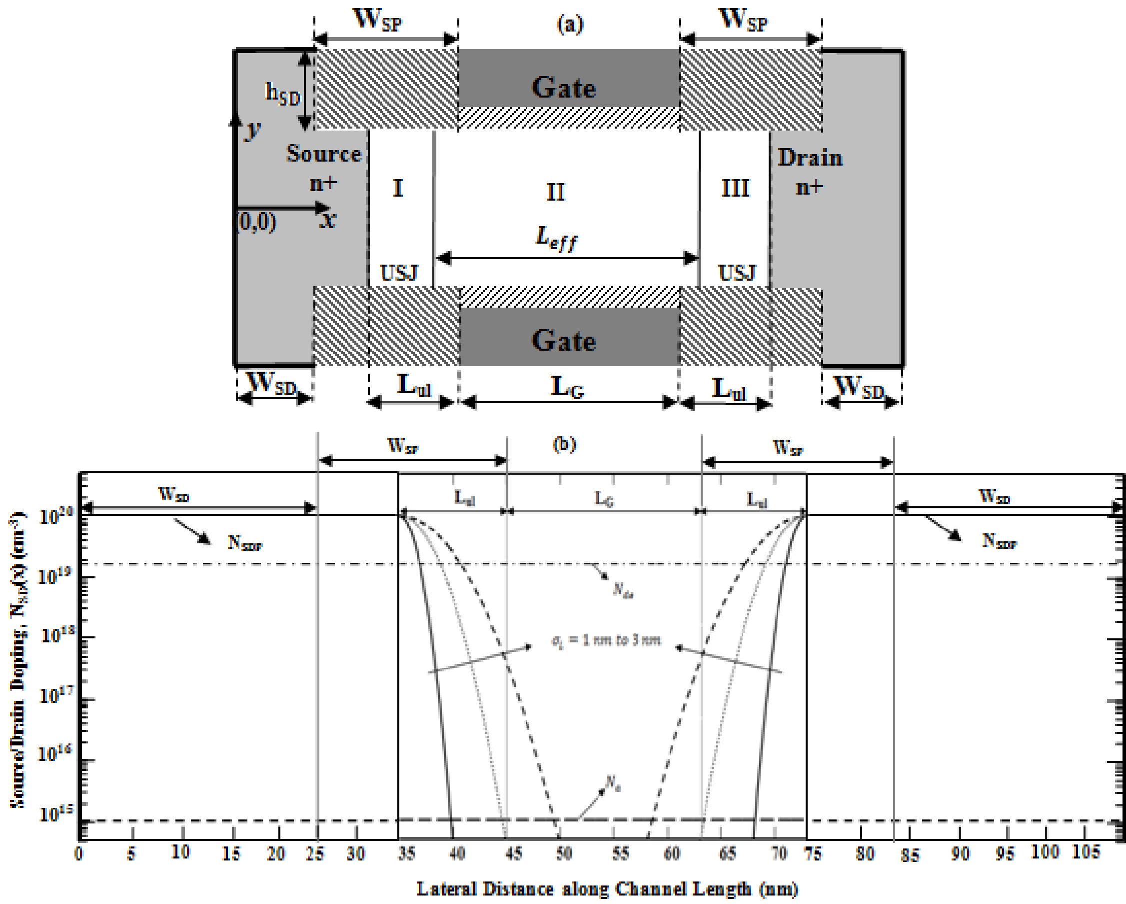

Fig4.1: (a) Schematic view of the underlap elevated source/drain DG MOSFET with following device parameters: source/drain width, $W_{SD} = 25\,nm$, gate-underlap length, $L_{ul} = 10\,nm$, gate length, $L_G = 18\,nm$, gate side spacer length, $W_{SP} = 20\,nm$, gate oxide thickness, $t_{ox} = 1\,nm$, and channel thickness, $t_{si} = 7\,nm$;**(b)** Dimensions of various channel regions used for simulation along with the lateral doping profile in the source/drain extension region for different values of straggle parameter σ_L.

profiles for different values of lateral straggle σ_L in the channel of the device. It is important to note that the elevated source and drain electrodes are formed over the uniformly doped source (i.e. the region between $x = 0$ and $x = W_{SD} + W_{SP} - L_{ul}$) and drain

(i.e. the region between $x = W_{SD} + W_{SP} + L_G + L_{ul}$ and $x = W_{SD} + W_{SP} + L_G + L_{ul} + W_{SD}$) with a doping concentration of $1 \times 10^{20}\text{cm}^{-3}$ as considered in the conventional MOS devices for S/D contacts with low parasitic source and drain resistances. Two Gaussian doped regions are introduced in the underlap gate regions I and III with the peak doping ($1 \times 10^{20}\text{cm}^{-3}$) of the Gaussian profile placed at $x = W_{SD} + W_{SP} - L_{ul}$ and $x = W_{SD} + W_{SP} + L_G + L_{ul}$ at the source and drain sides respectively as shown in Fig. 4.1. The objective of introduction of such Gaussian doped regions at the ends of the uniformly doped source and drain regions in the gate-underlap regions is to convert the abrupt source-channel and drain-channel junctions into the ultra-shallow graded junctions by reducing their junction depths as already considered in the previous two chapters. Since a doping concentration beyond $2.7 \times 10^{19}\text{cm}^{-3}$ can make Si into a degenerated material (Nandi, Saxena, and Dasgupta 2013), two degenerate Gaussian doped regions with concentration greater than or equal to $2.7 \times 10^{19}\text{cm}^{-3}$ will exist in the vicinity of $x = W_{SD} + W_{SP} - L_{ul}$ and $x = W_{SD} + W_{SP} + L_G + L_{ul}$ in the underlap gate region which effectively extend the source and drain regions towards the gate and reduce the effective channel length of the device. Thus, the proposed structure provides additional flexibility in terms of the source/drain elevation height, spacer dielectric constant and Gaussian doping profile parameters for controlling the drivability characteristics of the device while maintaining low parasitic source and drain resistances same as those of the conventional MOS devices. The standard drift-diffusion model along with the *fermi* model for the classical Fermi-Dirac statistics of the carrier distribution, *srh* model for the Schottky-Read-Hall recombination, *aug* for Auger recombination and *quantum* model for

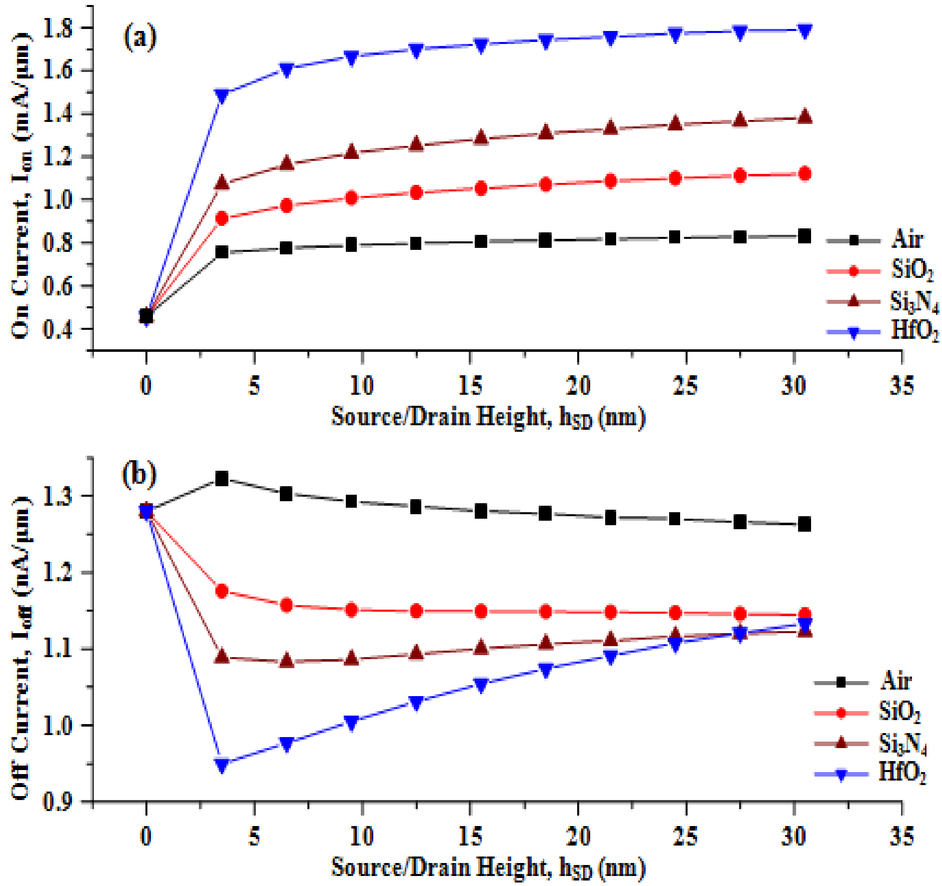

Fig 4.2: Drain current variations as a function of elevation height h_{SD} for the four side spacer dielectrics namely Air, SiO_2, Si_3N_4 and HfO_2: **(a)** On current versus h_{SD} plot for $V_{DS} = 1.0$ V and $V_{GS} = 1.0$ V ; **(b)** Off current versus h_{SD} plot for $V_{DS} = 1.0$ V and $V_{GS} = 0.0$ V.

including the quantum mechanical effects have been used in the ATLAS simulator for simulating the structure. The tungsten (work function $\varphi_M = 4.7$ eV) has been used as the gate-electrode for both the gates of the symmetric DG MOS device. Four different materials namely Air ($\varepsilon_r = 1$), SiO_2 ($\varepsilon_r = 3.9$), Si_3N_4 ($\varepsilon_r = 7.5$) and HfO_2 ($\varepsilon_r = 20$) as

the dielectric spacer between the gate and source/drain region have been explored in the present study to investigate their individual effects on the drivability of the MOS device with elevated source/drain structures. The height of the side spacer dielectric material is maintained to be same as that of the source/drain elevation height

4.3 Results and Discussion

The variations of I_{on} and I_{off} as a function of drain/source elevation h_{SD} $(0.0\text{ nm} \rightarrow 30.5\text{ nm})$ have been shown Fig 4.2 (a) and (b) for Air, SiO_2, Si_3N_4 and HfO_2 spacer dielectrics, respectively. The magnitude of I_{on} ($V_{GS} = 1.0V$ and $V_{DS} = 1.0V$) is observed to be increased, the I_{off} ($V_{GS} = 0.0V$ and $V_{DS} = 1.0V$) is decreased with the increase in spacer dielectric permittivity. While the increase in I_{on} with the h_{SD} is attributed to the reduction in the parasitic drain/source resistance (Shenoy *et al.* 2003), the increase in I_{on} with the increased permittivity of the spacer dielectric is believed to be resulted from the enhancement of electric field coupling from the gate to the channel through the higher permittivity dielectric spacer material. Although, the common trend of increase in I_{on} with increase in h_{SD} for all four spacer dielectrics is observed in the above figures, however, dissimilar trends of I_{off} with increased h_{SD} are observed for different spacer dielectric materials. To investigate the above trends of I_{off}, we have the recombination rate and vertical electric field (E_Y) as a function channel position at the channel center for Air, SiO_2, Si_3N_4 and HfO_2 spacer dielectrics in Fig 4.3(a) and (b); 4.4(a) and (b), 4.5(a) and (b) and, 4.6 (a) and (b) respectively. The recombination rate and

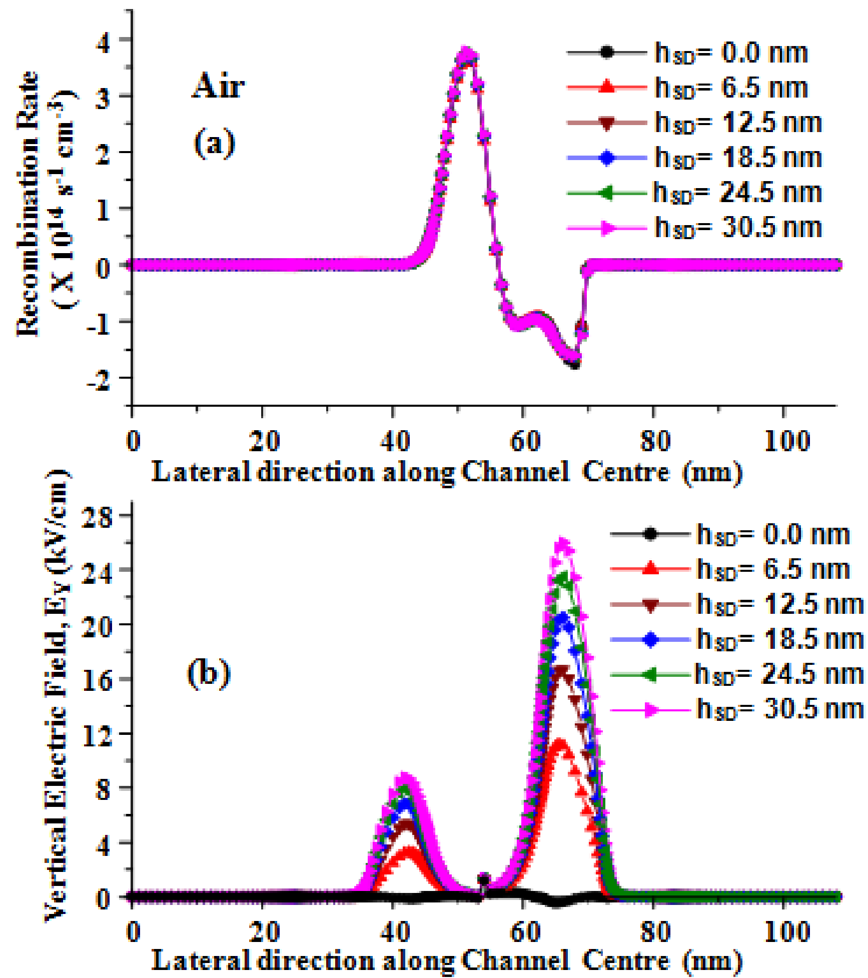

Fig 4.3 (a): Variation of recombination rate per unit volume along the channel for different values of h_{SD} with Air as the side dielectric spacer; **(b):** Vertical electric field, E_Y, along the lateral direction (x-axis) of channel center for different values of h_{SD} with Air side dielectric spacer as considered in (a).

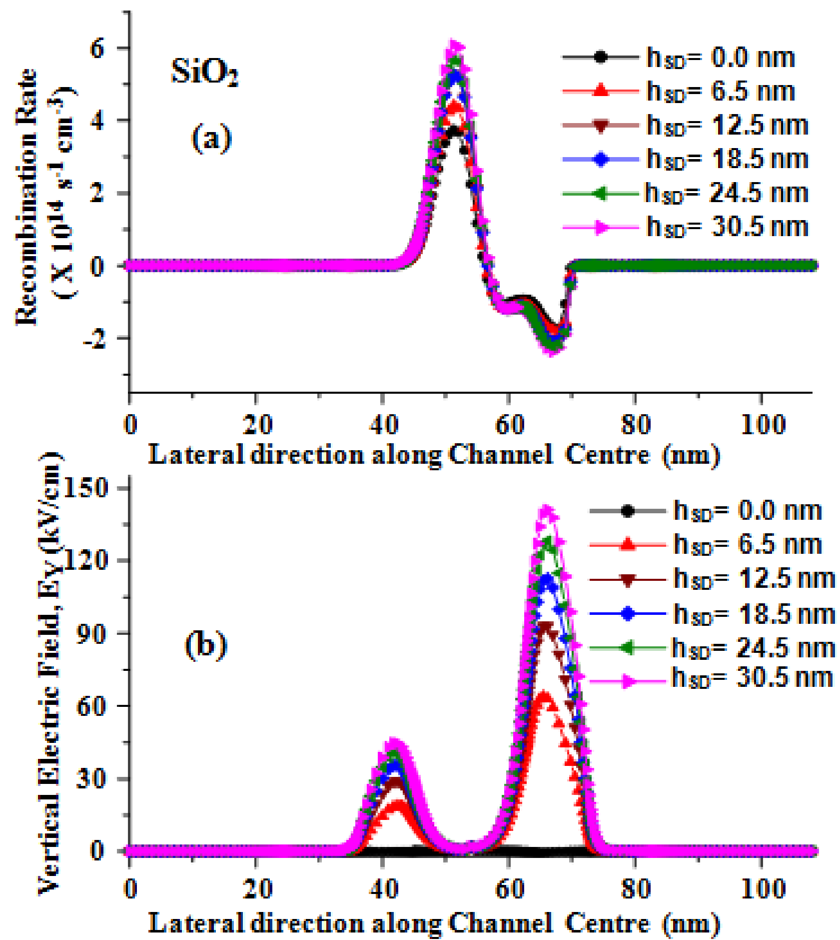

Fig 4.4(a): Variation of recombination rate per unit volume along the channel for different values of h_{SD} with SiO_2 as the side dielectric spacer; **(b):** Vertical electric field, E_Y, along the lateral direction (x-axis) of channel center for different values of h_{SD} with SiO_2sidedielectric spacer as considered in (a).

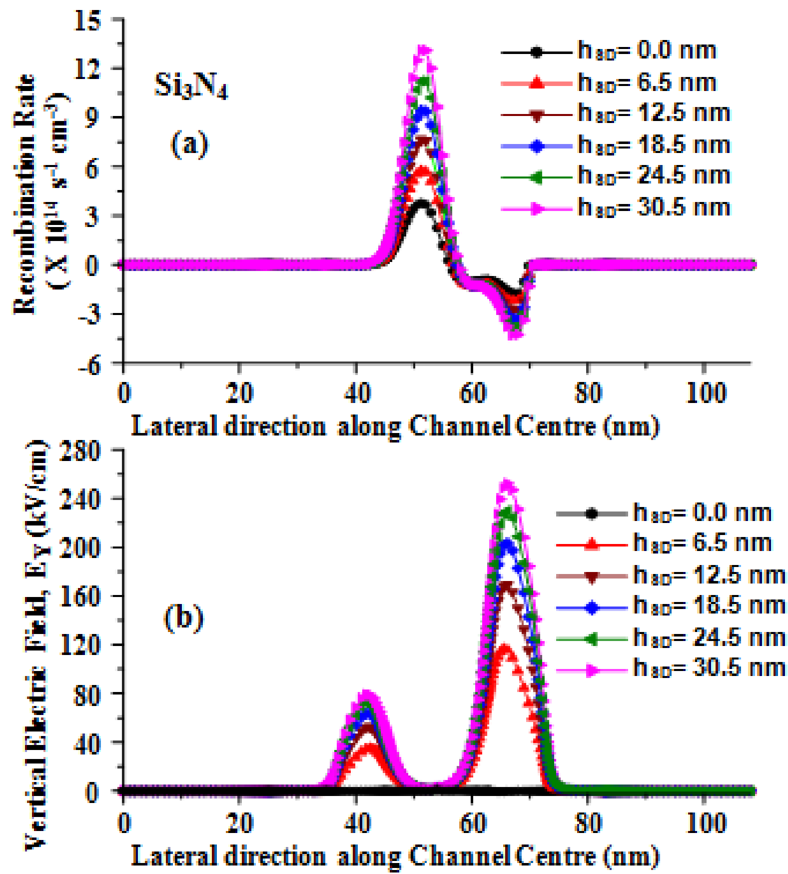

Fig 4.5(a): Variation of recombination rate per unit volume along the channel for different values of h_{SD} with Si_3N_4 as the side dielectric spacer; **(b):** Vertical electric field, E_Y, along the lateral direction (x-axis) of channel center for different values of h_{SD} with Si_3N_4 side dielectric spacer as considered in (a).

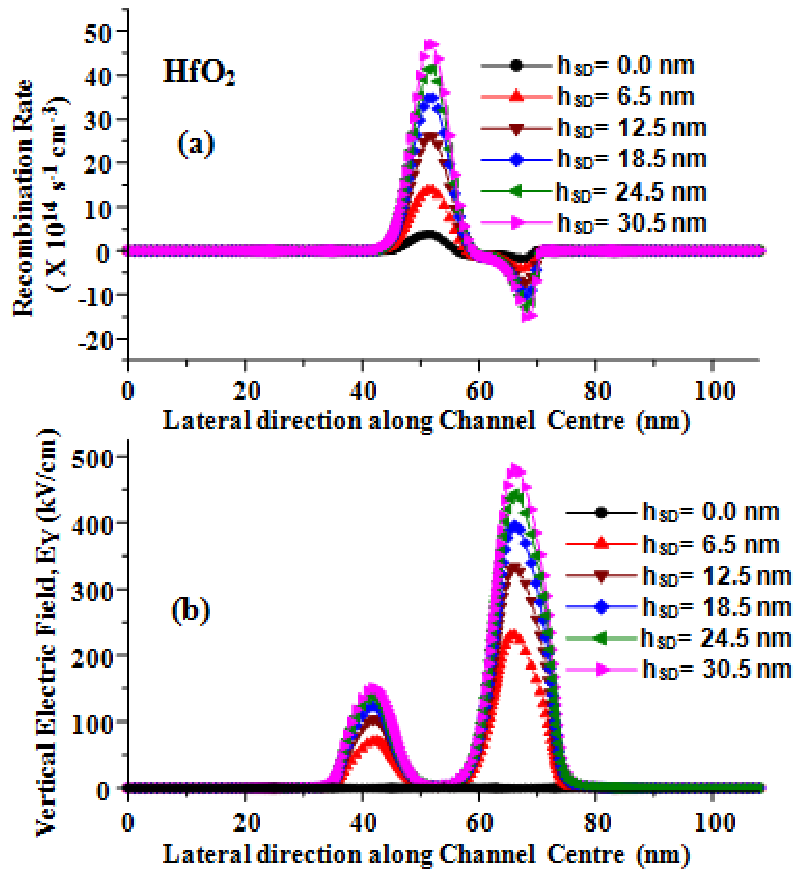

Fig 4.6(a): Variation of recombination rate per unit volume along the channel for different values of h_{SD} with HfO_2 as the side dielectric spacer; **(b):** Vertical electric field, E_Y, along the lateral direction (x-axis) of channel center for different values of h_{SD} with HfO_2 side dielectric spacer as considered in (a).

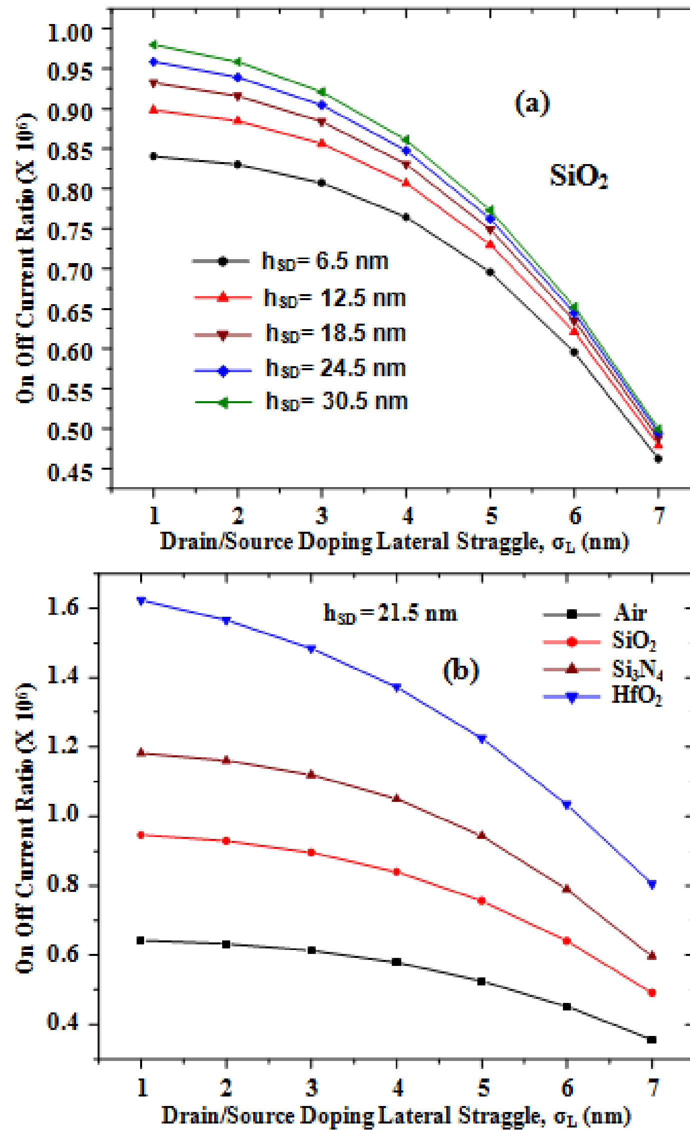

Fig 4.7(a): Drivability characteristics for SiO_2 spacer dielectric: I_{on}/I_{off} ratio versus the lateral straggle σ_L of the drain/source Gaussian doping profile for different h_{SD} values and **(b):** Variation of I_{on}/I_{off} ratio as a function of σ_L for different side spacer dielectric materials but with a fixed value of $h_{SD} = 2.15\text{nm}$.

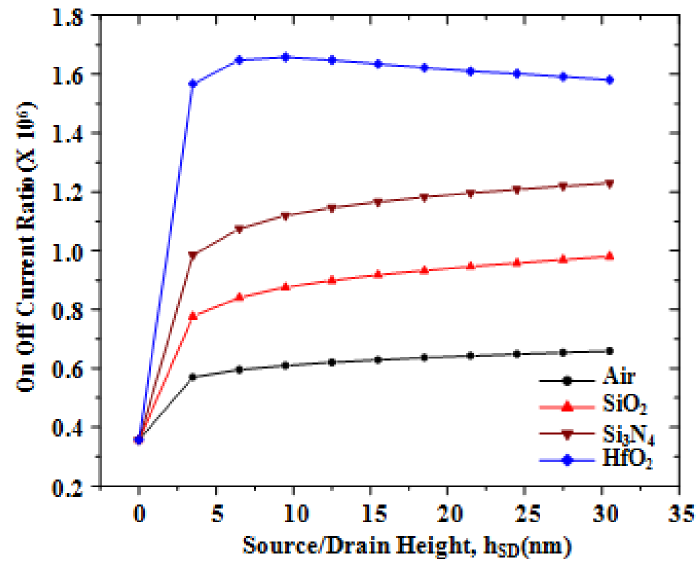

Fig 4.8: Variation of I_{on}/I_{off} ratio as a function of the drain/source elevation height h_{SD} for different side spacer dielectrics under study.

vertical electric field have been computed along the line $y=0$ for $V_{DS}=1.0V$ and $V_{GS}=0.0V$. The two peaks of vertical electric field at the source/channel and drain-channel junction are resulted from the crowding of electric field lines at the respective junctions due to the source/drain elevation. The amplitude of the vertical electrical fields is decreased to zero at the middle due to the symmetry of the device structure with respect to source and drain of the device under consideration. By comparing all the corresponding figures, it is observed that the negative recombination (i.e. generation) of carriers and vertical field E_Y are increased at the drain side with the increase in both h_{SD} and permittivity of the spacer dielectric. However, the negative recombination (i.e.

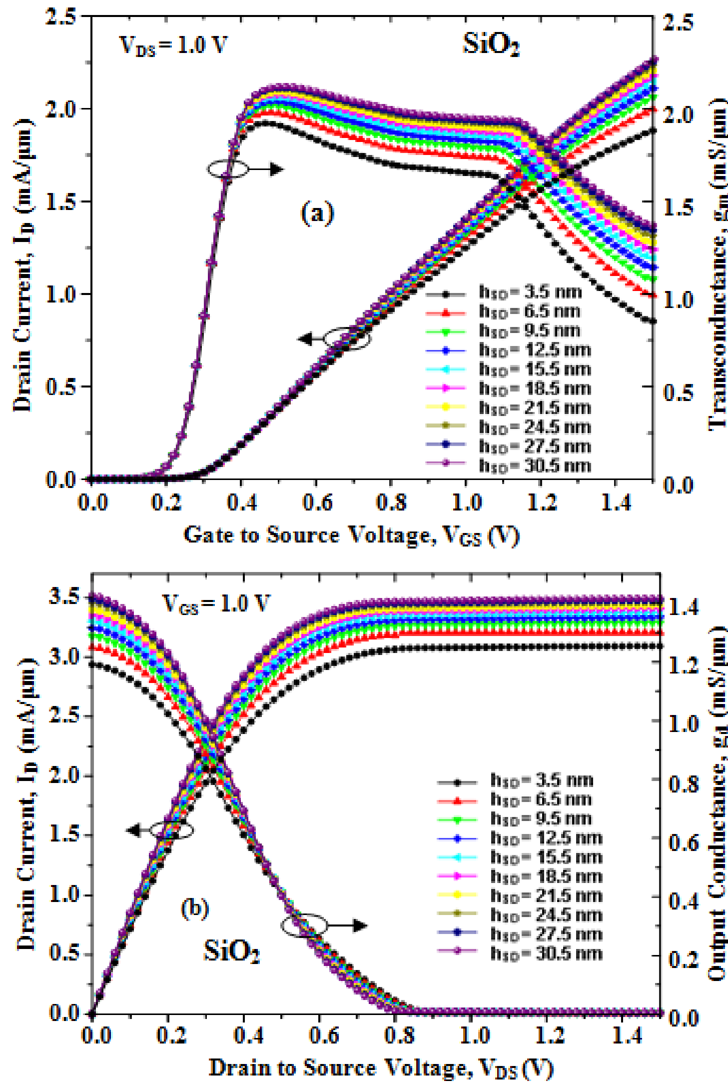

Fig 4.9 (a): Variations of drain current and transconductance with respect to the gate to source voltage for different h_{SD} values but for the fixed spacer dielectric SiO_2 and straggle parameter $\sigma_L = 4\,nm$; **(b):** Variations of drain current and output conductance due to the drain to source voltage for different h_{SD} values but for the fixed spacer dielectric SiO_2 and straggle parameter $\sigma_L = 4\,nm$ (both figure 4.9(a) and 4.9(b) uses same symbolic notation for different values of h_{SD}).

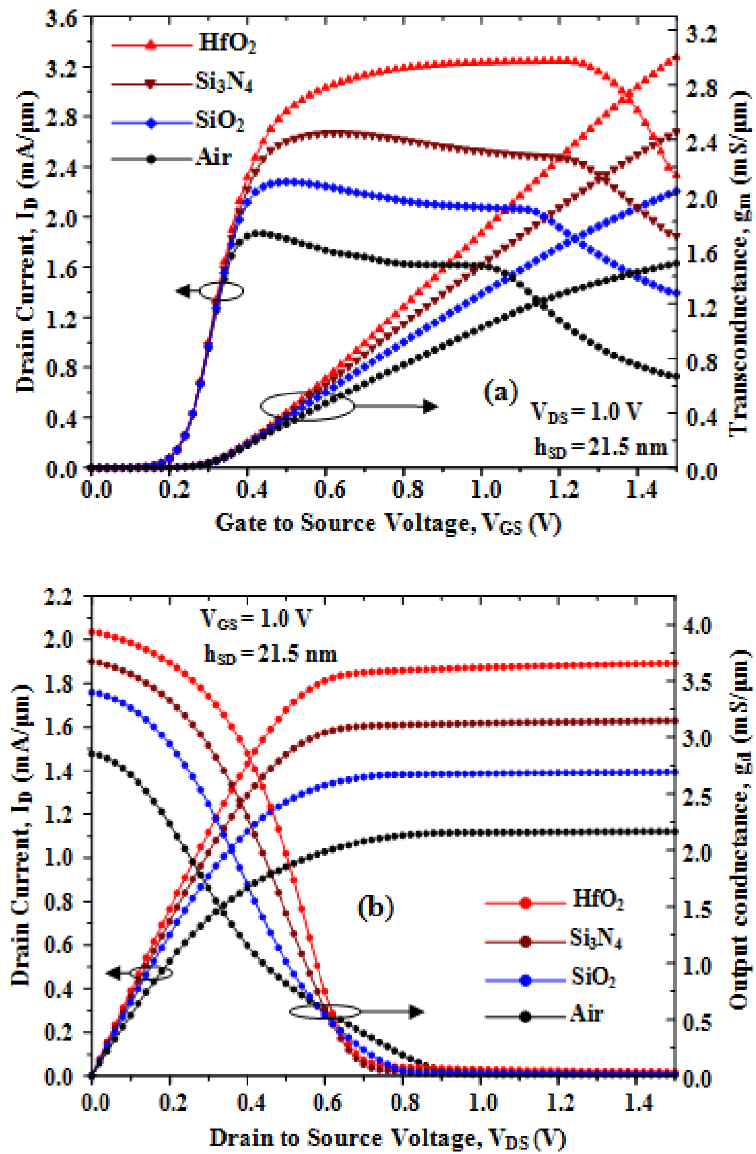

Fig 4.10 (a): Plots of drain current and transconductance as functions of the gate to source voltage for the four different side spacer dielectric materials namely Air, SiO_2, Si_3N_4 and HfO_2 and h_{SD} = 21.5 nm; (b): Variations of the drain current and output conductance due to the drain to source voltage for the four dielectric spacer materials Air, SiO_2, Si_3N_4 and HfO_2 with a fixed h_{SD} = 21.5 nm.

Table 4.1: (DG) Percentage change in I_{on}/I_{off} value at different h_{SD} w.r.t I_{on}/I_{off} value at h_{ref} ($h_{ref} = h_{SD} = 0$ nm). [$\%(I_{on}/I_{off}) = \frac{(I_{on}/I_{off})|_{h_{SD}} - (I_{on}/I_{off})|_{h_{REF}}}{(I_{on}/I_{off})|_{h_{REF}}} X100$]

h_{SD} (.nm)	$\%(I_{on}/I_{off})$ at $\sigma_L = 1$ nm				$\%(I_{on}/I_{off})$ at $\sigma_L = 4$ nm				$\%(I_{on}/I_{off})$ at $\sigma_L = 7$ nm			
	Air	SiO_2	Si_3N_4	HfO_2	Air	SiO_2	Si_3N_4	HfO_2	Air	SiO_2	Si_3N_4	HfO_2
3.5	59.87	117.99	176.41	339.96	89.92	158.62	228.01	396.41	154.50	235.76	313.04	496.20
6.5	66.91	135.99	201.72	362.86	96.59	175.63	251.66	408.77	160.53	250.65	332.16	513.30
9.5	71.03	145.73	214.09	365.46	100.40	184.80	263.17	408.09	163.83	258.46	341.16	516.77
12.5	73.99	152.28	221.64	362.71	103.10	190.91	270.08	403.81	166.07	263.52	346.35	515.69
15.5	76.39	157.38	227.19	358.95	105.23	195.56	274.93	399.04	167.77	267.25	349.85	513.38
18.5	78.47	161.75	231.79	355.35	107.03	199.40	278.74	394.67	169.14	270.25	352.52	510.94
21.5	80.33	165.64	235.80	352.06	108.59	202.72	281.92	390.81	170.28	272.76	354.69	508.65
24.5	81.87	169.14	239.26	349.79	109.80	205.53	284.84	388.39	171.26	275.29	357.28	507.48
27.5	83.42	172.30	242.39	346.81	111.04	208.12	287.16	385.13	172.10	277.17	358.81	505.37
30.5	84.84	175.15	245.11	343.82	112.15	210.42	289.11	381.99	172.83	277.17	360.09	503.26

generation) and E_Y are much smaller for the Air and SiO_2 dielectric spacers than those obtained for the Si_3N_4 and HfO_2 materials with higher permittivities. The increase in the vertical electric field E_Y with increased permittivity of the spacer dielectric increases the generation of carriers at the drain side which, in turn, increases the gate-induced drain leakage (GIDL) current (Y. Taur and T. H. Ning 1998) of the device. Since the GIDL current is very small for the Air and SiO_2 spacer dielectrics, the decrease in I_{off} with the increased h_{SD} in Fig 4.2(a) and (b) are mainly attributed to the decrease in the band-to-band tunneling (Zhang *et al.* 2003) with the elevation height. However, the increase in I_{off} due to GIDL becomes the dominant phenomena over the reduction in I_{off} due to band-to-band for higher spacer dielectric materials beyond a certain value of h_{SD}. As a consequence, while the resultant I_{off} current is initially decreased with increased h_{SD} for smaller values of h_{SD} mainly due to the dominant band-to-band tunneling (but negligible GIDL current), it starts to increase beyond a certain value of h_{SD} due to the dominant GIDL current (but negligible band-to-tunneling current) for Si_3N_4 and HfO_2 spacer

dielectrics as observed from Fig. 4.2(a) and 4.2(b) respectively. Although, the reason for the initial increase of I_{off} in Fig 4.2(b) is not clearly known for the Air spacer dielectric, but, it may be possibly due to the extremely poor gate-to-drain coupling of the electric field owing to negligible spacer capacitance between the gate and drain for $h_{SD} < 3.5$ nm . The plot of I_{on}/I_{off} ratio versus σ_L for different h_{SD} values but fixed spacer dielectric as SiO_2 has been shown in Fig 4.7(a) while the same for fixed $h_{SD} = 21.5$ nm but for different spacer dielectric has been shown in Fig 4.7(b).It is important to note that although the on-state current is increased with σ_L (not shown the figure) as reported by other researchers (Saitoh *et al.* 2011), (Nandi, Saxena, and Dasgupta 2013) but the resultant I_{on}/I_{off} ratio is decreased with increased $\sigma_L = 1$ nm . On the other hand, the result of Fig 4.7(b) confirms that the I_{on}/I_{off} ratio is increased with the permittivity of the spacer dielectric. Fig 4.8 shows the I_{on}/I_{off} ratio versus h_{SD} plots for different spacer dielectrics but fixed $\sigma_L = 1$ nm . The percentage variation of I_{on}/I_{off} ratio with respect to the I_{on}/I_{off} ratio at $h_{SD} = 0.0$ nm has been studied and listed in Table 4.1 for different values of h_{SD}, σ_L ($\sigma_L = 1$ nm, 2 nm, 7 nm) and side spacer ($\varepsilon_r = 1$, 3.9, 7.5, 20). Note that the percentage of I_{on}/I_{off} is increased for Air, SiO_2 and Si_3N_4 for all values of σ_L, it is increased with h_{SD} to a certain value and further increase in h_{SD} decreases the % ratio for HfO_2 spacer dielectric due to the dominant GIDL phenomena discussed earlier. In case of SiO_2 side spacer dielectric, I_{on} is increased by ~146% whereas I_{off} is reduced only by ~10%, which can cause a net increase in the I_{on}/I_{off} ratio by ~175% for a fixed

$\sigma_L = 1\,nm$ and $h_{SD} = 30.5$ nm . The maximum I_{on}/I_{off} ratio has been changed from~175% to ~277% when σ_L is increased from 1nm to 7nm due to the increase in I_{on} by ~203% and decrease in I_{off} by 11%. However, the maximum value of $I_{on}/I_{off} = 8.6\times10^5$ with a percentage increase of ~210% is observed for $\sigma_L = 4\,nm$. The maximum I_{on}/I_{off} ratios for Air, Si_3N_4 and HfO_2 as spacer dielectrics observed to be 6.6 x 10^5 at $\sigma_L = 1\,nm$ and $h_{SD} = 30.5\,nm$; 1.23 x 10^6 at $\sigma_L = 1\,nm$ and $h_{SD} = 30.5\,nm$; and 1.65 x 10^6 at $\sigma_L = 1\,nm$ and $h_{SD} = 9.5\,nm$ respectively. On the other hand, the maximum % I_{on}/I_{off} are observed as ~516 % for HfO_2 at $h_{SD} = 9.5\,nm$, ~360% for Si_3N_4 at $h_{SD} = 30.5\,nm$ and ~172% for Air at $h_{SD} = 30.5\,nm$ as compared to ~277 % for SiO_2 at $h_{SD} = 30.5\,nm$) of each structure at $\sigma_L = 7\,nm$. The drain current I_{DS} versus gate voltage (V_{GS}) [Left] and Transconductance (g_m) versus V_{GS} [Right] have been shown in Fig4.9(a) whereas the I_{DS} versus drain voltage (V_{DS}) [Left] and output conductance g_d [Right] versus the V_{DS} characteristics have been shown in Fig 4.9(b) for a fixed $\sigma_L = 4\,nm$ and fixed spacer dielectric SiO_2 but for different values of h_{SD}. It is observed that the magnitudes of I_{DS} , g_m and g_d are increased with the increase in the h_{SD} . Fig 4.10(a) shows I_{DS} Vs. V_{GS} [Left] and g_m Vs. V_{GS} [Right] graphs while the I_{DS} Vs. V_{DS} [Left] and g_d Vs. V_{DS} [Right] characteristics have been shown in Fig 4.10(b) for fixed values of $\sigma_L = 4\,nm$ and $h_{SD} = 21.5$ nm but for different spacer dielectrics. It is clear from Fig4.10 that the magnitudes of I_{DS} , g_m and g_d are increased with the increase in dielectric permittivity of the spacer.

4.4 Conclusion

A detailed TCAD based simulation study for investigating the effects of S/D elevation height h_{SD} and four different dielectric spacers (namely Air, SiO_2, Si_3N_4 and HfO_2 in the gate and S/D regions) on the drivability, transconductance and output conductance of USJ GU DG MOSFET have been reported in this chapter. It is observed that the I_{on}/I_{off} ratio of the device can be significantly improved by increasing h_{SD} and permittivity of the spacer dielectric material. While the I_{off} is reduced with increased h_{SD} by the band-to-band tunneling for lower permittivity spacer dielectrics Air and SiO_2, it is increased significantly for higher permittivity spacer dielectrics Si_3N_4 and HfO_2 due to the dominance of the GIDL phenomena over the band-to-band tunneling. Among the four spacer dielectrics under study, increase in I_{on} and decrease in I_{off} is only observed for the entire increased values of h_{SD} in case of SiO_2 spacer dielectric confirms that band-to-band tunneling is the dominant phenomena for all values of h_{SD}. However, both the I_{on} and I_{on}/I_{off} ratio are improved by using higher permittivity spacer dielectrics. Further, while I_{on} is increased with the straggle parameter σ_L of the Gaussian profile in the S/D region, the overall I_{on}/I_{off} ratio is decreased with increased σ_L . Moreover, the transconductance and output conductance characteristics are also improved with the increased value of h_{SD} for different spacer dielectric materials. In brief, the elevation height of the S/D regions, permittivity of the side spacer dielectric and σ_L can be explored as additional parameters for optimizing the drivability as well as other

performance parameters of the sub-20nm non-abrupt GU DG MOSFETs structure under consideration.