Chapter 3

Subthreshold Current and Swing Modeling of Gate Underlap DG MOSFETs with Source/Drain Lateral Gaussian Doping Profile

3.1 Introduction.

The subthreshold current presents the drain current even when the device is under OFF-state condition causing static power loss of any MOS transistors in both the analog and digital circuit applications. On the other hand, the subthreshold swing (SS) parameter represents the switching characteristics of the MOS transistors in digital circuit applications. Thus, it is very important to investigate subthreshold current and subthreshold swing characteristics of any MOS transistor to understand the static power loss and switching performance of the device for VLSI circuit applications. In view of the above, after studying the channel potential and threshold voltage characteristics in Chapter 2, we have devoted this Chapter to develop the analytical models for investigating the subthreshold current and subthreshold swing characteristics of the USJ gate- underlap DG MOSFETs with a lateral Gaussian doping profile in the source/drain region already considered in Chapter 2. The subthreshold current under each of the two gates have been summed to model the total drain current under subthreshold regime of operation of the device. Then subthreshold swing characteristics have been modeled by using the concept of effective conduction path following the methods described in refs.

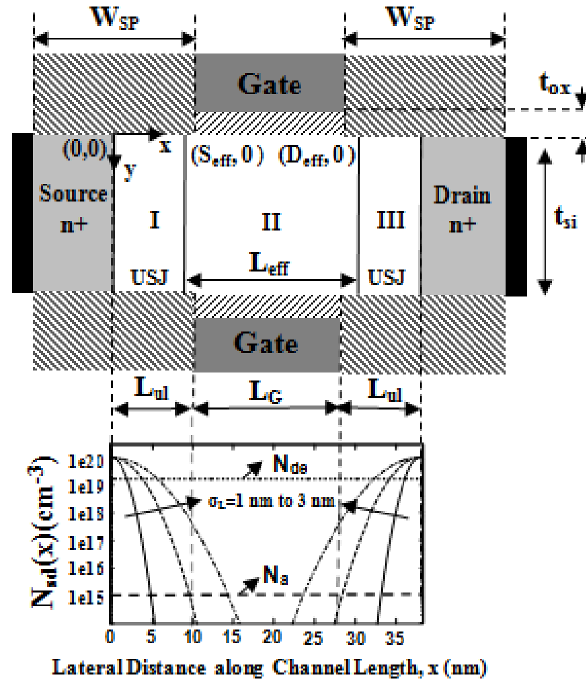

Fig 3.1: Schematic view of underlap USJ DG MOSFET.

(Dubey *et al.* 2011). Since the present work is in continuation to our earlier work reported in chapter 2, we will use all the device parameters with same nomenclatures as defined in Chapter 2 for developing models for the subthreshold current and subthreshold swing in this chapter. Some of the results of Chapter 2 will also be directly used in this chapter. The outline of the present Chapter is given below.

In Sec. 3.2, we have used the results of channel potential of IInd region (i.e. the gate overlap region) derived in section 2.2 has been used to model the subthreshold current of the device. The expression for the subthreshold swing of the device under study has been derived in Sec. 3.3 by using the effective conduction path concept. Section 3.4 presents

the model results along with their comparison with the ATLAS™ TCAD simulation for checking the validity of our proposed models. Finally, the summary and conclusion of the chapter have been described in Sec.3.5.

3.2 Analytical Formulation of Subthreshold current model

Fig 3.1 shows the schematic diagram of the gate-underlap DG MOSFET structure under consideration. Although, the device structure under study is same as that considered in Chapter 2, but we have reproduced the schematic structure in Fig. 3.1 for the better clarity of understanding of the work carried out in this chapter. The total channel region $0 \le y \le t_{si}$ in the vertical direction is divided into two regions namely the front and back regions under the control of the front gate and back gate respectively as shown in Fig.3.1. The total subthreshold current in the channel can be obtained by summing the currents of the individual regions under each of the gate which are modeled as follows.

Assuming that the diffusion is the dominant phenomena for the subthreshold current flow mechanism in the MOS device, the subthreshold current of the DG MOSFETs under study can be given as (Dubey *et al.* 2011).

$$I_S = \int_0^{t_{si}} qD_n \frac{n_{min}(y)}{L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) dy \qquad (3.1)$$

where D_n is diffusion constant, L_{eff} the effective channel length, V_{DS} the drain to source voltage, V_T the thermal voltage and

$$n_{min}(y) = \frac{n_i^2}{N_a}\exp\left(\frac{\psi_{VC}(y)}{V_T}\right) \tag{3.2}$$

$$\psi_{VC}(y) = \psi_{s2}(x_{min})\left[1 + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}y - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}}y^2\right] + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}(V_{GS} - V_{fb})\left[-y + \frac{y^2}{t_{si}}\right] \tag{3.3}$$

where $x_{min} = L_{ul} + (\lambda/2)\ln((D/C)_{max})$ represents the location at which $\psi_{c2}(x)$ has the minimum value (i.e. x_{min} is obtained by solving $\left.\frac{\partial\psi_{c2}(x)}{\partial x}\right|_{x=x_{min}} = 0$ as discussed in Chapter 2), and $n_{min}(y)$ is the carrier concentration at the virtual cathode. The virtual cathode is defined as a hypothetical electrode placed at $x = x_{min}$ along the vertical direction of the channel with potential distribution of $\psi_{VC}(y)$ and a carrier distribution of $n_{min}(y)$ from which carriers are assumed to be emitted by the thermionic emission phenomena to constitute the subthreshold drain current of a MOS transistor (Dubey *et al.* 2010). Since the minimum potential of the virtual cathode represents the maximum energy barrier for the electrons, the carriers emitted from the source by thermionic emission are required to overcome this maximum energy barrier to contribute the drain current under subthreshold regime of operation of the device. Thus the position of the minimum potential plays a significant role in modeling the subthreshold current. Assuming that $y = y_{min}$ represents the location of the minimum potential, say $\psi_{VC}(y_{min}) = \psi_{VC}(y)|_{y=y_{min}}$, on the virtual cathode, y_{min} can be obtained by solving the following equation (Dubey *et al.* 2011):

$$\left.\frac{\partial\psi_{VC}(y)}{\partial y}\right|_{y=y_{min}} = 0 \tag{3.4}$$

Let the subthreshold currents contributed by the front and back channel regions be denoted by I_{Sf} and I_{Sb} respectively. Thus the total subthreshold current described by Eq. (1) can be expressed as

$$I_S = I_{Sf} + I_{Sb} \tag{3.5}$$

where,

$$I_{Sf} = \int_0^{y_{min}} qD_n \frac{n_{min}(y)}{L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) dy \tag{3.6}$$

And

$$I_{Sb} = \int_{y_{min}}^{t_{si}} qD_n \frac{n_{min}(y)}{L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) dy \tag{3.7}$$

Following the methodology described by Dubey *et al.*(Dubey *et al.* 2011) Eqns. (3.6) and (3.7) can be expressed as

$$I_{Sf} = K_f \left(\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(0)}{V_T}\right)\right) \tag{3.8}$$

and

$$I_{Sb} = K_b \left(\exp\left(\frac{\psi_{VC}(t_{si})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right)\right) \tag{3.9}$$

where,

$$K_f = \frac{qD_n n_i^2 V_T}{E_f N_a L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$

$$K_b = \frac{qD_n n_i^2 V_T}{E_b N_a L_{eff}} \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right)$$

$$E_f = \frac{\psi_{VC}(y_{min}) - \psi_{min}(0)}{y_{min} - 0}$$

$$E_b = \frac{\psi_{VC}(y_{min}) - \psi_{min}(t_{si})}{y_{min} - t_{si}}$$

where E_f and E_b are the respective electric fields associated with the front and back surfaces of the underlap USJ DG MOSFET structure under consideration.

3.3 Analytical formulation of subthreshold swing model

The subthreshold swing (S) can be defined as

$$S = \left(\frac{\partial \log I_S}{\partial V_{GS}}\right)^{-1} \tag{3.13}$$

where, I_S is the subthreshold current of the underlap USJ DG MOSFET under study. Since the subthreshold current I_S is mainly due to the diffusion phenomenon, it can be assumed to be proportional to the carrier concentration $n_{min}(y)$ at the virtual cathode, and hence I_S can be expressed as (Dey *et al.* 2008).

$$I_S \propto n_{min}(y) \propto \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) \tag{3.14}$$

Using Eq. (3.14) in Eq. (3.13), we can express S as

$$S = V_T(\ln 10) \times \left(\frac{\partial \psi_{VC}(y)}{\partial V_{GS}}\right)^{-1} \tag{3.15}$$

Equation (3.15) shows that the subthreshold swing is a function of *y* which is undesirable since S is a position independent device parameter. In order to make "S" independent of *y*, we can use the concept of effective conduction path proposed by Dey *et al.* (Dey *et*

al. 2008) According to this concept, the subthreshold currents I_{fs} and I_{bs} are assumed to flow at fixed distances measured from the respective channel/oxide interfaces of the front and back channel regions. Assuming that $d_{eff,A}$ and $d_{eff,B}$ are the effective conduction path parameters (Dubey *et al.* 2011) of the front and back regions of the channel (see Fig. 3.1), we may write

$$d_{eff,A} = \frac{\int_0^{y_{min}} y \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy}{\int_0^{y_{min}} \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy} = \frac{\left(y_{min} - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right) - \left(0 - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(0)}{V_T}\right)}{\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(0)}{V_T}\right)} \tag{3.16}$$

$$d_{eff,B} = \frac{\int_{y_{min}}^{t_{si}} y \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy}{\int_{x_{min}}^{t_{si}} \exp\left(\frac{\psi_{VC}(y)}{V_T}\right) dy} = \frac{\left(t_{si} - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(t_{si})}{V_T}\right) - \left(y_{min} - \frac{V_T}{E_f}\right)\exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right)}{\exp\left(\frac{\psi_{VC}(t_{si})}{V_T}\right) - \exp\left(\frac{\psi_{VC}(y_{min})}{V_T}\right)} \tag{3.17}$$

Now assuming that the resultant current of the entire channel flows at a distance $y = d_{eff}$ (i.e. measured from the front channel/oxide interface), we may write the effective conduction path parameter for the entire device under consideration as:

$$d_{eff} = \frac{I_{Sf}\left|d_{eff,A}\right| + I_{Sb}\left|d_{eff,B}\right|}{I_S} \tag{3.18}$$

Using $y = d_{eff}$ in Eq. (3.15), can now model the subthreshold swing as

$$S = \frac{V_T \ln 10}{\left(\left(\frac{c_1(e_1+f_1)}{d_1}\right)+1\right)b_1 + a_1} \tag{3.19}$$

where,

$$a_1 = \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left[-d_{eff} + \frac{d_{eff}^2}{t_{si}}\right]$$

$$b_1 = \left\{1 - \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left[-d_{eff} + \frac{d_{eff}^2}{t_{si}}\right]\right\}$$

$$c_1 = \frac{1}{\sqrt{C_{min}D_{min}}}$$

$$d_1 = \frac{4t_{ox}gh}{\eta\lambda}\cosh\left(\frac{L_G}{\lambda}\right) + 2\left(g^2 + \left(\frac{t_{ox}h}{\eta\lambda}\right)^2\right)\sinh\left(\frac{L_G}{\lambda}\right)$$

$$e_1 = D_{min}\left(g\left(e^{-L_G/\lambda} - 1\right) - \frac{t_{ox}h}{\eta\lambda}\left(e^{-L_G/\lambda} + 1\right)\right)$$

$$f_1 = C_{min}\left(g\left(1 - e^{L_G/\lambda}\right) - \frac{t_{ox}h}{\eta\lambda}\left(e^{L_G/\lambda} + 1\right)\right)$$

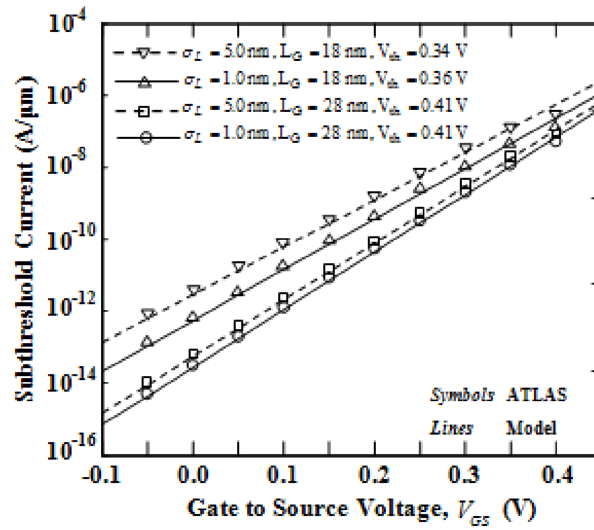

Fig 3.2: Subthreshold Current vs. Gate to Source Voltage. Parameters used: $V_{DS} = 0.05$ V, $L_{ul} = 10$ nm, $t_{si} = 7$ nm, $t_{ox} = 1$ nm.

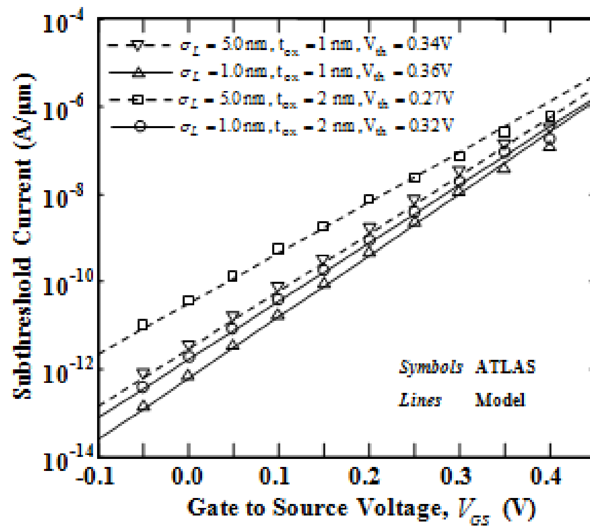

Fig 3.3: Subthreshold Current vs. Gate to Source Voltage. Parameters used: $V_{DS} = 0.05$ V, $L_G = 18$ nm, $L_{ul} = 10$ nm, $t_{si} = 7$ nm.

3.4 Results and Discussion

In this section, we have presented some of model results of the subthreshold current (I_S) and subthreshold swing (S) of the underlap DG MOSFETs with a lateral Gaussian doped source/drain region. The results have also been compared with the numerical simulation results obtained by the 2D device simulation software ATLAS^{TM} for verifying the validity of our proposed models. The drift-diffusion (DD) model and Fermi-Dirac statistics have been used for the carrier transport and carrier distribution in the ATLAS simulation. The results have been presented for identical front and back gate structures with the same gate-oxide thicknesses and tungsten (work function $\phi_M = 4.7$ eV) as the gate material for both of the gates of the device. The threshold voltage used in the modeling of the subthreshold current has been calculated from Eq. (2.43) of Chapter 2.

Subthreshold Current: The variations of the subthreshold current as a function of gate to source voltage for three different combinations of σ_L and L_G; σ_L and t_{ox} and σ_L and t_{si} (while keeping the underlap length (L_{ul}) and other parameters constant) have been shown in Fig.3.2, Fig. 3.3 and Fig. 3.4 respectively. It is observed that the subthreshold current is increased with σ_L when other parameters remain unchanged. The increased σ_L reduces the effective channel length of the device which, in turn, increases the subthreshold current. Further, for a fixed value of σ_L, the subthreshold current is increased with the decreased channel length, increased oxide thickness and increased channel thickness due to increased SCEs as observed in Fig.3.2, Fig 3.3 and Fig 3.4 respectively. It is demonstrated in our previous work (chapter 2) that the threshold

voltage of the device is decreased with the decrease in channel length, increase in channel thickness and increase in oxide thickness due to SCEs which, in turn, increases the subthreshold current of the device. From the results of Figs.3.2-3.4, it is observed that the straggle parameter σ_L can provide us an additional flexibility of controlling the subthreshold current of the device. The variations of subthreshold current as a function of the gate-underlap channel length (L_{ul}) for three different combinations of σ_L and L_G; σ_L and t_{ox} and, σ_L and t_{si} (while keeping other parameters constant) have been shown in Fig 3.5, Fig 3.6 and Fig 3.7 respectively. Subthreshold leakage current is observed to be decreased with the increase in the gate underlap region due to reduction in the SCEs. However, for fixed values of L_{ul} and σ_L, the subthreshold current is increased with decreased channel length, increased oxide thickness and increased channel thickness as demonstrated in Fig 3.5, Fig 3.6 and Fig 3.7 respectively. Similarly, it is increased with σ_L for a fixed L_{ul} and other device parameters as discussed earlier. It may be mention that the reduction in subthreshold current at the cost of increased L_{ul} must increase the overall size of the transistor under consideration. Note that our model results are observed to be in good agreement with the ATLAS^{TM} based TCAD simulation data thereby confirming the validity of our proposed model.

Subthreshold Swing: We will now discuss the subthreshold swing characteristics of the device under study. The variations of subthreshold swing as a function of the gate-underlap length ($\mathrm{L_{ul}}$) for three different combinations of σ_L and $\mathrm{L_G}$; σ_L and $\mathrm{t_{ox}}$ and, σ_L and $\mathrm{t_{si}}$ (while keeping other parameters constant) have been shown in Fig.3.8, Fig. 3.9

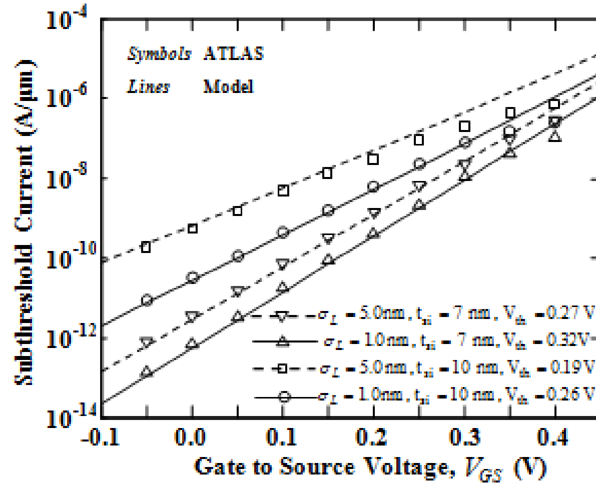

Fig 3.4: Subthreshold Current vs. Gate to Source Voltage. Parameters used: $V_{DS} = 0.05$ V , $L_G = 18\,\text{nm}$, $L_{ul} = 10\,\text{nm}$, $t_{si} = 7\,\text{nm}$.

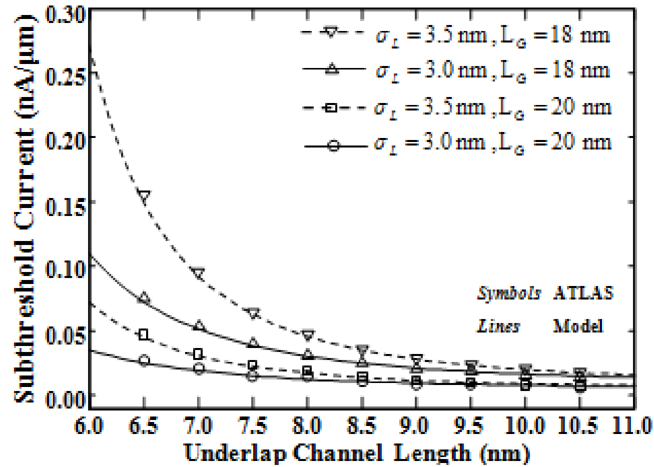

Fig 3.5: Subthreshold Current vs. Underlap Channel Length. Parameters used: $V_{DS} = 0.05$ V, $V_{GS} = 0.1$ V, $t_{si} = 7\,\text{nm}$, $t_{ox} = 1\,\text{nm}$.

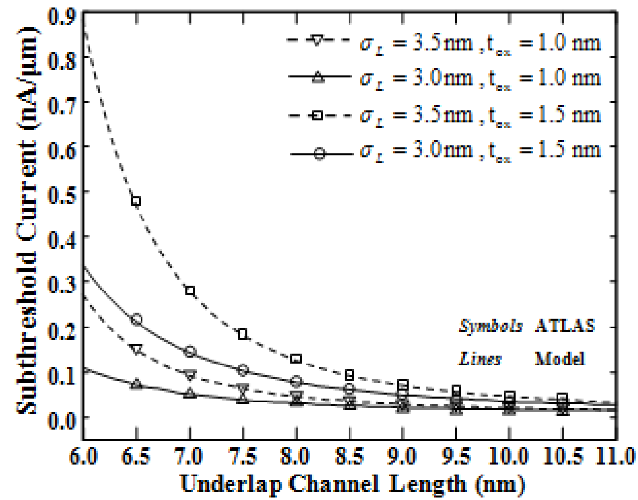

Fig 3.6: Subthreshold Current vs. Underlap Channel Length. Parameters used: $V_{DS} = 0.05$ V, $V_{GS} = 0.1$ V, $t_{si} = 7$ nm , $L_G = 18$ nm.

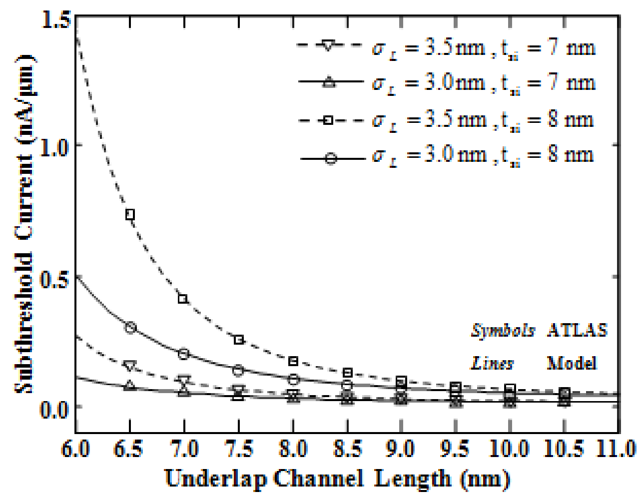

Fig 3.7: Subthreshold Current vs. Underlap Channel Length. Parameters used: $V_{DS} = 0.05$ V, $V_{GS} = 0.1$ V, $L_G = 18$ nm , $t_{ox} = 1$ nm.

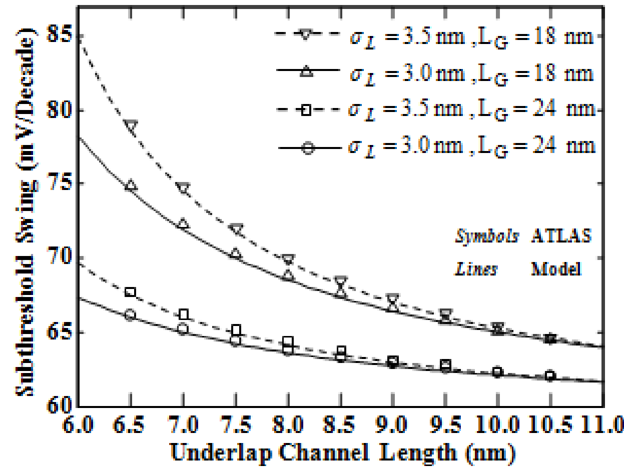

Fig 3.8: Subthreshold Swing vs. Underlap Channel Length. Parameters used: $V_{DS} = 0.05$ V, $t_{si} = 7$ nm, $t_{ox} = 1$ nm, $V_{GS} = 0.1$ V.

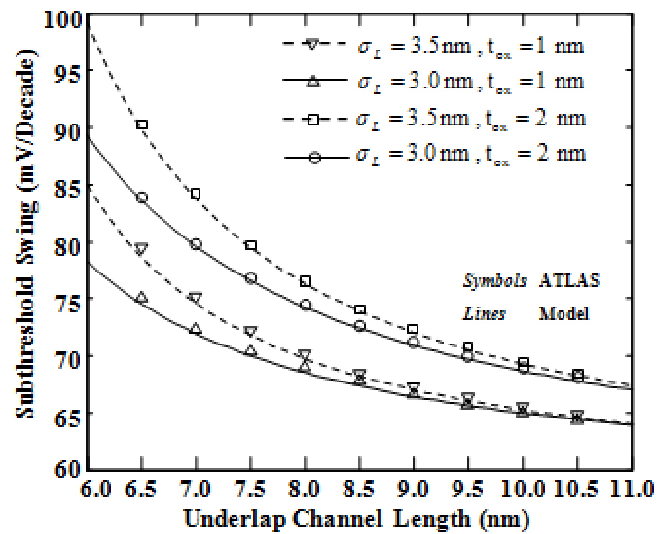

Fig 3.9: Subthreshold Swing vs. Underlap Channel Length. Parameters used: $V_{DS} = 0.05$ V, $t_{si} = 7$ nm, $V_{GS} = 0.1$ V, $L_G = 18$ nm.

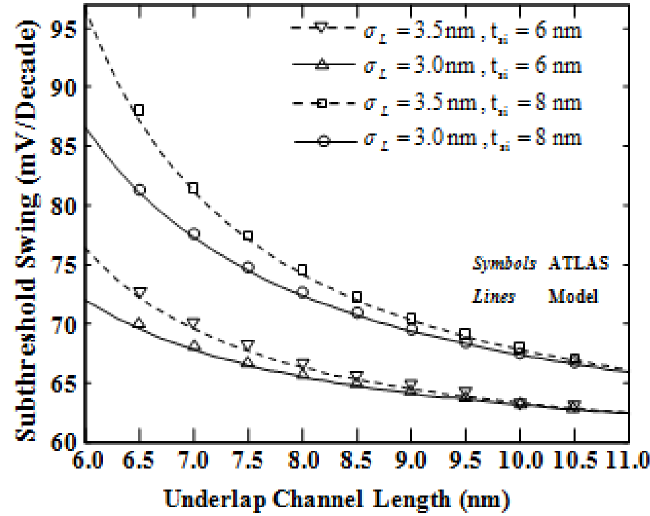

Fig 3.10: Subthreshold Swing Vs Underlap Channel Length. Parameters used: $V_{DS} = 0.05$ V, $t_{ox} = 1$ nm, $V_{GS} = 0.1$ V, $L_G = 18$ nm.

and Fig. 3.10 respectively. Like the subthreshold current, the subthreshold swing is increased also with σ_L. For fixed values of σ_L and L_{ul}, the swing also increases with the decreased channel length, increased oxide thickness and increased channel thickness due to increased SCEs as observed from Fig 3.8, Fig 3.9 and Fig 3.10 respectively. Like the subthreshold current, we also observe a reasonably good matching between our model results and TCAD simulation data for subthreshold swing characteristics of the device. The present study clearly shows that two parameters namely σ_L and L_{ul} can be used as additional parameters along with other device parameters for optimizing the subthreshold performance characteristics of the USJ gate-underlap DG MOSFETs under consideration.

3.5 Conclusion

Analytical models for the subthreshold current and subthreshold swing of the short-channel symmetric USJ gate-underlap DG MOSFETs with a lateral source/drain Gaussian doping profile have been proposed in this chapter. The results have been compared with ATLAS simulation data to validate the proposed model. Both the subthreshold current and subthreshold swing are observed to be dependent on the gate underlap length (L_{ul}) and straggle parameter (σ_L) of the source/drain Gaussian profile. The general trend of increased subthreshold current and subthreshold swing can be compensated by reducing σ_L and/or increasing L_{ul}. These two additional parameters thus provide better flexibility for optimization of the subthreshold current and swing characteristics of the device under study.