Chapter 2

Analytical Modeling of Potential Distribution and Threshold Voltage of Gate-underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile

2.1 Introduction

State-of-the-art of different types of source/drain engineering and their advantages have been reviewed in Chapter-1. It has been observed from Chapter-1 that gate-underlap can be explored to control the short channel effects (SCEs) in ultra-shallow junction DG MOSFETs. We have already discussed in the previous chapter that the combined benefits of improved immunity to SCEs (due to gate-underlap region) and enhanced on-state drive current (due to the introduction of a lateral Gaussian doping profile in the source/drain region) can be achieved by exploring both the ultra-shallow junction (USJ) and gate-underlap engineering in DG MOSFET structures (Trivedi *et al.* 2005), (Vaddi, Agarwal, and Dasgupta 2012), (Vaddi, Agarwal, and Dasgupta 2011). The literature survey presented in Chapter-1 also shows that, although some theoretical investigations have been reported on both the gate-underlap and gate-overlap DG MOSFET structures with uniform doping in the source and drain regions, however, no significant subthreshold characteristics of the USJ gate-underlap DG MOSFETs with a non-uniform doping profile in the source/drain (S/D) region. Thus, the present Chapter has been devoted for developing analytical models for the channel potential and threshold voltage of the USJ

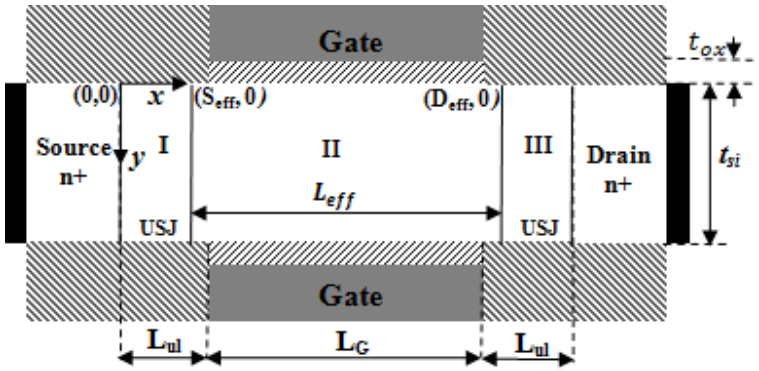

Fig 2.1(a): Schematic view of underlap DG MOSFET.

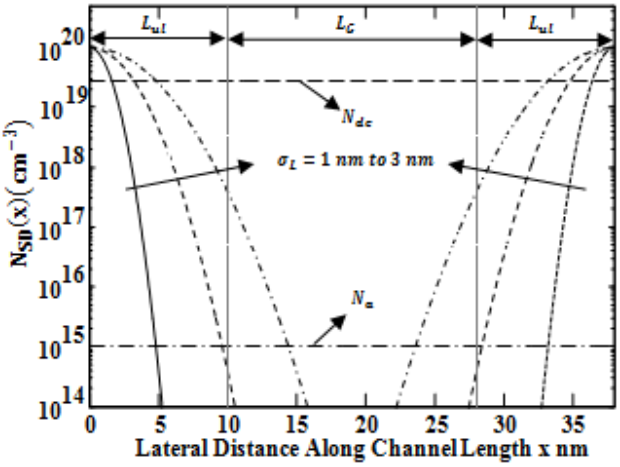

Fig 2.1(b): Lateral doping profile in the Source/Drain extension region for different values of straggle parameter.

gate-underlap DG MOSFETs with a lateral Gaussian profile in the source/drain region. The layout of the present chapter is as follows:

In Sec. 2.2, the 2-D potential distribution function in the channel region is obtained by solving the 2-D Poisson's equation using parabolic approximation and conformal mapping techniques. Sec. 2.3 deals with the modeling of the threshold voltage, DIBL and loss of switching speed with DIBL of the device. In Sec. 2.4, we have presented some

results and discussions related to the surface potential, threshold voltage, DIBL and loss in switching speed with DIBL of the short- channel gate-underlap USJ DG MOSFETs under study. Finally, the summary and conclusion of this chapter have been presented in Sec. 2.5.

2.2 Analytical Modeling of the 2-D Channel Potential

Fig 2.1(a) shows the schematic diagram of the gate-underlap DG MOSFET structure under consideration with the lateral Gaussian doping in the S/D region. The symbols L_G, L_{ul}, t_{si} and t_{ox} represent the gate length, underlap channel length, silicon film thickness and gate oxide thickness of the device respectively. The front and back gates are assumed to be tied together with a single gate-to-source voltage (V_{GS}). The doping profile, say $N_{sd}(x)$, in the S/D region of the device is the lateral Gaussian function expressed as Nandi *et al.* (Nandi, Saxena, and Dasgupta 2013):

$$N_{sd}(x) = N_{sdp} e^{\left(\frac{-x^2}{2\sigma_L^2}\right)} \tag{2.1}$$

where, N_{sdp} is the peak Gaussian doping.

Fig 2.1 (b) shows various lateral Gaussian profiles in the S/D region for different values of lateral straggle σ_L in the channel. The degenerated doping value N_{de} has been assumed as $\left(2.7\times10^{19}\,\mathrm{cm}^{-3}\right)$ (Nandi, Saxena, and Dasgupta 2013) for the present study.

Let us consider that $\psi_1(x,y)$, $\psi_2(x,y)$ and $\psi_3(x,y)$ are the 2-D potential functions in the regions I, II and III as shown in Fig 2.1(a). Now the generalized potential function

$\psi_i(x,y)$ for $i=1,2$ and 3 can be determined by solving the following 2D Poisson equation:

$$\frac{d^2\psi_i(x,y)}{dx^2}+\frac{d^2\psi_i(x,y)}{dy^2}=\frac{q}{\varepsilon_{si}}(N_a^- - N_{sd}^+(x)) \tag{2.2}$$

where, N_a^- is the ionized acceptor concentration and $N_{sd}^+(x)$ is the ionized donor concentration represented by (Nandi, Saxena, and Dasgupta 2013):

$$N_{sd}(x)=\left(\frac{N_{sdp}e^{\left(\frac{-x^2}{2\sigma_L^2}\right)}+N_{sdp}e^{\left(\frac{-(L_G+2L_{ul}-x)^2}{2\sigma_L^2}\right)}}{\left(1+s_D e^{\left(\frac{(E_F-E_D)}{kT}\right)}\right)}\right) \tag{2.3}$$

where, s_D is the spin degeneracy factor, E_F and E_D are the fermi level and donor level of the $N_{sd}(x)$ profile given by (Nandi, Saxena, and Dasgupta 2013).

$$E_F=\left(\frac{E_g}{2}\right)+kT\ln\left(\frac{N_{sd}(x)}{n_{i,eff}}\right) \tag{2.4}$$

$$E_D=E_{g,eff}-EI \tag{2.5}$$

$$EI=EI_o\left(1-\sqrt[3]{N_{sd}(x)/N_{de}}\right) \tag{2.6}$$

where, EI stands for ionization energy considering many body effects and, $n_{i,eff}$ and $E_{g,eff}$ are the effective intrinsic concentration and effective band-gap defined as (Nandi, Saxena, and Dasgupta 2013).

$$n_{i,eff}=\sqrt{n_i^2 e^{\frac{\Delta E_g}{kT}}} \tag{2.7}$$

$$E_{g,eff}=E_g-\Delta E_g \tag{2.8}$$

where, E_g, ΔE_g and n_i are the energy band-gap, band-gap narrowing and intrinsic carrier density of Si. By considering the parabolic approximation, the solution of Eq. (2.2), $\psi_i(x,y)$ can be expressed as (K Young 1989):

$$\psi_i(x,y) = C_{i1}(x) + C_{i2}(x)y + C_{i3}(x)y^2 \tag{2.9}$$

where, $C_{i1}(x)$, $C_{i2}(x)$ and $C_{i3}(x)$ are arbitrary functions of x (for all $i = 1,2$ and 3) which can be determined from the following boundary conditions:

$$\psi_i(x,0) = C_{i1}(x) \tag{2.10}$$

$$\psi_i(x,t_{si}) = C_{i1}(x) + C_{i2}(x)t_{si} + C_{i3}(x)t_{si}^2 \tag{2.11}$$

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=0} = C_{i2}(x) \tag{2.12}$$

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=tsi} = C_{i2}(x) + 2t_{si}C_{i3}(x) \tag{2.13}$$

Assuming $\psi_{si}(x) = \psi_i(x,y)|_{y=0}$ (for $i = 1,2$ and 3) as the surface potential, the criteria of the continuity of electric field at gate oxide–channel interface gives (Bansal and Roy 2007).

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{si}(x))}{t_{ox}} \tag{2.14}$$

$$\left.\frac{d\psi_i(x,y)}{dy}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{si}(x))}{t_{ox}} \tag{2.15}$$

where, ε_{si} and ε_{ox}, V_{GS} are the permittivity of the silicon and SiO_2, gate to source voltage respectively, and V_{fb} is the flat band voltage given by Bansal & Roy (Bansal and Roy 2007).

$$V_{fb} = \phi_M - \left(\chi_s + \frac{E_g}{2q} + \frac{kT}{q} \ln\left(\frac{N_a}{n_i} \right) \right) \tag{2.16}$$

where, ϕ_M, χ_s and E_g are the gate metal work function, electron affinity and band gap of the silicon, respectively.

By solving Eq. (2.11) with the help of boundary condition from Eqs. (2.12), (2.13), (2.14) and (2.15), we get

$$C_{i2}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\left(V_{GS} - V_{fb} - \psi_{s2}(x)\right)}{t_{ox}} \tag{2.17}$$

$$C_{i3}(x) = C_{i2}(x)/t_{si} = -\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{si}} \frac{\left(V_{GS} - V_{fb} - \psi_{s2}(x)\right)}{t_{ox}} \tag{2.18}$$

By rearranging Eq. 2 for region II with the help of Eqs. (2.10), (2.17) and (2.18), we obtain

$$\frac{d^2\psi_{2s}(x)}{dx^2} - \frac{\psi_{2s}(x)}{\lambda^2} = \frac{q}{\varepsilon_{si}}(N_a - N_{sd}^+(x)) - \frac{\left(V_{GS} - V_{fb}\right)}{\lambda^2} \tag{2.19}$$

where, $\lambda = \sqrt{\frac{\varepsilon_{si} t_{si} t_{ox}}{2\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{ox} t_{ox}} \right)}$ is the characteristic length associated with the surface potential of the channel. Solving Eq. (2.19), the surface potential for the gate overlapped channel region II is given as:

$$\psi_{s2}(x) = Ce^{(x - L_{il})/\lambda} + De^{-(x - L_{ul})/\lambda} - \frac{q\lambda^2\left(N_a - N_{SD}^+(x)\right)}{\varepsilon_{si}} + V_{GS} - V_{fb} \tag{2.20}$$

To model the fringing electric fields from gate to the gate-underlapped spacer regions I and III, we have used the conformal mapping technique by converting (x, y) to (u, v) plane by using the following transfer function (Bansal and Roy 2007):

$$-y + j\eta(L_{ul} - x) = t_{ox}\sin(u + jv) \tag{2.21}$$

where,

$$\eta = \frac{t_{ox}}{L_{ul}}\sinh\left(\cosh^{-1}\left(\frac{t_{ox} + t_g}{t_{ox}}\right)\right) \tag{2.22}$$

Now, from the continuity of the electric fields in all three regions in the (u, v) plane, we can write

$$\left.\frac{d\psi_i(u,v)}{dy}\right|_{u=o;\, i=1,3} = -\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{(V_{GS} - V_{fb} - \psi_{si}(v))}{n\pi/2} \tag{2.23}$$

where, n is such that $|\sin(n\pi/2)| = 1$.

Following the methodology of Bansal and Roy (Bansal and Roy 2007) for the conformal mapping technique, the surface potential functions in regions I and III from Eq. (2.2), Eq. (2.22) and Eq. (2.23) are given as:

$$\psi_{s1}(x) = A\left[1 - \frac{\alpha}{2}r_1^{\,2}\right] + B\left[r_1 - \frac{\alpha}{6}r_1^{\,3}\right] + V_{GS} - V_{fb} \tag{2.24}$$

$$\psi_{s3}(x) = E\left[1 - \frac{\alpha}{2}r_2^{\,2}\right] + F\left[r_2 - \frac{\alpha}{6}r_2^{\,3}\right] + V_{GS} - V_{fb} \tag{2.25}$$

where,

$$r_1 = \eta(L_{ul} - x)/t_{ox},\ r_2 = \eta(x - L_G - L_{ul})/t_{ox} \text{ and } \alpha = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{2}{t_{ox}t_{si}(m\pi/2)}\left(\frac{t_{ox}}{\eta}\right)^2$$

Constants A, B, C, D, E and F in Eq. (2.24), and (2.25) can be determined by applying the following boundary conditions:

$$\psi_{s1}(S_{eff}) = V_{bi} \tag{2.26}$$

$$\psi_{s1}(L_{ul}) = \psi_{s2}(L_{ul}) \tag{2.27}$$

$$\psi_{s2}(L_{ul} + L_G) = \psi_{s3}(L_{ul} + L_G) \tag{2.28}$$

$$\psi_{s3}(D_{eff}) = V_{bi} + V_{DS} \tag{2.29}$$

$$\left.\frac{d\psi_{s1}(x)}{dx}\right|_{x=L_{ul}} = \left.\frac{d\psi_{s2}(x)}{dx}\right|_{x=L_{ul}} \tag{2.30}$$

$$\left.\frac{d\psi_{s2}(x)}{dx}\right|_{x=L_G+L_{ul}} = \left.\frac{d\psi_{s3}(x)}{dx}\right|_{x=L_G+L_{ul}} \tag{2.31}$$

where, $S_{eff} = \sqrt{\ln\left(\frac{N_{de}}{N_{sdp}}\right) \times \left(-\sigma_L^2\right)}$ is defined as the distance at which the Gaussian doping profile in the source and drain region, and effectively reduced to the critical degenerated doping value N_{de} in the channel (Nandi, Saxena, and Dasgupta 2013) and

$D_{eff} = L_G + 2L_{ul} - S_{eff}$.

Now, the effective channel length is calculated as

$$L_{eff} = L_G + 2L_{ul} - 2 \times S_{eff} \tag{2.32}$$

Therefore, we can write

$$A = C + D - \frac{q\lambda^2\left(N_a - N_{sd}(x)\right)}{\varepsilon_{si}} \tag{2.33}$$

$$B = \frac{t_{ox}}{\eta\lambda}(D - C) \tag{2.34}$$

$$C = \left(\frac{g\left(V_{DS} + V_x\left(1 - e^{-L_G/\lambda}\right)\right) + \frac{t_{ox}H}{\eta\lambda}\left(V_{DS} + V_x\left(1 + e^{-L_G/\lambda}\right)\right)}{4\left(\frac{t_{ox}gH}{\eta\lambda}\right)\cosh\left(\frac{L_G}{\lambda}\right) + 2\left(g^2 + \left(\frac{t_{ox}H}{\eta\lambda}\right)^2\right)\sinh\left(\frac{L_G}{\lambda}\right)} \right) \tag{2.35}$$

$$D = \left(\frac{g\left(V_x\left(e^{L_G/\lambda} - 1\right) - V_{DS}\right) + \frac{t_{ox}H}{\eta\lambda}\left(V_{DS} + V_x\left(1 + e^{L_G/\lambda}\right)\right)}{4\left(\frac{t_{ox}gH}{\eta\lambda}\right)\cosh\left(\frac{L_G}{\lambda}\right) + 2\left(g^2 + \left(\frac{t_{ox}H}{\eta\lambda}\right)^2\right)\sinh\left(\frac{L_G}{\lambda}\right)} \right) \tag{2.36}$$

$$E = Ce^{L_G/\lambda} + De^{-L_G/\lambda} - \frac{q\lambda^2\left(N_a - N_{sd}(x)\right)}{\varepsilon_{si}} \tag{2.37}$$

$$F = \frac{t_{ox}}{\eta\lambda}\left(Ce^{L_G/\lambda} - De^{-L_G/\lambda}\right) \tag{2.38}$$

where,

$$g = 1 - \frac{\alpha}{2}\left(\frac{\eta L_{ul}}{t_{ox}}\right)^2$$

$$H = \frac{\eta L_{ul}}{t_{ox}} - \frac{\alpha}{6}\left(\frac{\eta L_{ul}}{t_{ox}}\right)^3$$

$$V_x = V_{bi} - V_{GS} + V_{fb} + g\frac{q\lambda^2\left(N_a - N_{sd}(x)\right)}{\varepsilon_{si}}$$

$$V_{bi} = V_T \ln\left(\frac{N_{de} \times N_a}{n_i^2}\right)$$

Finally, using the values of $C_{i1}(x) = \psi_i(x,0) = \psi_{s1}(x)$, $C_{i2}(x)$ and $C_{i2}(x)$ from their respective Eqs. (2.10), (2.17) and (2.18) in Eq. (2.2), the 2D potential function in the three regions of the channel can be written as

$$\psi_i(x,y)=\psi_{si}(x)\left[1+\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}y-\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}t_{si}}y^2\right]+\frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left(V_{GS}-V_{fb}\right)\left[-y+\frac{y^2}{t_{si}}\right] \quad (2.39)$$

2.3 Formulation of Threshold Voltage, DIBL and Loss of Switching Speed

By putting $y=t_{si}/2$in Eq. (2.39), the central channel potential for gate overlap region $\psi_{c2}(x)=\psi_2(x,y)\big|_{y=t_{si}/2}$ is given by

$$\psi_{c2}(x)=\psi_{s2}(x)\left[1+\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\right]-\frac{\varepsilon_{ox}t_{si}}{4\varepsilon_{si}t_{ox}}\left(V_{GS}-V_{fb}\right) \quad (2.40)$$

It is important to mention that position (x_{min}) of the minimum channel central potential plays the role of a virtual cathode from which electron enters into the channel to contribute the drive current. By solving $\left.\frac{\partial\psi_{c2}'(x)}{\partial x}\right|_{x=x_{min}}=0$, $x=x_{min}$ (at which $\psi_{c2}(x)$ has the minimum value) is

given as $x_{min}=L_{ul}+(\lambda/2)\ln\left((D/C)_{max}\right)$

Now, the threshold voltage can be defined as the gate voltage $V_{GS}=V_{th}$ at which the channel electron density at the minimum channel potential point reaches the channel doping density(Nandi, Saxena, and Dasgupta 2013). Hence, we write

$$\left(n_i^2/N_a\right)e^{(\psi_{c2}(x_{min})/V_T)}=N_a \quad (2.41)$$

where, V_T is the thermal voltage.

Now, solving Eq. (2.41) for $V_{GS} = V_{th}$, the final expression of the threshold voltage can be given by

$$V_{th} = V_{fb} + 2\phi - D_{max} e^{\frac{-x_{min}}{\lambda}} - C_{max} e^{\frac{x_{min}}{\lambda}} + \frac{\lambda^2 q\left(N_a - N_{SD}^{+}(x)\right)}{\varepsilon_{si}} - V(x_{min}) \tag{2.42}$$

To include the quantum mechanical effects, we have added the quantum correction factor ΔV_t^{QM} to the value of V_{th} described by Eq. (42) to obtain the final expression for the threshold voltage as

$$V_{thf} = V_{th} + \Delta V_t^{QM} \tag{2.43}$$

where,

$$\Delta V_t^{QM} = \frac{h^2}{8 q m_{eff} t_{si}^2}$$

where, h is Planck's constant, $m_{eff} = 0.19 m_o$ is the effective mass of electron with m_o as the mass of the electron in vacuum.

Now, the DIBL of the USJ underlap short-channel symmetric DG MOSFETs can be expressed as :

$$DIBL = \frac{V_{thf}\big|_{V_{DS}=0.1} - V_{thf}\big|_{V_{DS}=1.1}}{(V_{DS}=1.1) - (V_{DS}=0.1)} \tag{2.44}$$

It is important to mention that the DIBL severely affects the switching speed of the scaled CMOS devices. The loss of switching speed caused by the DIBL effect in the short-channel underlap DG MOSFETs under consideration can be expressed as (Ferain, Colinge, and Colinge 2011)

$$\left(\frac{\Delta f}{f}\right) = \frac{-2\,DIBL}{V_{DS} - V_{thf}} \tag{2.45}$$

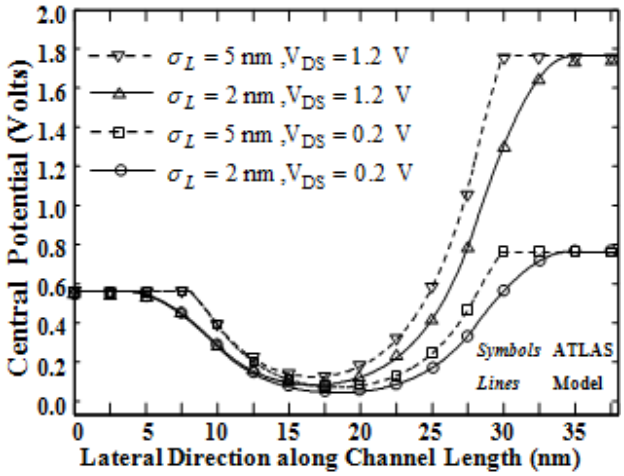

Fig 2.2: Central potential along channel length. Parameters used: $V_{GS} = 0.1\,V$, $L_G = 18nm, L_{ul} = 10nm, t_{si} = 7nm$, $t_{ox} = 1nm$.

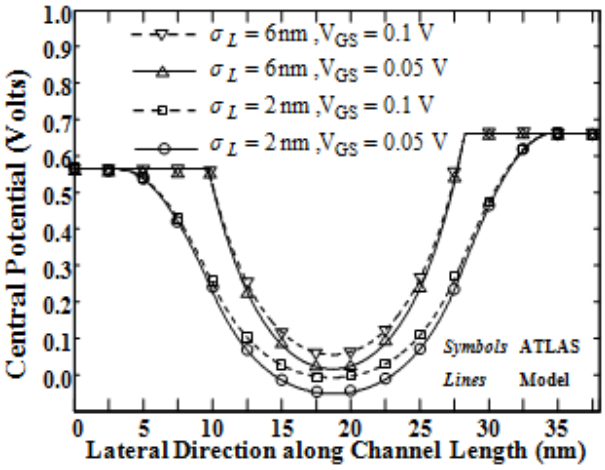

Fig 2.3: Central potential along channel length. Parameters used: $V_{DS} = 0.1V$, $L_G = 18nm, L_{ul} = 10nm$, $t_{ox} = 1nm$, $t_{si} = 7nm$.

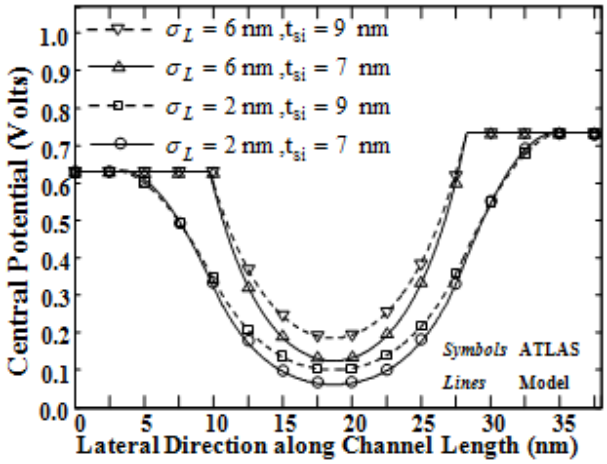

Fig 2.4: Central potential along channel length, Parameters used: $V_{GS} = 0.1\,V$, $L_G = 18\,nm$, $L_{ul} = 10\,nm$, $V_{GS} = 0.1\,V$, $t_{ox} = 1\,nm$.

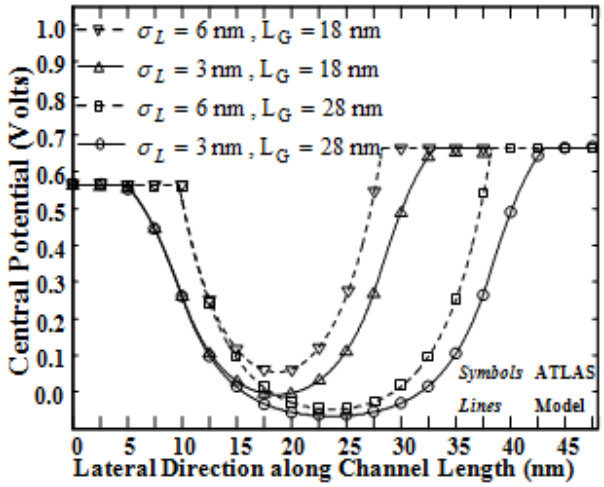

Fig 2.5: Central potential along channel length, Parameters used: $V_{DS} = 0.1\,V$, $t_{si} = 7\,nm$, $L_{ul} = 10\,nm$, $V_{GS} = 0.1\,V$, $t_{ox} = 1\,nm$.

where, Δf is the decrease in the maximum operating frequency f due to the DIBL described by Eq. (2.44).

2.4 Results and Discussion

In this section, we will present some of our model results related to the channel central potential, threshold voltage, DIBL and loss of switching speed of the underlap DG MOSFETs with Gaussian doped source/drain region. We will also compare the results with the TCAD simulation data obtained by using the ATLAS^{TM} 2D device simulation software. The drift-diffusion (DD) model along with the classical Fermi-Dirac statistics has been used for simulating the device structure in the ATLAS^{TM} software. The quantum model $(quantum)$ has been used in the simulation to include the quantum mechanical effects. This model is based on the Wigner function equations-of-motion which employ quantum correction potential in the carrier current and energy flux equations. Modeling has been done under the assumptions of identical front and back gate structures with same gate-oxide thicknesses and tungsten (with work function $\phi_M = 4.7eV$) as the gate electrode material for both of the gates of the device.

Central Channel Potential: The variations of the central channel potential $\psi_{ci}(x) - \phi_f$ measured with respect to the Fermi potential $\phi_f = V_T \ln(N_a / n_i)$ as a function of lateral channel position have been shown for different combinations of σ_L and V_{DS} in Fig 2.2, σ_L and V_{GS} in Fig 2.3, σ_L and t_{Si} in Fig 2.4, and σ_L and L_G in Fig 2.5 for fixed values of underlap length (L_{ul}) and other device parameters. The central channel potential profiles

shown in Figs. 2.2, 2.3, 2.4 and 2.5 clearly demonstrate that the decrease(increase) in source-to-channel barrier (i.e. increase(decrease) in the DIBL) with the increase(decrease) in V_{DS}, V_{GS} and t_{si}; and decrease (increase) in L_G are stimulated further by the increase (decrease) in the straggle parameter value (σ_L). This may be attributed to the decrease (increase) in the source (drain)-channel abruptness with the increased (decreased) value of σ_L. The increased (decreased) junction abruptness reduces (increases) the effective channel length which increases (decreases) the SCEs. Thus, unlike the uniformly doped S/D gate-underlap DG MOSFETs (Bansal and Roy 2007), the value of the straggle parameter (σ_L) of the lateral Gaussian doping in the S/D region can be explored as an additional parameter for controlling the DIBL and SCEs of the underlap DG MOSFETs.

Threshold Voltage, DIBL and Loss of Switching Speed: The combined effects of σ_L and underlap length L_{ul} on the threshold voltage (V_{thf}) have been demonstrated by plotting the V_{thf} as a function of L_{ul} in Fig 2.6 for different values of σ_L but for fixed values of other device parameters. It is observed that, for a fixed value of L_{ul} (and other device parameters), the threshold voltage (V_{thf}) is decreased with the increase in σ_L as evidenced from the potential profiles shown earlier in Figs. 2.2-2.5. Further, for a fixed value of σ_L, the threshold voltage roll-off is observed to be increased with the decreased in the gate-underlap spacer length L_{ul} due to enhanced SCEs. It is also observed from Fig 2.6 that the roll-off becomes the lowest for $\sigma_L \sim 3\text{nm}$ for all values of the underlap length considered in the present study. Clearly, the threshold voltage roll-off of underlap

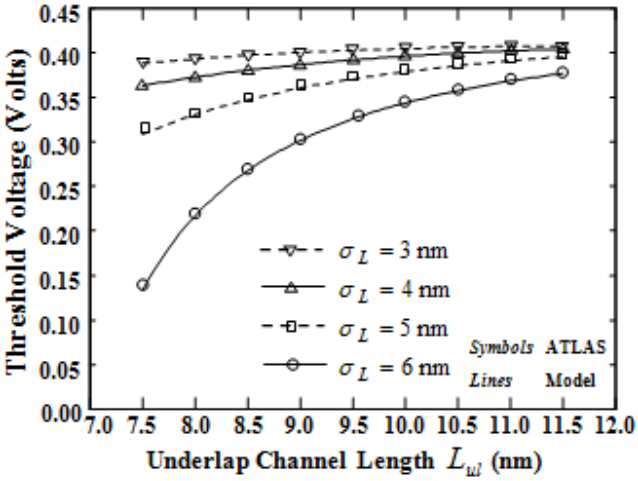

Fig 2.6: Threshold Voltage vs. Underlap Channel Length for different values of σ_L Parameters used: $t_{si} = 7\,nm$, $t_{ox} = 1nm$, $V_{DS} = 0.1\,V$, $L_G = 18nm$.

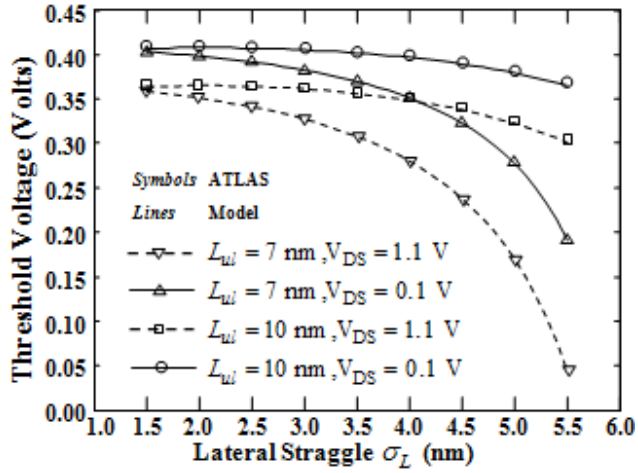

Fig 2.7: Threshold Voltage vs. Lateral Straggle for different values of L_{ul} and V_{DS} .Parameters used: $t_{si} = 7\,nm$, $t_{ox} = 1nm$, $L_G = 18\,nm$.

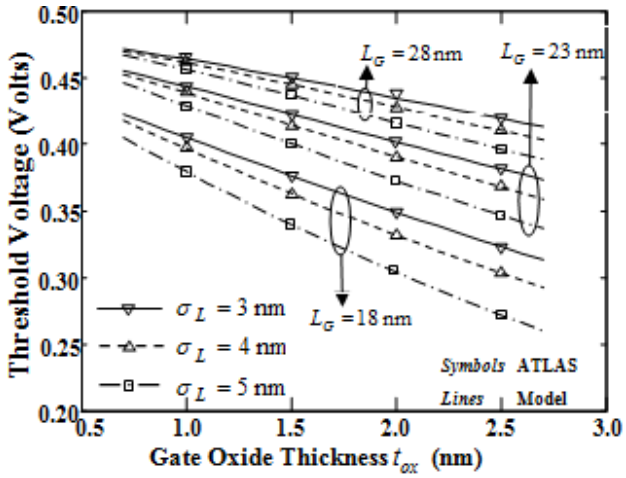

Fig 2.8: Threshold Voltage vs. Gate oxide thickness for different values of σ_L and L_G. Parameters used: $V_{DS} = 0.1V$, $L_{ul} = 10\,nm$, $t_{si} = 7\,nm$.

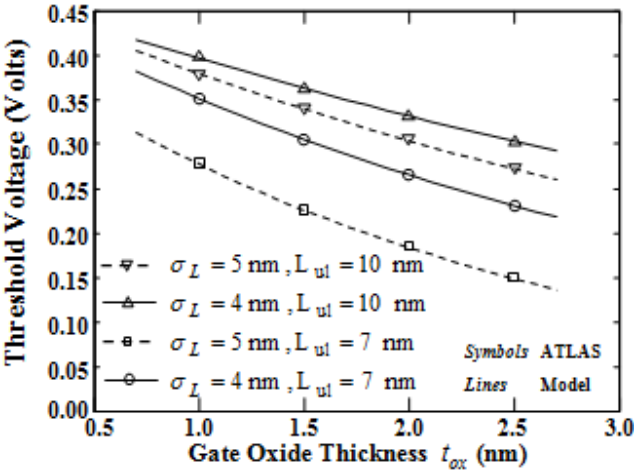

Fig 2.9: Threshold Voltage vs. Gate oxide thickness for different values of σ_L and L_{ul}. Parameters used: $V_{DS} = 0.1\ V$, $L_G = 18\,nm$, $t_{si} = 7\,nm$.

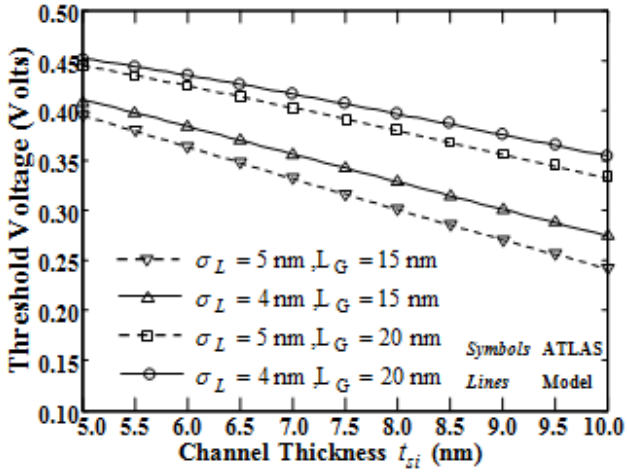

Fig 2.10: Threshold Voltage vs. Channel thickness for different values of σ_L and L_G. Parameters used: $V_{DS} = 0.1\,V$, $L_{ul} = 10\,nm$, $t_{ox} = 1\,nm$.

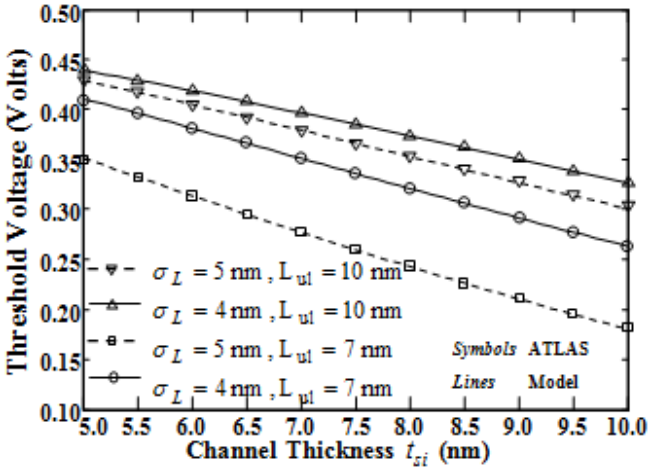

Fig 2.11: Threshold Voltage vs. Channel thickness for different values of σ_L and L_{ul}. Parameters used: $V_{DS} = 0.1\,V$, $L_G = 18\,nm$, $t_{ox} = 1\,nm$.

DG MOSFETs with a lateral Gaussian doping profile S/D region can be optimized by selecting a suitable value of the lateral straggle parameter σ_L of the profile. To investigate further the effect of σ_L on the threshold voltage, the variation of threshold voltage as a function of σ_L for two pairs of L_{ul} and V_{DS} values has been plotted in Fig 2.7. Clearly, V_{thf} is decreased with the increased value of σ_L as well as V_{DS} for all values of L_{ul}. However, the smaller difference between the threshold voltages for $L_{ul} = 10\text{nm}$, $V_{DS} = 1.1\text{V}$ and $L_{ul} = 10\text{nm}$, $V_{DS} = 0.1\text{V}$ pair than the difference between the threshold voltages for $L_{ul} = 7\,\text{nm}$, $V_{DS} = 1.1\text{V}$ and $L_{ul} = 7\,\text{nm}$, $V_{DS} = 0.1\text{V}$ pair observed in Fig 2.7 implies that the smaller DIBL (i.e. better SCEs) is achieved for 10 nm than that for the 7 nm underlap length devices. Fig 2.8 shows the variation of the V_{thf} as a function of the gate oxide thickness t_{ox} for different values of σ_L and L_G. The V_{thf} is observed to be decreased with increased t_{ox}, decreased L_G and increased σ_L due to the increased SCEs . The variation of V_{thf} with t_{ox} for two sets of values of L_{ul} and σ_L plotted in Fig 2.9 shows that deterioration of threshold voltage (DIBL) with the increase in σ_L is smaller for $L_{ul} = 10\text{nm}$ than that for $L_{ul} = 7\,\text{nm}$ device. Similarly, Fig 2.10 demonstrates the decrease V_{thf} with the increased channel thickness t_{si}, and σ_L, but decreased channel length L_G. The plot of V_{thf} versus t_{si} for two sets of σ_L and L_{ul} values in Fig 2.11 confirms the smaller degradation of V_{thf} of underlap DG MOSGETs with $L_{ul} = 10\text{nm}$ than that of the devices with $L_{ul} = 7\text{nm}$ underlap lengths. The threshold voltage degradation shown in Fig 2.10 and Fig 2.11 with the increased channel thickness

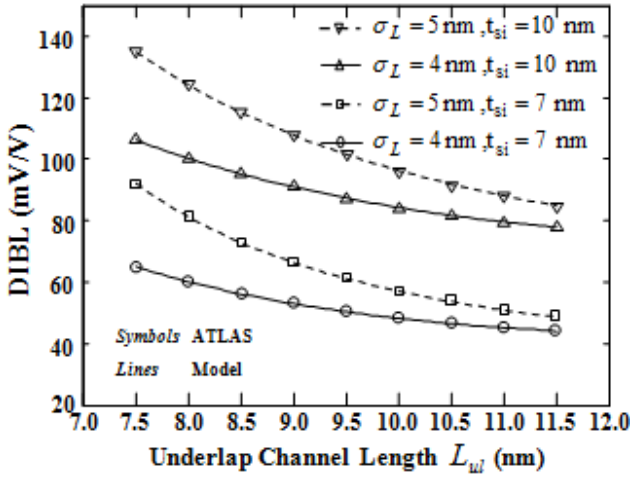

Fig 2.12: DIBL vs. Underlap Channel Length for different values of σ_L and t_{Si} Parameters used: $V_{DS} = 0.1\,\mathrm{V}$, $L_G = 18\,\mathrm{nm}$, $t_{ox} = 1\,\mathrm{nm}$.

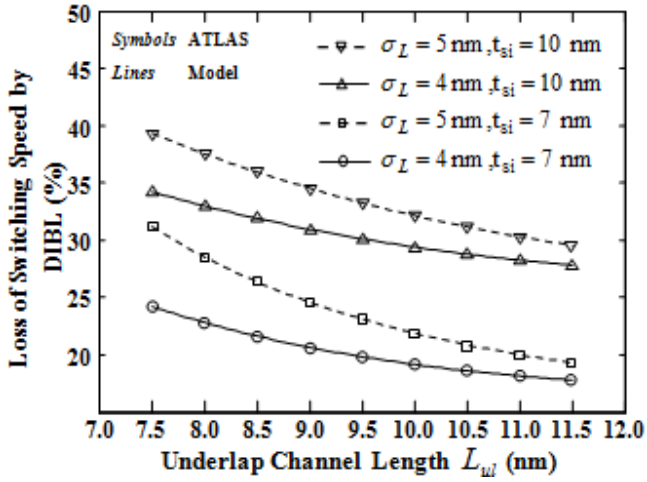

Fig 2.13: Loss in Switching Speed by DIBL vs. Underlap Channel Length for different values of σ_L and t_{Si} Parameters used: $V_{DS} = 0.1\,\mathrm{V}$, $L_G = 18\,\mathrm{nm}$, $t_{ox} = 1\,\mathrm{nm}$.

may be attributed to the reduction in the gate control over the channel carriers owing to the decrease in the L_{eff}/t_{si} ratio. We now consider the DIBL characteristics as a function of the underlap length L_{ul} shown in Fig 2.12. It is observed from the figure that, while the DIBL is decreased with L_{ul}, it is increased with both the channel thickness t_{si} and lateral σ_L. The deteriorations of the DIBL at larger channel thickness and larger σ_L are attributed to the poor control of the gate over the channel carriers and decrease in the source-channel abruptness respectively, as discussed earlier. Finally, the loss of switching speed described by Eq. (2.44) due to the DIBL has been plotted in Fig 2.13. The loss is found to be ~3% to 4% lesser in the underlap DG MOSFET devices with body thickness of $t_{si} = 7\,\text{nm}$ than the devices with $t_{si} = 10\,\text{nm}$ with every $\sim 1\,\text{nm}$ increase in the value of σ_L. Thus, the loss in switching speed of the DG MOSFETs can be optimized by controlling the values of the additional parameters σ_L and L_{ul} introduced with the USJ underlap DG MOS structures considered in the present study.

2.5 Conclusion

A comprehensive analytical study has been presented for the modeling of 2D potential distribution and threshold voltage of underlap DG MOSFETs with lateral Gaussian doping in the source/drain (S/D) regions. Parabolic approximation along with the conformal mapping technique has been used for obtaining the potential function by solving the 2D Poisson's equation with suitable boundary conditions. The effects of the lateral struggle parameter (σ_L) and the underlap length (L_{ul}) on the potential

distribution, threshold voltage, DIBL and switching speed of the devices have been analyzed in details. While the threshold voltage is decreased with the increase in σ_L, the same is observed to be improved with the increase in L_{ul}. Although, the DIBL, threshold-voltage roll-off, and loss of switching speed are found to be deteriorated with the increase in σ_L, however, they are improved by increasing the underlap length, L_{ul}. Noticeable control of the threshold voltage with the control of σ_L and L_{ul} parameters may be explored for achieving the higher drive current with lower SCEs in the underlap DG MOS device structures with lateral Gaussian doping in S/D over the conventional DG MOSFETs. Proper optimization between the geometrical parameters and doping profile parameters should be made in order to make a healthy trade-off among the drive current, SCE and Electrostatic integrity of the device. Thus the USJ underlap DG MOSFETs with lateral Gaussian doping S/D structures can be considered as a potential candidate both for high drive current and better switching speed. An excellent agreement between the analytical results and the ATLAS^{TM} based TCAD simulation date confirms the validity of our proposed model.