Chapter 1

Introduction and Scope of Thesis.

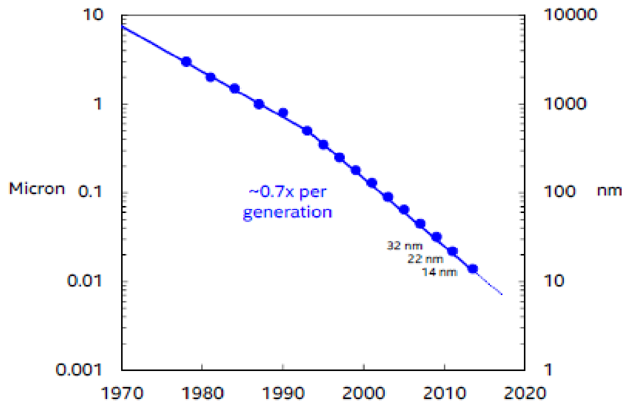
1.1 Introduction

The metal-oxide-semiconductor field effect transistor (MOSFET) (Kahng and Atalla 1960) has been playing the key role in the growth and development of integrated circuit (IC) technology over more than past five decades. The relentless scaling of the MOS transistors have enabled us to integrate millions of transistors in a single wafer for developing high-performance and low-power ICs for various computing and communication applications. Several forms of the MOS transistors have been developed by introducing various structural and material changes in the conventional bulk MOSFETs in order to suppress the adverse effects caused by the dimensional miniaturization owing to scaling.

In 1965, Gordon Moore predicted that the complexity in the IC would continue to double annually until about 1980 and it would decrease to a rate of doubling approximately every two years thereafter (Gordon E. Moore 1965) Following the Moore's prediction, the channel length of the MOSFET has been reduced from micrometer (μm) to sub 20 nm regime during the past 30 years. Figure 1.1(a) shows the Intel scaling trend both in microscale [left] and nanoscale [right] which try to follow ~ 0.7× scaling per generation from years 1970 to 2020 (Bohr 2014). Figure 1.1(b) demonstrates the Intel technology roadmap to define the current status of recent technology nodes of transistors where 22 nm tri-gate FinFET is already manufactured (H Iwai 2009) and 14 nm technology node is

(a)

Intel Scaling Trend



Scaled transistors provide:

- Higher performance
- Lower power
- Lower cost per transistor

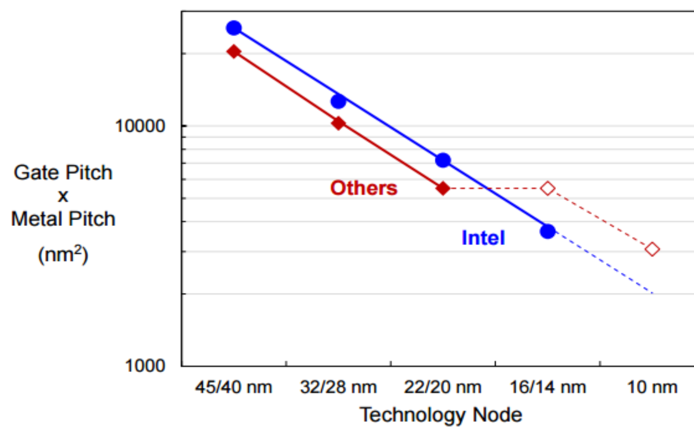
Moore's Law continues!

(b)

Intel Technology Roadmap

(c)

Logic Area Scaling



Intel continues scaling at 14 nm while other pause to develop FinFETs

Fig 1.1(a): Intel scaling trend trying to sustain the Moore's law to provide high performance, low power dissipation and low cost per transistors, **(b):** Intel Technology Roadmap, **(c):** Comparative Logic Area Scaling between Intel and other semiconductor industries (Bohr 2014).

about to be introduced for manufacturing. The research of technology node of 10 nm transistor has already been finished and very soon it will come into development; whereas the research of technology node of 7 nm transistor is still in developing phase (Standaert *et al.* 2016), (Xie *et al.* 2015). Figure 1.1(c) compares the logic area scaling trend between Intel and other semiconductor industries, where blue line indicates the logic area scaling of Intel and the red line stands for logic area scaling of other industries. The switching from single-gate to multi-gate MOSFET structures has made possible for Intel to scale down to 14 nm technology node to continue the scaling trend while other industries are still working on the SOI technology and are paused at 22 nm technology node. The aim of technology scaling is to shrink the overall size of MOSFET without deteriorating the device performance. However, in practice, the reduction in the dimensions of the MOSFETs below sub-100nm technology node may lead to the degradation of the device performance severely due to the so called short-channel effects (SCEs)(S. Yang *et al.* 2005). The threshold voltage, subthreshold swing and subthreshold leakage current characteristics of the MOS transistors are degraded severely due to the SCEs. As a consequence, the lower limit of achievable channel lengths of MOS transistors is practically dependent on the SCEs for a given technology. Yau (Yau 1974) proposed a charge conservation principle based simple expression for the threshold voltage of an insulated gate FET (IGFET) by considering the two-dimensional edge effects. They (Yau 1974) suggested that following two geometrical modifications of the MOS transistors could lead to the reduction in the SCEs:

- The gate oxide thickness needs to be decreased to increase the gate control over the channel of the device
- The depth of the source/channel and drain/channel junctions should be reduced.

Dennard *et al.* (Dennard *et al.* 1974) have proposed a scaling theory, called constant field scaling, in which the electric fields inside the transistors are maintained constant whenever the device dimensions are reduced due to a change in the technology node. Under this scaling rules, if the channel length is scaled by 'γ', then the gate oxide thickness, source/drain channel junction depth, supply voltage and threshold voltage are also required to be scaled by the same factor 'γ' whereas the substrate doping is to be increased by the factor 'γ'. According to the constant field scaling, the switching speed is increased by the factor of 'γ' with reductions in the dc and dynamic power dissipation by a factor of "$1/\gamma^2$", power-delay product by a factor of "$1/\gamma^3$" at the cost of the decreased power supply voltage by the factor of '$1/\gamma$'. Although, the constant field scaling is suitable for low-power applications but the reduction in the supply voltage below a certain level is not permissible for the practical operations of the CMOS circuits. In order to overcome the reduction in power supply, another scaling theory namely the constant voltage scaling is introduced in the literature (Y. Taur and T. H. Ning 1998). According to this scaling rule, all the device dimensions are scaled down by the factor 'γ' with the increased doping concentration by the factor 'γ' similarly as those of the constant field scaling rules except the supply voltage which is kept constant in this case. This scaling principle leads a speed of the device by a factor of "γ^2" at the cost of increased power dissipation by a factor of "γ". Thus the constant field scaling is suitable for high-speed applications at the cost of increased power dissipation in the device. The effects of constant field and constant voltage scaling on various parameters of the device have been compared in Table 1.1. Note that the increased doping concentration by the factor of "γ" in the scaling leads to the degradation of the mobility of carriers due to increased impurity scattering. Further, the higher switching speed is achieved at the cost of increased power dissipation in the constant voltage scaling.

Table 1.1 Scaling of device dimensions and circuit parameters (Y. Taur and T. H. Ning 1998)

Device Parameter		**Multiplication Factor,** $\gamma > 1$ **Scaling parameter,** α			
		Constant - field Rules	**Constant-voltage Rules**	**Generalized Rules**	
Scaling assumption	Device dimension (t_{ox}, L, W)	$1/\gamma$	$1/\gamma$	$1/\gamma$	
	Doping concentration(N_d, N_a)	γ^2	γ^2	$\alpha\gamma$	
	Voltage(V)	$1/\gamma$	1	α/γ	
Derived scaling behavior of device parameters	Electric field (E)	1	γ	α	
	Depletion Layer width(W_d)	$1/\gamma$	$1/\gamma$	$1/\gamma$	
	Capacitance (C)	$1/\gamma$	$1/\gamma$	$1/\gamma$	
	Inversion/Layer charge density (Q_i)	1	γ	1	
				Long channel	**Velocity Saturation**
	Carrier velocity (v)	1	γ	α	1
	Drift current (I)	$1/\gamma$	γ	α^2/γ	α/γ
	Channel resistance (R_c)	1	$1/\gamma$	α^2/γ	α/γ
Derived scaling behavior of circuit parameters	Circuit delay time	$1/\gamma$	$1/\gamma^2$	$1/\alpha\gamma$	$1/\gamma$
	Power dissipation per circuit	$1/\gamma^2$	γ	α^3	α^2/γ^2
	Power density	1	γ^3	α^3	α^2
	Power-delay product per circuit	$1/\gamma^3$	γ	α^2/γ^3	

Y. Taur and T. H. Ning (Y. Taur and T. H. Ning 1998) have proposed a generalized hybrid scaling theory obtained by mixing the principles of constant field and constant voltage scaling rules for optimizing the device performances for high-speed and low-power applications. The scaling of bulk MOSFETs has reached to its bottleneck due to the detrimental SCEs. As a consequence, researchers have been working hard to find the alternate of non-classical MOS transistors with single-gate and multiple-gate structures for sustaining scaling for future generation VLSI/ULSI circuits and systems. In this direction, various theoretical and simulation based studies have been reported on the performances of non-classical MOS transistors obtained by incorporating several techniques including the substrate engineering (i.e. use of Silicon-on-Insulator (SOI), SiGe etc. as substrates) (Colinge 2004), (Cheng *et al.* 2001), (S. Yu *et al*. 2004), gate-structure engineering (i.e. use of single/multiple gate structures with different high-k gate dielectric oxides and/or cascaded connection of different gate-electrode materials) (Hiroshi Iwai and Momose 1995), (B. Cheng *et al.* 1999), (B. H. Lee *et al.* 2008) and (Wang *et al.* 2006), channel engineering (i.e. use of different materials such as SiGe, III-V compounds etc. with various channel doping profiles) (Krishnamohan *et al.* 2008), (Beneventi *et al.* 2014) and (Amir N Hanna, Fahad, and Hussain 2015), and source/drain engineering (i.e. use of recessed source/drain and raised source/drain structures with graded and abrupt junctions) (Z. Zhang, S. Zhang, and Chan 2004), (Svilic, Jovanovic, and Suligoj 2009), (Saramekala *et al.* 2013), (Waite *et al.* 2005), (D. Chen, Jacobson, and Liu 2013) and (Holtij *et al.* 2012) in the conventional bulk MOSFET technology. In fact, there is an ample opportunity to investigate the effects of one or more aforementioned techniques on the performance optimization of various non-classical MOS transistors (i.e. MOSFET structures other than the conventional bulk MOSFETs). While the mathematical modeling can be explored for

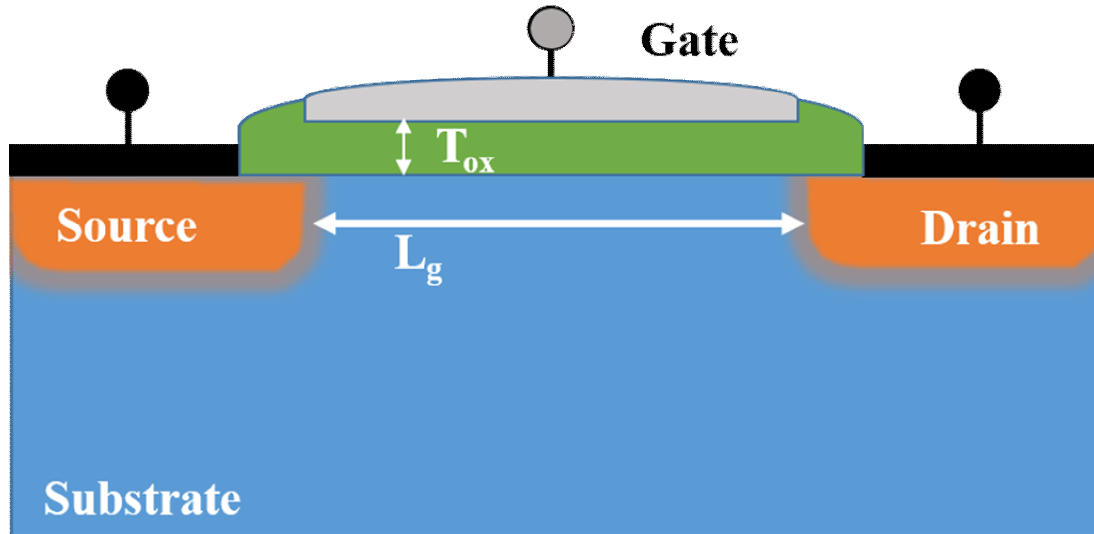


Fig 1.2: Schematic diagram of the bulk Si MOSFET.

investigating the detrimental SCEs on various device characteristics, the industry standard TCAD simulation based investigations are also equally important for optimizing certain performances of complicated MOS transistor structures to avoid the mathematical complexity. In view of the above, the present thesis has been designed to investigate the effects of raised source drain structures on the drivability and/or subthreshold characteristics of some gate-undelap non-classical MOS structures.

1.2 Non-Classical MOS Transistors

The schematic structure of a conventional bulk MOSFET is shown in Fig 1.2. It has been mentioned that the severe SCEs have restricted the scaling of the bulk MOSFETs with the channel lengths in the sub-100 nm regime. Thus, various modifications in the device geometry as well as in the device parameters have been introduced in the conventional MOS transistors to suppress the SCEs resulted for maintaining scaling for future generation VLSI/ULSI circuits and systems. We will call such MOS devices which are

different from the conventional bulk MOSFETs introduced in our texts as the non-classical MOS transistors. For example, the conventional SiO_2 can be replaced by other high-k dielectrics such as hafnium silicate ($HfSiO_4$), zirconium silicate ($ZrSiO_4$), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2) etc. for achieving higher gate oxide capacitance (B. Cheng *et al.* 1999), (M. J. Kumar, Gupta, and Venkataraman 2006) and (Chau *et al.* 2004). Similarly, we can engineer the gate structure (by using double gate (DG) (Kranti, Hao, and Armstrong 2008), triple gate (TG) (Saitoh *et al.* 2011), Fin gate (FG) (Pal, Kaushik, and Dasgupta 2014), and gate-all-around (GAA) (X. Chen and Tan 2014) structures to improve the controllability over the channel), gate electrode structure (by using a cascaded connection of multiple materials of different work functions as gate electrode structure), channel region (by using materials such as the Ge (Akatsu *et al.* 2006), SiGe, III-V group compounds in place of Si in the channel to improve the carrier mobility, by using different doping profiles (Cheng *et al.* 2001), (S. Yu *et al.* 2004), (Krishnamohan *et al.* 2008), (Beneventi *et al.* 2014) and (Amir N Hanna, Fahad, and Hussain 2015) and introducing strain in the channel (M. Kumar *et al.* 2013) to improve the mobility of the channel carriers), source/drain structure (by using raised source/drain (D. Chen, Jacobson, and Liu 2013) and recessed source/drain structures (Svilic, Jovanovic, and Suligoj 2009) and (Saramekala *et al.* 2013)) etc. to achieve many new non-classical MOS structures with better immunity to the SCEs over the conventional bulk MOSFETs. Other non-classical MOS device structures namely the junctionless field effect transistors (JFETs) (Ferain, Colinge, and Colinge 2011), tunnel field effect transistors (TFETs) (Anghel *et al.* 2010), and Ring MOSFETs (Williams, Silva, and Gokirmak 2012) and Kumar *et al.* (S. Kumar *et al.* 2015) have also been introduced in the literature. In place of using source/channel and drain/channel homo-junctions, two different materials can be used for the channel and

source/drain to have hetero-junctions at the source/channel and drain/channel junctions (A. N. Hanna and Hussain 2015) and (Asthana *et al.* 2014). In the following subsections, we will briefly introduce some commonly used mechanisms which can be explored for achieving various non-classical MOS transistor structures operating in the inversion mode similarly as the bulk MOS transistors.

1.2.1 Gate Dielectric Engineering

Due to relentless scaling, the gate leakage current has been drastically increased due to the shrinkage of the SiO_2 based gate oxide thickness in the bulk MOSFETs. Thus, as per the demand of the scaling, the use of ultra-thin gate dielectrics (Hiroshi Iwai and Momose 1995) may lead to excessive static power dissipation in the MOS devices. The gate leakage current can be reduced by using high-k dielectric materials as the gate oxide in the device. Note that the gate oxide capacitance per unit area is be given by $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ where ε_{ox} and t_{ox} are the permittivity and thickness of the oxide layer respectively. Clearly, use of larger value of ε_{ox} may allow us to use larger oxide thickness t_{ox} to achieve same density of oxide capacitance but with lower gate leakage current. For a fixed gate oxide capacitance, the physical thickness of the high-k materials is given by $t_{hk} = t_{ox}\left(\frac{\varepsilon_{SiO2}}{\varepsilon_{hk}}\right)$, where ε_{SiO2} is the permittivity of silicon dioxide, $\boldsymbol{\varepsilon_{hk}}$ is the permittivity of high-*k* dielectric material and t_{ox} is the actual SiO_2 oxide thickness required to achieve the desired oxide capacitance in the bulk MOS device. In recent years, materials like $\mathbf{Si_3N_4}$ (relative permittivity, k =7), $\mathbf{HfO_2}$ (k =22), $\mathbf{ZrO_2}$ (k =25) , $\mathbf{Ta_2O_3}$ (k =26), $\mathbf{HfSiO_4}$ (k =27), and $\mathbf{TiO_2}$ have come up as strong replacements of $\mathbf{SiO_2}$ when the channel length is scaled down to sub 20 nm

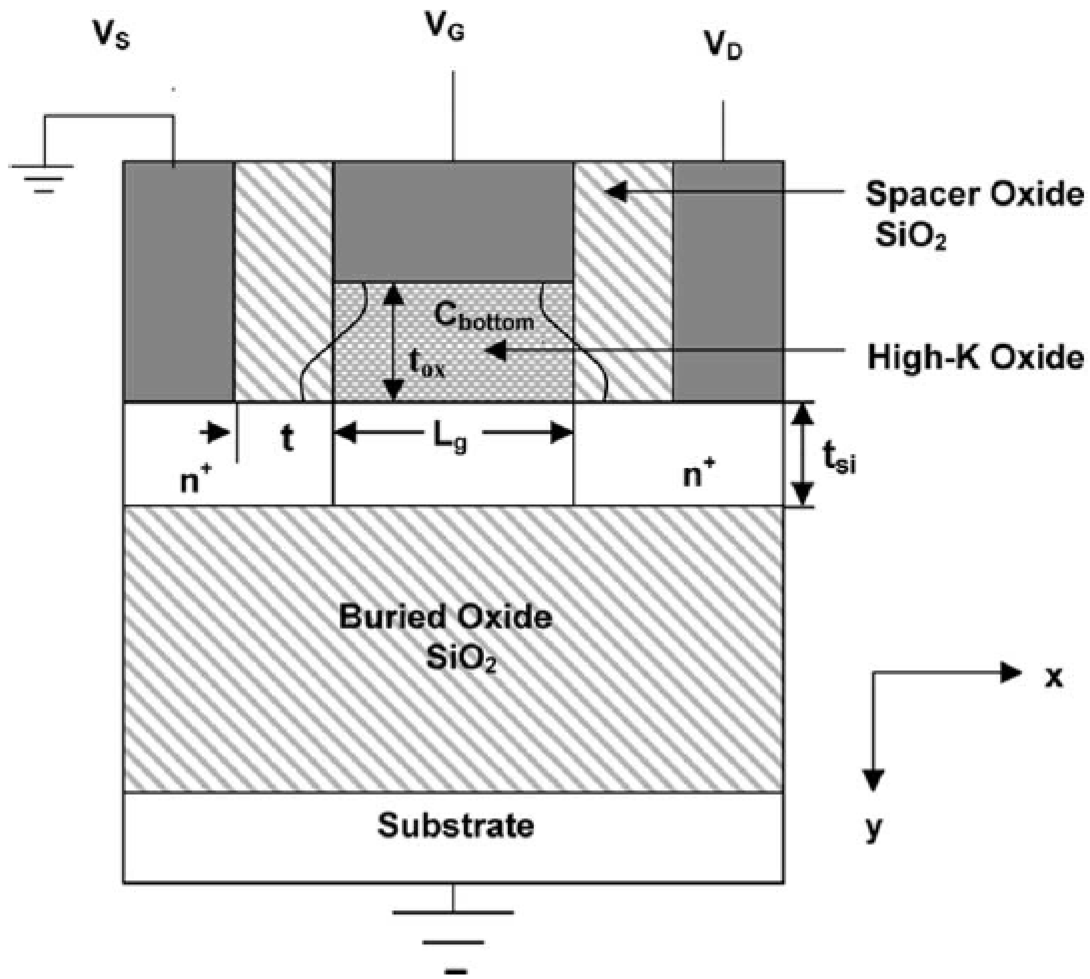


Fig 1.3: Cross-sectional view of an SOI MOSFET showing the internal parasitic fringe capacitance (M. J. Kumar, Gupta, and Venkataraman 2006).

(B. Cheng *et al.* 1999). The high-*k* materials can also be used at the gate side spacer regions (i.e. between the source/drain and gate) to enhance the figure of merits (FOMs) including g_m/I_{DS} (transconductance generation factor), g_d (output conductance) and g_m/g_d (intrinsic gain) of the device. The high-k dielectric based spacer engineering technique may be explored to improve the subthreshold and analog/RF circuit performances of the non-classical MOS devices (Pradhan *et al.* 2014), (Koley *et al.* 2013). It has been reported that the use of high-*k* as gate dielectric and low-*k* as side spacer may

enhance the on-state current in the tunnel FETs (Anghel *et al.* 2010). Even some researchers have used hetero dielectric in DG tunnel FETs in order to improve I_{on}/I_{off} ratio and average subthreshold swing (Jain, Prabhat, and Ghosh 2015; M. J. Lee and Choi 2012). However, in the case of DG MOSFETs, lateral source/drain doping gradient along with spacer width can effectively control short channel effects through the modulation of effective channel length (Kranti and Armstrong 2006). Use of high-*k* dielectrics in stacked gate oxide based DG MOSFET structures have been reported for reducing the field induced barrier lowering (FIBL) (Ma *et al.* 2012), (Ji *et al.* 2008). Analytical formulation of the threshold voltage of the high-*k* based SOI MOSFET shown in Fig 1.3 has been reported by (M. J. Kumar, Gupta, and Venkataraman 2006), (Feng, Ji, Jing-Ping, Xu, Pui-To 2007) while the fringe capacitance model of the device has been proposed by Ji *et al.* (Ji *et al.* 2008).

1.2.2 Channel Engineering

The threshold voltage and maximum depletion width cannot be controlled independently in a MOSFET with a uniform channel doping profile (Y. Taur and T. H. Ning 1998). Uniform doping level that yields acceptable depletion depth may lead to undesirable threshold voltages and vice versa (Y. Taur and T. H. Ning 1998). Some researchers (G. Zhang, Shao, and Zhou 2008), (Suzuki *et al.* 2007) have reported that the doping profile in the channel region of practical MOSFETs is inherently of non-uniform nature resulted from various fabrication steps. For example, the diffusion process used for channel doping and the ion-implantation method used for the threshold adjustment in the practical MOSFETs may make the doping profile in the channel region non-uniform in nature. In general, the doping profile created by the ion-implantation is considered to be a Gaussian

function. Thus, it is difficult to develop theoretical models for MOSFETs with a Gaussian doping profile due to the analytically non-integral nature of the Gaussian function over any finite interval. Dasgupta and Lahiri (Dasgupta and Lahiri 1988) have proposed a approximated Gaussian-like analytic function to replace the original non-analytic Gaussian function for mathematical simplification purposes. This new function closely resembles the Gaussian function and can be integrated twice over any finite interval (Dasgupta and Lahiri 1988). Super retrograde doping profiles (De Indranil and Osburn 1999) and halo/pocket implants (B. Yu *et al.* 1997) at the channel created locally with a high doping concentration at the source and drain junction is basically an to reduce the SCEs, halo/pocket implants increase the average channel doping to increase the threshold voltage with the decrease in the effective channel lengths which may result in decreased SCEs. Further, the super retrograde doping profiles in the MOS transistors can be used to control the depletion regions at the source (drain)/channel junctions without degrading the mobility of the charge carriers in channel. Kaur *et al.* (Kaur *et al.* 2007) have used graded channel to control the electric field at the drain side of the MOSFETs for controlling the hot electron effects in GAA MOSFETs. Ramezani *et al.* (Ramezani *et al.* 2016) have employed a vertical graded doping in the channel region to improve the hot carrier effects (HCEs), short-channel effects (SCEs), gate induced drain lowering (GIDL), leakage current and self-heating effects (SHEs). Barraud *et al.* (Barraud *et al.* 2005) have introduced strain engineering in the Si channel to enhance the channel carriers of the MOS devices. Many researchers have replaced the conventional Si channel by other materials such as the Ge (Akatsu *et al.* 2006), SiGe (Rahimian and Orouji 2011), InAs (Beneventi *et al.* 2014) etc. to make the carrier mobility higher than that of the Si. Apart from the doping distribution, strain and new materials other than the Si in the channel, the

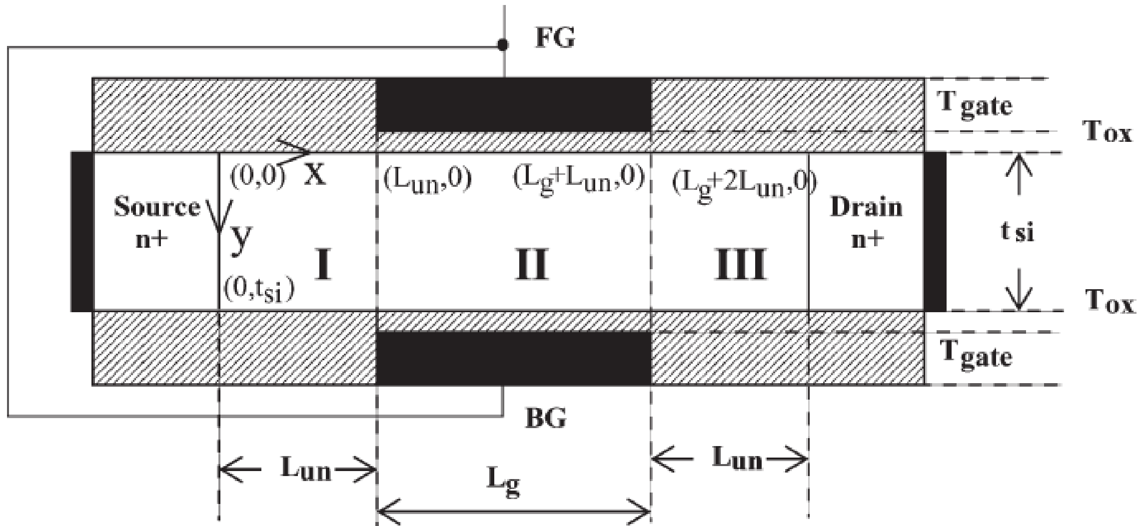


Fig 1.4: Schematic of an underlap DGMOS with two underlap and one overlap regions (Bansal and Roy 2007).

performance can also be controlled by using the gate-underlap (Bceuf *et al.* 2001) or gate overlap structures (Nandi *et al.* 2013). It is observed that the gate overlapped device structure is more prone to short-channel effects (SCEs) than the underlap structures (Nandi, Saxena, and Dasgupta 2013). Gusmeroli *et al.* (Gusmeroli *et al.* 2003) have proposed the need of a large underlap region (>10 nm) for improving the device performance. Based on a simulation study, Paul *et al.* (Paul, Bansal, and Roy 2006) have observed that about eight times reduction in the effective gate capacitance can be achieved by optimizing gate-underlap region. They (Paul, Bansal, and Roy 2006) explored their observation to reduce upto 40% delay and upto seven times power delay product (PDP) in a three-stage ring oscillator (RO). They also have designed a circuit for 1-bit full-adder circuit with operating frequency at 1.25 GHz and have observed almost six times reduction in the power dissipation than the circuit designed by using the standard overlap DG MOSFETs. Kim *et al.* (Kim et al. 2006) have formulated the fringe capacitance analytically for a non-classical CMOS Device with gate-underlap regions. Kim & Fossum

(Kim and Fossum 2007) have reported the design optimization and performance projections of gate-underlap double-gate FinFETs for SRAM applications. Yang *et al.* (Yang *et al*. 2007) have optimized the speed of a gate-underlap DG FinFET based CMOS circuit. The gate fringe-induced barrier lowering in underlap DG MOSFETs has been observed by Sachid *et al.* (Sachid *et al.* 2008). By introducing high-*k* spacers, they (Sachid et al. 2008) have observed significant improvement in the on-state current of gate-underlap DG MOSFETs. Bansal & Roy (Bansal and Roy 2007) have proposed a model for the subthreshold potential distribution of gate-underlap DG MOSFET structure shown in Fig. 1.4. Vaddi *et al.* (Vaddi, Agarwal, and Dasgupta 2011) have modeled the subthreshold current and subthreshold swing of the gate-underlap DG MOSFET structure with a uniformly doped channel.

1.2.3 Gate-Electrode-Material Engineering

In order to improve the performance of the single gate and multiple gate conventional and non-classical MOS transistors, the conventional poly Si gate electrode may be replaced by two or three different materials connected in cascaded with increasing order of their work functions to form the resultant gate electrode (Chiang 2009), (Reddy and Kumar 2005) and (Tiwari *et al.* 2010). The SCEs and HCEs are reported to be reduced significantly by proper selection of the work functions and lengths of the gate electrode materials in such devices. The material near the source side with the highest work function is called the control gate whereas the material with the lowest work function near the drain side is called the screen gate in such structures. A typical triple material single gate SOI MOSFET structure studied by Chiang (Chiang 2009) is shown in Fig. 1.5. Chiang (Chiang 2009) have also proposed an analytical model for subthreshold characteristics of the device to

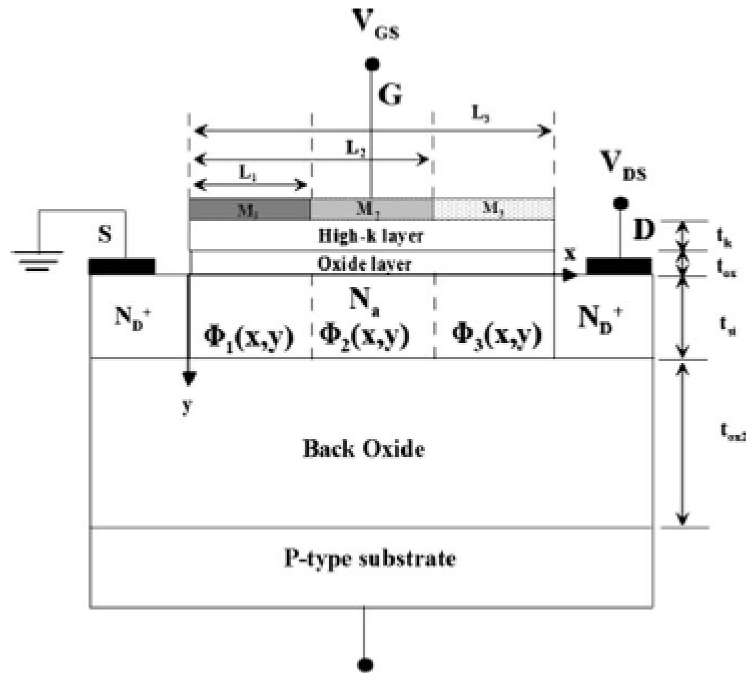


Fig 1.5: Schematic of an tri-material stack gate SOI MOSFET (Chiang 2009).

demonstrate the improvement in the performance by creating two steps in channel potential and screening the channel from the drain (see Fig 1.5 where $\varphi_{m1} > \varphi_{m2} > \varphi_{m3}$). (Reddy and Kumar 2005) have proposed a double gate dual-material structure while (Tiwari *et al.* 2010a) have analytically investigated the subthreshold characteristics of a triple-material-gate (TMG) DG MOSFETs. Such structures are believed to reduce the hot carrier effects due to the reduction of the electric field at the drain side.

1.2.4 Source/Drain Engineering

As the CMOS scaling technology node has reached sub 20 nm, it has practically difficult to neglect the source/drain (S/D) resistance of the MOS transistors. Thus attempts have been made to reduce the source/drain resistance of the MOS devices. One of the techniques for reducing the source/drain resistance is the use of low-barrier Schottky

contacts for the source and drain electrodes to reduce the source/drain parasitic resistance (Lefselter *et al.* 1968) (Ieong *et al.* 1998). Zhu *et al.* (G. Zhu *et al.* 2009) have proposed a compact model for the undoped Si-nanowire MOSFETs with schottky-barrier source/drain. Another method to reduce the source/drain parasitic resistance is to increase the source/drain current flowing area (Holtij *et al.* 2012). Zhang *et al.* (Zhang *et al.* 2004) have used the recessed source/drain silicon-on-insulator (SOI) MOSFET structure obtained by extending the source and drain regions symmetrically in its buried oxide (BOX) region to reduce the source/drain resistance of the device. Sviličic´ *et al.*(Sviličic´ *et al.* 2009) proposed an analytical model for both the potential distribution and threshold voltage of recessed source/drain ultra thin body (UTB) SOI MOSFETs. Saramekala *et al.* (Saramekala *et al.* 2013) have analytically investigated the threshold voltage of a fully depleted recessed source/drain (Re-S/D) SOI MOSFET with a dual-material-gate (DMG) structure. Instead of using a recessed source/drain structure, some researchers have explored the elevated source/drain structure by using selective epitaxial silicon growth on the top of source/drain regions symmetrically in order to trim the series resistance of device Wong *et al.* (Wong *et al.* 1984) and Yamakawa *et al.* (Yamakawa *et al.* 1999) have observed a significant improvement in the drivability performance of the deep-submicron MOSFETs by using elevated source/drain structures. Choi *et al.* (Choi *et al*. 2000) have reported an experimental study to demonstrate that the elevated source/drain structure can be explored for improving the current drive of ultrathin-body (UTB) SOI MOSFET for deep-sub-tenth micron era. Zhang *et al.* (Z. Zhang *et al.* 2003) have reported the reduction in source/drain parasitic resistance and band-to-band drain leakage at off-state in elevated source/drain on insulator structure. Shenoy *et al.* (Shenoy *et al.* 2003) have used simulation tools to optimize the extrinsic source/drain resistance of UTB DG FETs. Zhu *et al.* (M.

Zhu *et al.* 2010) have studied the effects of non-stationary transports in UTB MOSFETs with both the elevated and recessed source/drain structures by using full band Monte Carlo simulation method. Zhu *et al.* (M. Zhu *et al.* 2010) observed that the recessed source/drain engineering can be utilized the velocity over shooting effect to improve the on-state characteristics. Saitoh *et al.* (Saitoh *et al.* 2011) have fabricated the Trigate silicon nanowire MOSFETs with raised source/drain and thin spacer regions for reducing the short-channel effects. Chen *et al.* (D. Chen, Jacobson, and Liu 2013) have compared the performance of the raised source/drain (RSD) double-gate transistors with the dopant-segregated Schottky (DSS) double-gate MOSFETs for low power applications. The RSD MOS transistors are reported to have better performance over the DSS MOSFETs in terms of higher drive current and shorter intrinsic delay over the DSS structures for the same total device length (< 30 nm) (D. Chen, Jacobson, and Liu 2013). Further, the RSD MOS transistor structures can be used to reduce the parasitic resistance of deeply scaled double-gate MOSFETs (D. Chen, Jacobson, and Liu 2013). The 2D modeling of parasitic source/drain resistance in DG-MOSFETs using the conformal mapping technique has been reported by Holtij *et al.* (Holtij *et al.* 2012). However, it is observed that the doping profile engineering at the source and drain regions can play a significant role for optimizing both the source/drain resistance and short channel effects. Ng *et al.* (Ng *et al.* 1986) have formulated the dependence of spreading resistance on the lateral abruptness of the source (drain)-channel junction. Trivedi *et al.* (Trivedi, Fossum, and Chowdhury 2005) have carried out a simulation study for optimizing the source/drain series resistance by using lateral abruptness of source (drain)- channel junction of nanoscale gate-underlap FinFETs. Tassis *et al.* (Tassis *et al.* 2010) has proposed a source/drain engineering technique to optimize the performance of the gate-underlapped lightly doped nanoscale double-gate

MOSFETs. Analytical modeling of threshold voltage and on-state current of USJ DG MOSFETs with lateral Gaussian doping in the source(drain) region has been reported by Nandi *et al.* (Nandi *et al.* 2013). In brief, the raised source/drain engineering, doping profile engineering in the source and drain regions and the gate-underlap features can be combined altogether for proving better flexibility in optimizing the subthreshold characteristics and on-state drive current of all types of MOS transistor structures.

1.3 Some Common Non-Classical MOSFET structures

It is clear from the discussions of the previous section that we can obtain various types of non-classical MOS transistor structure by employing various engineering techniques in the source/drain structure, channel material and channel doping profile, gate-underlap and gate overlap structures, gate-electrode-materials, gate structure etc. Fig 1.6 shows some commonly used non-conventional MOSFET structures which can be broadly classified into two types: (1) Planar MOSFETs and (2) Non-planar MOSFETs. The planer MOS structures are generally of three types namely silicon-on-insulator (SOI) MOSFETs, SOI RingFETs and DG MOSFETs. shown in Fig 1.7. Nanoscale RingFETs [(Williams, Silva, and Gokirmak 2012) and (S. Kumar *et al.* 2015)] are the recent planer MOS structures reported in the literature. The non-planer structures are commonly known as FinFETs. Depending on their gate structures, they are classified as DG FinFETs, Trigate FinFETs, Quadgate FinFETs, Omega Gate FinFETs, Pi Gate FinFETs and Gate-All-Around FinFETs as shown in Fig 1.8. In the planar SOI MOSFETs, the conventional Si substrate is replaced by a SOI substrate containing an ultrathin silicon layer on a thick buried oxide (of SiO_2) layer grown on the Si substrate. Like the conventional MOSFETs, the source/drain and gate structures are grown on the ultrathin Si layer in the SOI MOSFETs. The Si layer

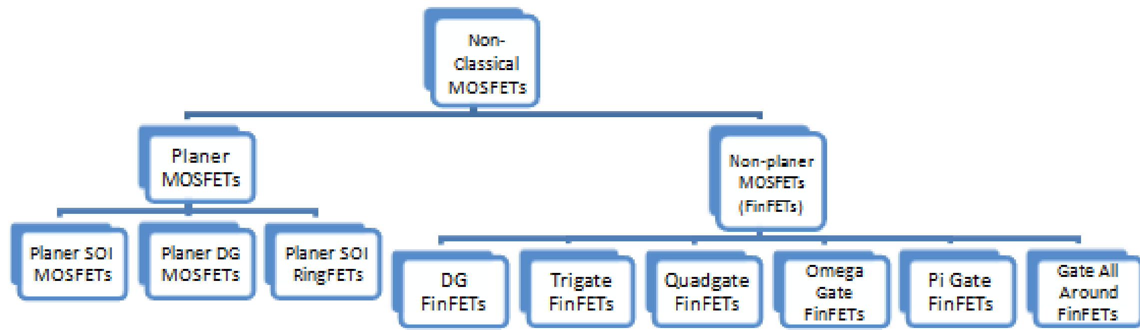


Fig 1.6 Non- classical MOSFET Tree.

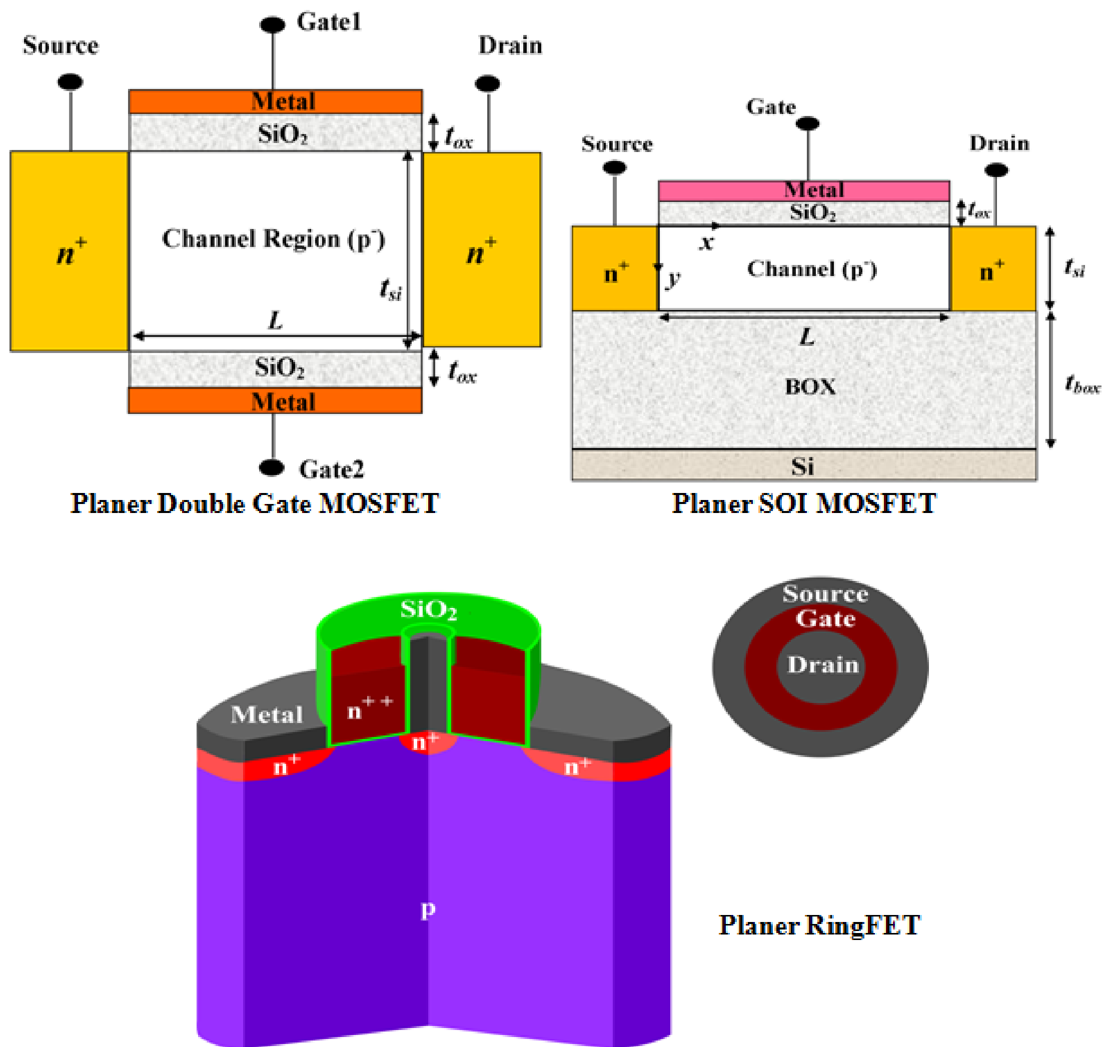


Fig 1.7 Some commonly used non-conventional planer MOSFET structures.

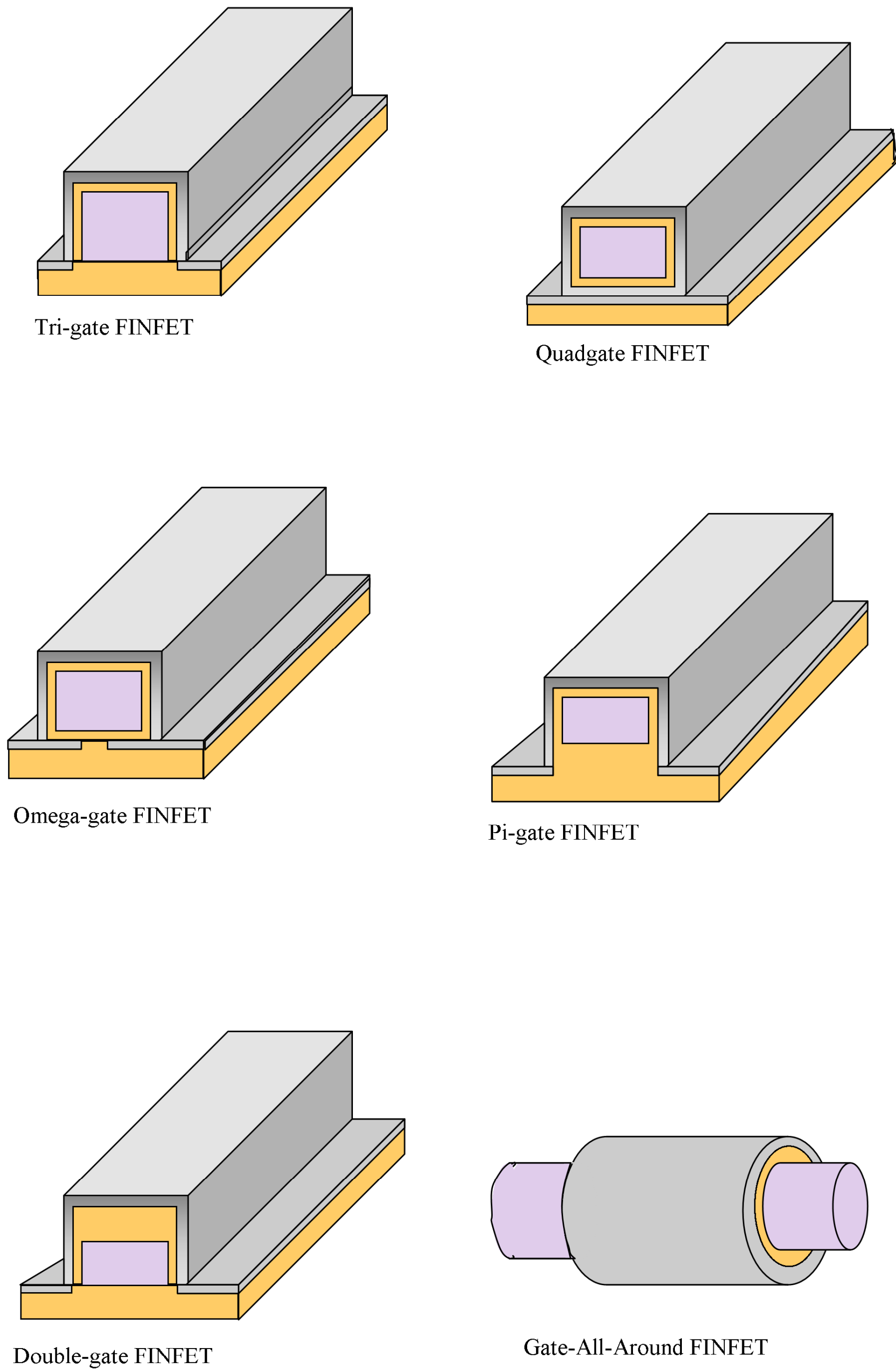


Fig 1.8: Some commonly used non-conventional non-planer MOSFET structures

is called the channel of the device which may be fully depleted (FD) or partially depleted (PD) depending on its thickness (Makoto *et al.* 1989). The floating body effects in the SOI MOSFETs are usually removed by reducing the channel thickness and increasing the channel doping. The SOI MOSFETs have a number of advantages over the bulk MOSFETs like better electrical isolation, reduced SCEs, better immunity to radiation-induced leakage current and diminished latch-up effects [(Colinge 2004), (Markov *et al.* 2012) and (Celler *et al* 2006)]. Ferain *et al.* (Ferain *et al.* 2011) have shown that multiple gate MOS transistors are essential for future generation IC technology due to the increased control of the gates over the channel in short-geometry devices. Thus, the single gate structure has been replaced by two gates in MOS transistors called the double gate (DG) MOSFETs. The DG MOS device stricture are of two types: planar DG MOSFETs and non-planer DG MOSFETs or DG FinFETs. The major difficulty in the planer DG MOSFETs (see Fig 1.6) is associated with the alignment of the front and back gates to achieve optimized performance of the device [(Sarangi *et al.* 2013) and (Sharma *et al.* 2016)]. The above problem is removed in the non-planar DG FinFETs by using vertical gates as shown in Fig 1.7 (Hisamoto *et al.* 2000). The tri-gate FinFETs (Doyle et al. 2003), GAA MOSFETs (Jiménez *et al.* 2004), Quadruple Gate GAA MOSFETs (Sharma *et al.* 2013), Π (Pi) - gate SOI MOSFETs (Park *et al.* 2001), Ω (Omega) – gate MOSFETs (Li *et al.* 2005). The basic objective of using the multiple gate structure is to increase the wrapping of channel surface area to reduce the SCEs. The gate-all-around (GAA) MOSFET structure can thus be considered as an important device with better control of the SCEs than many of the multiple gate MOS transistors (Song *et al.* 2006). They (Song *et al.* 2006) have discussed various merits of circular GAA over quadruple GAA due to reduced corner effects. The sharp corners of quadruple GAA can cause electrostatic coupling

between two adjacent gates at the corners which may degrade the SCEs, DIBL and drivability performance device. The SCEs of Π (Pi) - gate SOI MOSFETs (Park *et al.* 2001) is lower than the tri-gate FinFETs due to increased gate control over the bottom region of the channel. So far we have introduced various types of non-classical MOS transistor structures with possible features of sustaining the scaling trend for future generation IC technology. The present thesis has been designed to investigate the effects of gate/source elevation on the performances of gate-underlap non-classical DG MOSFETs and circular GAA MOSFETs. Prior to formulize the scope of the present thesis, we will survey some key literatures to investigate the state-of-the-art research in the related area of the thesis as discussed in the following.

1.4 Some State-of-the-Art Works on Source/Drain Engineering: Elevated Source/Drain and Ultra Shallow Junction (USJ) Structures

In this section, we will review some important literatures on the ultra shallow gate/source-channel junction non-classical MOS structures with/without elevated source/drain structures. The merits and demerits of both the gate-underlap and gate overlap structures will be reviewed. The effects of the source/drain elevation on the drivability performance of various non-classical MOS structures will also be reviewed.

1.4.1 Review of Some Elevated Source/Drain MOS Transistor Structures

The ultra-shallow junction (USJ) elevated source/drain (ESD) based MOSFET structure with one micron device channel length was first fabricated by (Wong *et al.* 1984)**.** The ESD MOFET structure showed better subthreshold characteristics in terms of smaller

threshold voltage roll off and smaller SCEs than the conventional MOSFETs. (Pfiester *et al.* (Pfiester *et al.* 1990) fabricated a self-aligned ESD MOSFET of 0.4 μm channel length by using a single selective silicon deposition step to define both the epitaxial source /drain and polycrystalline gate regions. They (Pfiester *et al.* 1990) used the self-aligned lightly doped drain/source and heavily doped channel regions in their ESD MOSFET structure. Kimura *et al.* (Kimura *et al.* 1991) fabricated a ESD MOSFET with channel length down to 0.1 μm (i.e. less than the contemporary lithography limit) by using Phase-shifted Lithography technique. Such structures were observed to have reduced source/drain resistance and junction capacitance as compared to the bulk MOSFETs (Kimura *et al.* 1991). A simulation based comparative study has been reported by Tian *et al.* (Tian *et al.* 1995) to show that in the ESD MOSFETs structure gradual profile at the source(drain)-channel junction has better suppression of hot carrier effects (HCEs) over the abrupt source(drain)-channel junction. Yamakawa *et al.*(Yamakawa *et al.* 1999) have observed a significant improvement in the drivability along with improved immunity against SCEs in ESD MOSFETs. Choi *et al.* (Choi *et al.* 2000) have simulated an ultra-thin body (UTB) ESD SOI MOSFET to demonstrate the reduction in the leakage current as well as the parasitic source/drain resistance. Their simulation study has shown the scalability of the UTB ESD SOI MOSFETs down to 18-nm gate length with a channel thickness of 5 nm. Shenoy *et al.* (Shenoy *et al.* 2003) have reported the optimization of the extrinsic source/drain resistance of sub-20 nm gate length UTB DG MOSFETs. About 80% reduction in the parasitic capacitance and 30% reduction in the series resistance have been reported by (Zhang *et al.* 2003) in the ESD MOS structures as compared to their corresponding values of the conventional planner source/drain MOS structures. Waite *et al.* (Waite *et al.* 2005) have studied the performance characteristics of the raised

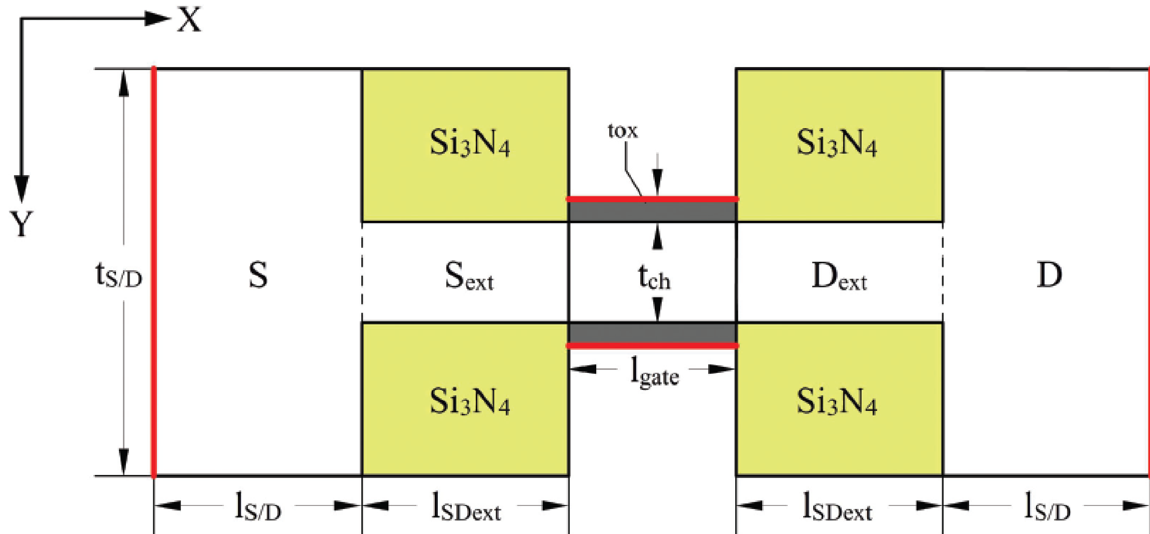


Fig 1.9: DG-MOSFET with RSD structure proposed by Holtij *et al.* (Holtij et al. 2012).

source/drain MOSFETs by using a silane /dichlorosilane mixture without any requirement of Cl_2 or HCl in the gas stream for selective source/drain epitaxy layers. They (Waite *et al.* 2005) have observed that the subthreshold swing is decreased from 102 mV/dec to 81.9 mV/dec when the thickness of the epitaxial silicon in source/drain is increased from 50 nm to 100 nm in the ESD MOSFETs. They have also observed that both the ON current (I_{on}) and OFF current I_{off} are decreased with the elevation height of the ESD MOSFETs while maintaining a nearly constant value of the I_{on}/I_{off} ratio. Saitoh *et al.* (Saitoh *et al.* 2011) have fabricated a Trigate silicon nanowire MOSFET with ESD structure. They (Saitoh *et al.* 2011) have shown that the short-channel performance can be improved by using elevated source/drain structures with thin spacers between the source-gate and drain-gate regions. Using the conformal mapping technique (i.e. the Schwarz-Christoffel transformation), Holtij *et al.* (Holtij *et al.* 2012) have proposed a 2D analytical model for the parasitic source/drain resistance in the ESD DG MOSFETs as shown in Fig. 1.9. They (Holtij *et al.* 2012) have modeled the fringing field from the raised and wrapped

source/drain to calculate the resistance of source/drain region which has been finally added to channel resistance to compute the overall resistance of device. Chen *et al.* (D. Chen, Jacobson, and Liu 2013) have carried out the simulation of an elevated source/drain MOSFET. They (D. Chen, Jacobson, and Liu 2013) have observed an increase in the effective drain current with the initial increase in the effective channel length due to drain to source direct tunneling . However, the effective drain current is decreased later with the increase in the effective channel length due to the increase in source/drain resistance. Therefore at lower effective channel length, increase in drain to source direct tunneling is dominant phenomenon over increase in source/drain resistance and for higher effective channel length it is vice versa. Tang *et al.* (Tang *et al.* 2013) have proposed a new fabrication technique for the elevated source/drain junctionless transistors. The literature survey carried out so far clearly shows that the elevated source/drain concept can be combined with the ultra-thin body (UTB) in MOS structures to optimize the device performance by controlling the parasitic source/drain resistance of the MOS transistors. The ESD structure can also be used in the MOSFETs with ultra-shallow source/drain junctions to improve their performance. We will thus carry out a brief literature survey on some non-abrupt ultra-shallow MOS structures in the following.

1.4.2 Review of Non-Abrupt Ultra Shallow Source/Drain Junction MOS Structures

Kwong *et al.* (Kwong *et al.* 2002) have studied the impacts of lateral doping abruptness at the source(drain)-channel junction and the gate-extension overlap length on the performance of MOS transistors. Shenoy *et al.* (Shenoy *et al.* 2003) have simulated a MOS transistor shown in Fig. 1.10 to optimize the extrinsic source drain resistance by

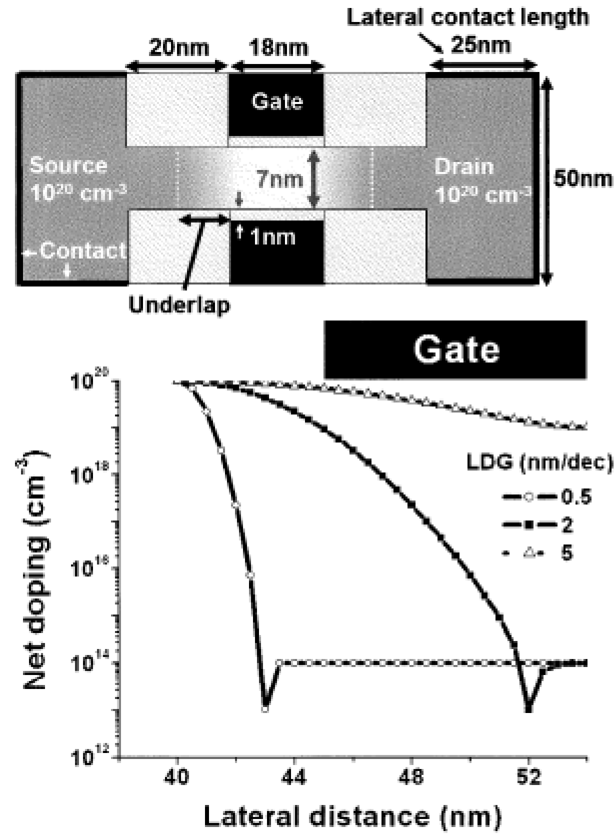


Fig 1.10: Ultra Shallow Junction Elevated Source/Drain Double gate MOSFET (top) and Lateral doping profile in the source extension region for three values of lateral doping gradient (bottom) (Shenoy *et al.* 2003).

investigating the effects of silicon body thickness t_{si}, gate length L_G, leakage current I_{off}, contact resistance ρ_c, underlap channel length L_{ul} and doping lateral straggle σ_L on the drivability performance of the device. In general, very low specific contact resistivity and hyper abrupt lateral doping profile are ideally desired for reducing the source/drain resistance . Kim *et al.* (Kim, Fossum, and Yang 2006) have proposed an analytical model for the fringe capacitance in the non-classical MOSFETs with gate–source and gate-drain underlap regions. By considering the source/drain doping profile into consideration, Kranti *et al.* (Kranti *et al.* 2006) have reported theoretical models for the channel potential, threshold voltage, DIBL and subthreshold swing of sub-50 nm DG MOSFETs with high-κ

gate dielectrics. Using the simulation results, Kim & Fossum (Kim and Fossum 2007) have reported the design optimization and performance projections of double-gate FinFETs with gate–source/drain underlap for SRAM applications. Yang *et al.* (J. Yang *et al.* 2007) have simulated a DG FinFET to show that the effect of gate source/drain underlap region on the speed performance of the device. They reported that by optimizing the gate-undelap length Fin thickness can be increased significantly up to the order of the physical gate length of the device without degrading the speed performance as compared to the conventional gate source/drain overlap. Such an increase in fin thickness combined with the relaxed required of abruptness at the source (drain)-channel junction can dramatically enhance the importance of DG FinFETs for 32-nm technology node and beyond. This study has shown that the gate-underlap region can be explored for reducing the leakage current, parasitic capacitances and SCEs (J. Yang *et al.* 2007). Kranti *et al.* (Kranti *et al.* 2008) have proposed a simulation study for the optimization of device parameters like $I_{off}, I_{on}, I_{on}/I_{off}$ ratio, intrinsic delay $(\tau = C_{gg}V_{dd}/I_{on})$, energy delay product and static power dissipation of the MOS transistors with lateral abruptness at the source(drain)-channel junction. Agrawal & Fossum (Agrawal and Fossum 2010) have reported an analytical model for the fringe capacitance in double-gate MOSFETs with realistic non-abrupt source(drain)-channel junctions and also with an effective gate-underlap region. A large number of works have also been reported on the analog and RF performances of ultra shallow junction gate-underlap MOS structures. Koley *et al.* (Koley *et al.* 2012) have analyzed the effect of asymmetric source/drain extensions on the subthreshold analog and RF performances of the ultra shallow junction gate-underlap DG MOSFETs at 45 nm technology node. Multistage circuits using DG MOSFETs with unsymmetrical source/drain extensions have better gain and grain-bandwidth product than the circuits

designed by DG MOS structures with symmetrical source/drain extension while a reverse phenomenon is observed for single stage circuits (Koley *et al.* 2012). In an another work, Koley *et al.* (Koley *et al.* 2013) have investigated the impact of high-*k* side spacer dielectrics on the subthreshold analog / RF performance enhancement of ultra shallow junction underlap DG FETs for low power applications. The effect of lateral straggle parameter of the Gaussian doping profile in the source/drain region on the distortion and intrinsic performance of asymmetric underlap DG-MOSFETs have also been reported by Koley *et al.* (Koley *et al.* 2014). They (Koley *et al.* 2014) have found that the intrinsic resistance and induction parameters for asymmetric underlap DG-MOSFETs are smaller than those of the symmetric underlap DG-MOSFETs at the cost of reduced intrinsic gain. The group (Koley *et al.* 2015) has also investigated the impact of different high-k spacers on asymmetric ultra shallow junction underlap DG-MOSFET for system-on-chip (SOC) applications. They (Koley *et al.* 2015) have observed that higher dielectric spacer can increase the miller capacitances which enhances the gain and the gain-bandwidth product of the device. Recently, Chattopadhyay *et al.* (Chattopadhyay *et al.* 2017) have studied the effect of spacer dielectric engineering on the performances of asymmetric source underlap DG MOSFETs using stack gate oxide structure. It is observed that the high-k spacer in the source side of the underlap gate stack DG MOSFETs not only improves the ON-state drain current, transconductance, intrinsic gain and intrinsic delay but also reduces the leakage current and DIBL of the device (Chattopadhyay et al. 2017). The increase in the lateral straggle parameter value reduces the output resistance (i.e. increases the channel conductance) at the cost of severe degradation of the device speed (Chattopadhyay et al. 2017). Nandi *et al.* (Nandi, Saxena, and Dasgupta 2013) have presented an analytical model for the threshold voltage and ON-state current of a USJ DG MOSFET with a gate

overlap structure. Sivaram *et al.* (Sivaram *et al.* 2016) have studied the impact of lateral straggle of the lateral Gaussian doping profile in the source/drain region on the RF and analog performances of the asymmetric gate stack DG MOSFETs.

1.4.3 Major Observations from the Literature Survey

We have presented some important state-of-the-art research works related to the effects of gate-underlap channel, source/drain elevation and ultra shallow junction at source-channel and drain-channel junctions. We will now summarize some major findings of the literature survey in the following:

- Ultra shallow junction (USJ) based gate overlap structure in the MOS transistors improves On-state current at the cost of increased short channel effects (SCEs) (Nandi, Saxena, and Dasgupta 2013). The increase in the lateral doping straggle parameter of the Gaussian doping profiles used in the source and drain regions increases DIDL, decreases threshold voltage and degrades the overall current I_{on}/I_{off} current ratio (Nandi, Saxena, and Dasgupta 2013).
- The replacement of the gate overlap structure by the gate-underlap structure in the MOSFET device structures can enhance the natural immunity against the SCEs and leakage current (J. Yang *et al.* 2007). The leakage current, gate capacitance, power and power-delay product (PDP) are decreased with the increase in gate-underlap length (Paul, Bansal, and Roy 2006). However, the above advantages are achieved at the cost of decreased On-state current due to increased effective channel length.
- Bansal & Roy (Bansal and Roy 2007) have analytically modeled the subthreshold potential, DIBL and subthreshold swing of uniformly doped underlap DG MOSFETs. Vaddi *et al.* (Vaddi, Agarwal, and Dasgupta 2011) have reported an

analytical model for the subthreshold current and subthreshold swing of an underlap DG MOSFET with tied/independent gate with symmetric/asymmetric options. In a later study, they (Vaddi, Agarwal, and Dasgupta 2012) have also analytically investigated the threshold voltage, threshold voltage roll-off and DIBL characteristics of uniformly doped underlap DG MOSFETs.

- Although, a large number of simulation studies have been reported on ultra shallow junction gate-underlap DG MOSFETs (Trivedi, Fossum, and Chowdhury 2005), (Kim, Fossum, and Yang 2006), (J. Yang *et al.* 2007), (Kranti, Hao, and Armstrong 2008), (Sachid *et al.* 2008), (Agrawal and Fossum 2010), (Tassis *et al.* 2010) and (Koley *et al.* 2013), no significant analysis has been reported for the subthreshold characteristics of the USJ gate-underlap MOSFETs with lateral Gaussian doping profiles in the source and drain regions.
- It is observed that the ON-state drain current is reduced due to increased effective channel length in all forms of gate-underlap MOSFET structures (Sachid *et al.* 2008), (Tassis *et al.* 2010) and (Vaddi, Agarwal, and Dasgupta 2011). However, the overall current On-to-Off state ratio is improved as a result of the decrease in the Off state leakage current (Sachid *et al.* 2008), (Tassis *et al.* 2010) and (Vaddi, Agarwal, and Dasgupta 2011).
- The recessed or elevated source/drain (ESD) structure in ultra thin body MOSFETs enhances the On-state drain current (M. Zhu *et al.* 2010), *(Shenoy et al.* 2003) and (D. Chen, Jacobson, and Liu 2013). Thus, the use of ESD engineering in the gate-underlap MOS structures can be expected to improve both the On-state drain current and ON-OFF current ratio I_{on}/I_{off} in addition to the enhanced immunity to the SCEs.

- A large number of simulation and fabrication studies (Wong *et al.* 1984), (K.K. Ng and Lynch 1987), (Pfiester *et al.* 1990), (Tian *et al.* 1995), (Yamakawa *et al.* 1999), (Choi *et al.* 2000), (Z. Zhang *et al.* 2003), (Shenoy *et al.* 2003), (Waite *et al.* 2005), (Saitoh *et al.* 2011), (Holtij *et al.* 2012) and (D. Chen, Jacobson, and Liu 2013) have been reported on the ESD gate-underlap MOSFETs to improve their drivability performance. However, there is no significant report on the effect of the source/drain elevation height and side spacer dielectric materials on the drivability performance of the ultra shallow junction (USJ) ESD gate-underlap MOSFETs structures.

In view of the above facts, we have tried to first develop analytical models for subthreshold potential, threshold voltage, subthreshold current and subthreshold swing characteristics of ultra shallow junction (USJ) gate-underlap DG MOSFETs. We have explored the commercial TCAD simulation tool ATLAS™ to investigate the quantitative effect of source/drain elevation height on the drivability performance of the USJ gate-underlap DG MOSFETs. Further quantitative effect of source/drain elevation height on the drivability performance of USJ gate-underlap GAA MOSFETs has been investigated. The overall scopes of the thesis have been outlined in the following section.

1.5 Scope of the Thesis

The prime target of this thesis is to investigate the effects of some source/drain engineering on the performance characteristics of gate-underlap DG and GAA MOS structures. The thesis consists of **Six Chapters** including the present Chapter namely “Introduction and

scope of the thesis". The contents of the remaining five Chapters of the thesis are outlined as follows:

In **Chapter-2,** we have developed analytical models for the potential distribution and threshold voltage of gate-underlap DG MOSFETs with a source/drain lateral Gaussian doping profile. The 2D Poisson's equation has been solved with suitable boundary conditions by applying the parabolic approximation and conformal mapping technique to obtain continuous channel potential in both the gate-underlap and overlap channel regions. The derived 2-D potential is used for defining the virtual cathode which is then used to obtain the threshold voltage for highly doped and moderately doped channels. The minimum surface potential has been used to model the threshold voltage of the DG MOSFETs. The effects of the doping profile parameters and other device parameters on the threshold voltage are investigated in details. The effects of doping lateral straggle σ_L parameter paired with different the geometrical parameters such as the gate under-lap length, the overlap gate length and channel thickness on the surface potential, threshold voltage and DIBL of the proposed device have been investigated. The validity of the proposed model is checked by comparing the results with the numerical simulation data obtained by using the commercially available ATLAS™ software, a 2D device simulator from SILVACO.

Chapter-3 presents a new analytical model for the subthreshold current and subthreshold swing of the short-channel symmetric underlap ultrathin DG MOSFETs with a source/drain lateral Gaussian doping profile as considered in Chapter-2. The channel potential model already derived in Chapter-3 has been utilized to formulate the closed form expression for the subthreshold current and swing of the device. The effects of the lateral straggle and geometrical parameters such as the channel length, channel thickness

and oxide thickness on the Off-state current and subthreshold slope have been demonstrated. Finally, theoretical results have been compared with ATLAS^{TM} simulation data to validate the observed results.

In **Chapter-4,** we have reported a TCAD based simulation study for investigating the effects of drain/source elevation height h_{SD} and side spacer dielectric between the gate and source/drain region on the drivability performance of the non-abrupt ultra-shallow-junction (USJ) gate-underlap DG MOSFETs of 18 nm gate length have been investigated for the first time in the present thesis. Four types of dielectrics namely the Air, SiO_2, Si_3N_4 and HfO_2 have been used as the spacer dielectrics in the region between the source (drain) and gate in the present study. A later Gaussian doping profile has been considered in the source and drain regions in the similar manner as considered in Chapter-2 and Chapter-3. Finally, the effects of both h_{SD} and spacer dielectric on the On-state I_{on} drain current, off-state I_{off} drain current, and I_{on}/I_{off} current ratio of the proposed structure have been investigated in details.

In **Chapter-5,** we have again explored the TCAD based simulation study for investigating the effects of source/drain elevation height h_{SD} engineering and permittivity of the side spacer dielectric material on the current drive of non- abrupt ultra shallow Junction (USJ) Gate All Around (GAA) MOSFETs. Four different types of dielectric materials namely Air, SiO_2, Si_3N_4 and HfO_2 as considered in Chapter-4 have also been in the present GAA structure. The effects of h_{SD} and spacer dielectric permittivity on the On-state I_{on} current, off-state I_{off} drain current, and I_{on}/I_{off} current ratio of GAA MOS transistors have been studied.

Chapter-6 includes the summary and conclusions of the present thesis. The major findings of the present study are summarized in this chapter. Finally, a brief discussion on the future scope of research in the related areas considered in the thesis is also presented in this chapter.