

---

---

## *References*

---

---

- E. O. Kane, "Zener tunneling in semiconductors," *J. Phys. Chem. Solids*, vol. 12, no. 2, pp. 181–188, Jan. 1960.
- D. Kahng, and M. M. Atalla. "Silicon-Silicon Dioxide Field Induced Surface Devices." *In IRE Solid-State Device Res. Conf.*, Carnegie Institute of Technology, Pittsburgh., 1960.
- Gordon E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 114–117, April 19, 1965.
- A. Grove and D. Fitzgerald, "The Origin of Channel Currents Associated with P+ Regions in Silicon," *IEEE Trans. Electron Devices*, vol. ED-12, no. 12, pp. 619-626, 1965.
- R. H. Dennard, F. H. Gaenssle., H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuit.*, vol. 9 , pp. 256-268, 1974.
- G. E. Moore, "Progress in Digital Integrated Electronics," Technical Digest 1975: *IEEE International Electron Devices Meeting*, pp. 11-13, 1975.
- J. Quinn, G. Kawamoto, and B. Mc Combe, "Subband Spectroscopy by Surface Channel Tunneling," *Surface Science*, vol. 73, pp. 190-196, 1978.
- S. M. Sze, *Physics of Semiconductor Devices*, New York: Wiley, 1981.
- R Booth, M. White, H. Wong, and T. Krutsick, "The Effect of Channel Implants on MOS Transistor Characterization," *IEEE Trans. Electron Devices*, vol. 34, pp. 2501-2506, Dec. 1987.
- S. Banerjee, W. Richardson, J. Coleman, and A. Chatterjee, "A new three-terminal tunnel device," *IEEE Electron Device Lett.*, EDL-8, pp. 347-349, 1987.
- K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 36, no. 2, pp. 399–402, Feb. 1989.
- T. Baba, "Proposal for Surface Tunnel Transistors," *Jpn. J. Appl. Phys.*, vol. 31, pp. L455-L457, 1992.
- N. D. Arora, "MOSFET Models for VLSI Circuit Simulations: Theory and Practice," *Springer-Verlog Wien*, New York, 1993.

- Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," *IEEE Electron Device Lett.*, vol. 14, no. 12, pp. 569–571, 1993.
- W. Reddick and G. Amaratunga, "Silicon surface tunnel transistor," *Appl. Phys. Lett.*, vol. 67, no. 4, pp. 494-496, 1995.
- J. Koga and A. Toriumi, "Negative differential conductance in three-terminal silicon tunneling device," *Appl. Phys. Lett.*, vol. 69, no. 10, pp. 1435-1437, 1996.
- E. Takeda, H. Matsuoka, Y. Igura, and S. Asai, "A band to band tunneling MOS device B2TMOSFET," in *IEDM Tech. Dig.*, pp. 402-405, 1998.
- Y. Taur, and T. H. Ning, "Fundamentals of Modern VLSI Devices" Cambridge University Press, 1998.
- X. Zhou and W. Long, "A Novel Hetero-Material Gate (HMG) MOSFET for Deep-Submicron ULSI Technology," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2546-2548, 1998.
- W. Long, H. Ou, J-M. Kuo, and K. K. Chin, "Dual-Material Gate (DMG ) Field Effect Transistor," *IEEE Trans. Electron Devices*, vol. 46, no. 5, pp. 865–870, 1999.
- W. Hansch, C. Fink, J. Schulze, and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon," *Thin Solid Films*, vol. 369, pp. 387-389, 2000.
- Xing Zhou, "Exploring the Novel Characteristics of Hetero-Material Gate Field-Effect Transistors with Gate-Material Engineering," *IEEE Trans. Electron Device*, vol. 47, no.1, pp. 113-120, Jan. 2000.
- K. Kim and J. Fossum, "Double-gate CMOS: Symmetrical-versus asymmetrical-gate devices," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 294–299, Feb. 2001.
- S. Lin and J. Kuo, "Modeling the fringing electric field effect on the threshold voltage of FD SOI nMOS devices with the LDD/sidewall oxide spacer structure," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2559– 2564, Dec. 2003.
- J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, pp. 196805-1-4, 2004.
- A. Chaudhry and M. J. Kumar, "Investigation of the Novel Attributes of a Fully Depleted Dual-Material Gate SOI MOSFET," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1463–1467, 2004.

- Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, Feb. 2004.
- Y. Hou, M. Li, Tony Low, and D. Kwong, "Metal Gate Work Function Engineering on Gate Leakage of MOSFETs," *IEEE Trans. Electron Device.*, vol. 51, no. 11, pp. 1783–1789, Nov. 2004.
- C. Aydin, A. Zaslavsky, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Lateral interband tunneling transistor in silicon-on-insulator," *Appl. Phys. Lett.*, vol. 84, no. 10, pp. 1780-1782, 2004.
- K. Bhuvalka, J. Schulze, I. Eisele, "Performance Enhancement of Vertical Tunnel Field-Effect Transistor with SiGe in the dp+ Layer," *Jap. J. Appl. Phys.*, vol. 43, no. 7A, pp. 4073-4078, 2004.
- P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, "Complementary tunneling transistor for low power application," *Solid State Electron.*, vol. 48, no. 12, pp. 2281–2286, Dec. 2004.
- J. Appenzeller, Y. Lin, J. Knoch, Z. Chen, P. Avouris, "Comparing Carbon Nanotube Transistors –The Ideal Choice: A Novel Tunneling Device Design," *IEEE Trans. Electron Devices*, vol. 52, no.12, pp. 2568-2576, 2005.
- K. K. Bhuvalka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate work function engineering," *IEEE Trans. Electron Devices*, vol. 52, no. 5, pp. 909–917, May 2005.
- G. V. Reddy, and M. J. Kumar, "Investigation of the novel attributes of a single-halo double gate SOI MOSFET: 2D simulation study," *Microelectronics Journal*, vol. 35, no. 9, pp. 761-765, 2004.
- B. Meyerson, *Semico Impact Conference*, Taiwan, January 2004.
- K. K. Bhuvalka, M. Born, M. Schindler, M. Schmidt, T. Sulima, and I. Eisele, "P-Channel Tunnel Field-Effect Transistors down to Sub-50 nm Channel Lengths," *Jap. J. Appl. Phys.*, vol. 45, no. 4, pp. 3106-3109, 2006.
- B. G. Streetman, and S. K. Banerjee, *Solid State Electronic Devices*, Pearson Prentice Hall India, 2006.
- P. Nilsson, "Arithmetic Reduction of the Static Power Consumption in Nanoscale CMOS," *IEEE Int. Conf. on Electronics, Circuits and Systems*, pp. 656-659 2006.

- B. Sviličić, and A. Kraš, “CMOS technology: challenges for future development”, Pomorstvo, *Journal of Maritime Studies*, vol. 20, no. 2, pp. 97-104, 2006.
- A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, “Tunnel field-effect transistor without gate-drain overlap,” *Appl. Phys. Lett.*, vol. 91, no. 5, pp. 053 102-1–053 102-3, Jul. 2007.
- T. K. Chiang and M.L. Chen, “A new analytical threshold voltage model for symmetrical double-gate MOSFETs with high- $k$  gate dielectrics,” *Solid State Electron.*, vol. 51, no. 12, pp. 387-393, Jan. 2007.
- P. Packan, “Device and Circuit Interactions,” *IEEE International Electron Device Meeting (IEDM '07) Short Course: Performance Boosters for Advanced CMOS Devices*, December 2007.
- T. Nirschl, M. Weis, M. Fulde, and D. Schmitt-Landsiedel, “Correction to Revision of Tunneling Field-Effect Transistor in Standard CMOS Technologies,” *IEEE Electron Device Lett.*, vol. 28, no. 4, p. 315, 2007.
- K. Boucart and A. M. Ionescu, “Threshold voltage in Tunnel FETs: physical definition, extraction, scaling and impact on IC design,” in *Proc. ESSDERC*, pp. 299-302, 2007a.
- K. Boucart and A. M. Ionescu, “Length scaling of the Double Gate Tunnel FET with a high- $k$  gate dielectric,” *Solid-State Elec.*, vol. 51, no. 11-12, pp. 1500-1507, Nov.-Dec. 2007b.
- E.-H. Toh, G. Wang, G. Samudra, and Y.-C. Yeo, “Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization,” *Appl. Phys. Lett.*, vol. 90, pp. 263507-1-3, 2007.
- W. Y. Choi, B. G. Park, J. D. Lee, and T.-J. King Liu, “Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec,” *IEEE Trans. Electron Devices*, vol. 28, no. 8, pp. 743–745, 2007.
- K. Boucart and A. M. Ionescu, “Double-gate tunnel FET with high- $\kappa$  gate dielectric,” *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725– 1733, Jul. 2007c.
- K. Boucart and A. M. Ionescu, “A new definition of threshold voltage in Tunnel FETs,” *Solid-State Electronics*, vol. 52, pp. 1318-1323, May 2008.
- C. Shen, S. Ong, C. Heng, G. Samudra, and Y. Yeo, “A Variational Approach to the Two-Dimensional Nonlinear Poisson’s Equation for the Modeling of Tunneling

- Transistors,” *IEEE Electron Devices Letters*, vol. 29, no. 11, pp. 1252–1255, Nov. 2008.
- S. Salahuddin and S. Datta, “Use of negative capacitance to provide voltage amplification for low power nanoscale devices,” *Nano Lett.*, vol. 8, no. 2, pp. 405–410, 2008.
- N. Patel, A. Ramesha, and S. Mahapatra, “Drive current boosting of n-type tunnel FET with strained SiGe layer at source,” *Microelectronics Journal*, vol. 39, pp. 1671–1677, 2008.
- V. Nagavarapu, R. Jhaveri, and J. Woo, “The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor,” *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013-1019, 2008.
- A. Verhulst, W. Vandenberghe, K. Maex, S. De Gendt, M. Heyns, and G. Groeseneken, “Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates,” *Electron Device Lett.*, vol. 29, no. 12, pp. 1398-1401, 2008.
- Eng-Huat Toh, G. H. Wang, G. Samudra, and Yee-Chia Yeo, “Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications,” *J. Appl. Phys.*, vol. 103, pp. 104504:1-5, 2008.
- T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, “Double-Gate Strained-Ge Hetero structure Tunneling FET (TFET) With Record High Drive Currents and  $\ll 60$  mV/dec Subthreshold Slope,” *IEEE Int. Electron Dev. Meeting (IEDM)*, 2008.
- O. M. Nayfeh, C. Ni Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D. A. Antoniadis, “Design of Tunneling Field-Effect Transistors Using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunctions,” *IEEE Electron Device Lett.*, vol. 29, no. 9, pp. 1074– 1077, Sep. 2008.
- C. Hu, “Green Transistor as a Solution to the IC Power Crisis,” in *Proc. 9th Int. Conf. Solid-State Int. Circuit Technol.*, pp. 16–20, 2008.
- V. Nagavarapu, R. Jhaveri, and Jason C. S. Woo, “The Tunnel Source (PNPN) n-MOSFET: A Novel High Performance Transistor,” *IEEE Trans. Electron Devices*, vol. 55, pp. 1013-1019, Apr. 2008.
- S. Saurabh and M. J. Kumar, “Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical

- Investigation and Analysis,” *Japanese Journal of Applied Physics*, vol. 48, pp. 064503-7, 2009.
- Y. Khatami and K. Banerjee, “Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2752-2761, 2009.
- M. Vadizadeh and M. Fathipour, “Using Low-k Oxide for Reduction of Leakage Current in Double Gate Tunnel FET,” in *Proc. ULIS*, pp. 301-304, 2009.
- C. Sandow, J. Knoch, C. Urban, Q.-T. Zhao, and S. Mantl, “Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors,” *Solid-State Elec.*, vol. 53, pp. 1126-1129, 2009.
- D. Kazazis, P. Jannaty, A. Zaslavsky, C. Le Royer, C. Tabone, L. Clavelier, and S. Cristoloveanu, “Tunneling field-effect transistor with epitaxial junction in thin germanium-on-insulator,” *Appl. Phys. Lett.*, vol. 94, pp. 263508-1-3, 2009.
- Y. Khatami and K. Banerjee, “Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits,” *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2752-2761, 2009.
- M. Luisier and G. Klimeck, “Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors,” *Electron Device Lett.*, vol. 30, no. 6, pp. 602-604, 2009.
- M. Schlosser, K. Bhuwarka, M. Sauter, T. Zilbauer, T. Sulima, and I. Eisele, “Fringing-Induced Drain Current Improvement in the Tunnel Field-Effect Transistor With High-k Gate Dielectrics,” *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 100-108, 2009.
- M. G. Bardon, Herc P. Neves, Robert Pures, and Chris Van Hoof, “Pseudo-Two-Dimensional Model for Double-Gate-Tunnel FETs Considering the Junctions Depletion Regions,” *IEEE Trans. Electron Devices*, vol. 57, no. 4, pp. 827-834, April 2010.
- W. Y. Choi and W. Lee, “Hetero-gate-dielectric tunneling field effect transistors,” *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2317– 2319, Sep. 2010.
- S. Dubey, P. K. Tiwari, and S. Jit, “A two-dimensional model for the potential distribution and threshold voltage of short-channel DG MOSFETs with a vertical Gaussian-like doping profile,” *Journal of Applied Physics*, vol. 108, pp. 034518-7, 2010.

- K. Boucart, "Simulation of Double-Gate Silicon Tunnel FETs with a High-k Gate Dielectric," *École Polytechnique Fédérale De Lausanne*, 2010.
- J. Knoch and J. Appenzeller, "Modeling of high-performance p-type III–V heterojunction tunnel FETs," *IEEE Electron Device Lett.*, vol. 31, no. 4, pp. 305–307, Apr. 2010.
- A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.
- A. S. Verhulst, B. Soree, D. Leonelli, W. G. Vandenberghe, and G. Groeseneken, "Modeling the Single-Gate, Double-Gate, and Gate-All-Around Tunnel Field-Effect Transistor," *J. Appl. Phys.*, vol. 107, pp. 024518:1-8, 2010.
- S. H. Kim, S. Agarwal, Z. A. Jacobson, P. Matheu, C. Hu, and Tsu-Jae King Liu, "Tunnel Field Effect Transistor With Raised Germanium Source," *IEEE Electron Device Lett.*, vol. 31, no. 10, pp. 1107–1109, Oct. 2010.
- D. Leonelli, A. Vandooren, R. Rooyackers, A. S. Verhulst, S. De Gendt, M. M. Heyns and G. Groeseneken, "Performance Enhancement in Multi Gate Tunneling Field Effect Transistors by Scaling the Fin-Width," *Japanese Journal of Applied Physics*, vol. 49, 2010.
- Chen Shen, Li-Tao Yang, Ganesh Samudra, and Yee-Chia Yeo, "A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET," *Solid-State Electronics*, vol. 57, pp. 20-30, 2011.
- W. G. Vandenberghe, B. Sorée, W. Magnus, G. Groeseneken, and M. V. Fischetti, "Impact of field-induced quantum confinement in tunneling field-effect devices," *Applied Physics Lett.*, vol. 98, pp. 143503-3, 2011.
- S. Saurabh and M. J. Kumar, "Novel attributes of a Dual Material Gate Nanoscale Tunnel Field-effect Transistor," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 404–410, Feb. 2011.
- A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy efficient electronic switches," *Nature*, vol. 479, no. 7373, pp. 329–337, Nov. 2011.
- W. Lee and W. Young Choi, "Influence of Inversion Layer on Tunneling Field-Effect Transistors," *IEEE Electron Device Letters*, vol. 32, no. 9, pp. 1191-1193, Sept. 2011.
- A. Pan and C. O. Chui, "A Quasi-Analytical Model for Double-Gate Tunneling Field-Effect Transistors," *IEEE Electron Device Letters*, vol. 33, pp. 1468-1470, 2012.

- L. Liu, D. Mohata, and S. Datta, "Scaling Length Theory of double-gate interband tunnel field-effect transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 902–908, Apr. 2012.
- Sung Hwan Kim, "Germanium-Source Tunnel Field Effect Transistors for Ultra-Low Power Digital Logic," Electrical Engineering and Computer Sciences University of California at Berkeley May. 2012.
- L. Zhang, J. He, and M. Chan, "A Compact Model for Double-Gate Tunneling Field-Effect-Transistors and Its Implications on Circuit Behaviors," *IEEE Int. Electron Dev. Meeting (IEDM)*, pp. 6.8.1–4, 2012.
- José L. Padilla, Francisco Gámiz, and Andrés Godoy, "Impact of Quantum Confinement on Gate Threshold Voltage and Subthreshold Swings in Double-Gate Tunnel FETs," *IEEE Trans. Electron Devices*, vol. 59, pp. 3205-3211, Dec. 2012.
- Rakhi Narang, M. Saxena, R. S. Gupta, and M. Gupta, "Drain current model for a gate all around (GAA) p–n–p–n tunnel FET," *Microelectronics Journal*, vol. 44, pp. 479-488, May 2013.
- M. J. Kumar and S. Janardhanan, "Doping-less Tunnel Field Effect Transistor: Design and Investigation," *IEEE Trans. Electron Devices*, vol. 60, pp. 3285-3290, 2013.
- A. Pan, S. Chen, and C. O. Chui, "Electrostatic Modeling and Insights Regarding Multigate Lateral Tunneling Transistors," *IEEE Trans. Electron Devices*, vol. 60, pp. 2712-2720, 2013.
- Li Chen, Z. He-Ming, Z. Yu-Ming, H. Hui-Yong, W. Bin, L. Yong, and Z. Chun, "Two-dimensional threshold voltage model of a nanoscale silicon-on-insulator tunneling field-effect transistor," *Chin. Phys. B*, vol. 22, no. 3. pp. 038501-1-03501-6. 2013.
- D. Sharma, and S. K. Vishvakarma, "Precise Analytical Model for Short-Channel Quadruple-Gate Gate-All-Around MOSFET", *IEEE Transactions on Nanotechnol*, vol. 12, no. 3, pp. 378-385, 2013.
- M. Yadav, A. Bulusu, and S. Dasgupta, "Two dimensional analytical modeling for asymmetric 3T and 4T double gate tunnel FET in sub-threshold region: Potential and electric field," *Microelectronics Journal*, vol. 44, pp. 1251-1259, 2013.
- G. Lee, J.-S. Jang, and W. Y. Choi, "Dual-dielectric-constant spacer hetero-gate dielectric tunneling field-effect transistors," *Semicond. Sci. Technol.*, vol. 28, no. 5, p. 052001, Mar. 2013.



- ATLAS: 2-D Device Simulator, SILVACO Int., Santa Clara, CA, USA, 2013.
- Rajat Vishnoi and M. Jagadesh Kumar, “2-D analytical model for the threshold voltage of a tunneling FET with localized charges,” *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3054–3059, Sept. 2014.
- Arnab Biswas, Adrian M. Ionescu, “Study of Fin-Tunnel FETs with doped pocket as Capacitor-less 1T DRAM,” *IEEE Proceedings of the SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, 2014.
- L. Zhang and M. Chan, “SPICE modeling of double-gate tunnel-FETs including channel transports,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 300–307, Feb. 2014.
- C. Wu, R. Huang, Q. Huang, C. Wang, J. Wang, and Y. Wang, “An analytical surface potential model accounting for the dual-modulation effects in Tunnel FETs,” *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2690-2696, Aug. 2014.
- Rajat Vishnoi and M. Jagadesh Kumar, “Compact Analytical Model of Dual Material Gate Tunneling Field Effect Transistor using Interband Tunneling and Channel Transport,” *IEEE Trans. Electron Devices*, vol. 61, pp. 1936-1942, June 2014.
- Rajat Vishnoi and M. Jagadesh Kumar, “A Pseudo 2D-analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET,” *IEEE Trans. Electron Devices*, vol. 61, pp. 2264-2270, July 2014.
- M. Gholizadeh and S. E. Hosseini, “A 2-D analytical model for double gate tunnel FETs,” *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1494–1500, May 2014.
- K.-H. Kao, A. S. Verhulst, W. G. Vandenberghe, B. Soree, G. Groeseneken, and K. De Meyer, “Direct and indirect band-to-band tunneling in germanium-based Tunnel FETs,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 1494–1500, Feb. 2014.
- L. Zhang and M. Chan, “SPICE modeling of double-gate tunnel-FETs including channel transports,” *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 300–307, Feb. 2014.
- G. B. Beneventi, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “Dual-metal-gate InAs Tunnel FET with enhanced turn-on steepness and high ON-current,” *IEEE Trans. Electron Devices*, vol. 61, pp. 776 -784, Mar. 2014.
- K. Tomioka and T. Fukui, “Current increment of tunnel field-effect transistor using InGaAs nanowire/Si hetero junction by scaling of channel length,” *Applied Physics Lett.*, vol. 104, pp. 073507-4, 2014.

- G. B. Beneventi, E. Gnani, A. Gnudi, S. Reggiani, and G. Bacarani, "Dual-Metal-Gate InAs Tunnel FET With Enhanced Turn-On Steepness and High ON-Current," *IEEE Trans. Electron Device.*, vol. 61, no. 3, pp. 776–784, March 2014.
- M. Graef, T. Holtij, F. Hain, A. Kloes, Benjamín Iníguez, "A 2-D closed form model for the electrostatics in hetero-junction double-gate tunnel-FETs for calculation of band-to-band tunneling current," *Microelectronics Journal*, vol. 45, pp. 1144–1153, Mar. 2014.
- F. Villani, E. Gnani, A. Gnudi, S. Reggiani, and G. Bacarani, "A quasi 2D semi analytical model for the potential profile in hetero and homo junction tunnel FETs," *Solid-State Electronics*, vol. 113, pp. 86-91, June 2015.
- R. Vishnoi and M. J. Kumar, "A compact analytical model for the drain current of gate-all-around nanowire Tunnel FET accurate from sub-threshold to ON-state," *IEEE Trans. Nanotech.*, vol. 14, no. 2, pp. 358-362, 2015.
- Upasana, R. Narang, M. Saxena, and M. Gupta, "Modeling and TCAD assessment for gate material and gate dielectric engineered TFET architectures: Circuit-level investigation for digital applications," *IEEE Trans. Electron Devices*, vol. 62, no. 10, pp.3348-3356, 2015.
- Jaya Madan, R. S. Gupta, and Rishu Chaujar, "Analytical drain current formulation for gate dielectric engineered dual material gate-gate all around-tunneling field effect transistor," *Japanese Journal of Applied Physics*, vol. 54, pp. 094202-9, Aug. 2015.
- M. Kumar and S. Jit, "A Novel Four-Terminal Ferroelectric Tunnel FET for Quasi-Ideal Switch," *IEEE Trans. Nanotechnology*, vol. 14, pp. 600-602, 2015a.
- M. Kumar and S. Jit, "Effects of Electrostatically Doped Source/Drain and Ferroelectric Gate Oxide on Subthreshold Swing and Impact Ionization Rate of Strained-Si-on-Insulator Tunnel Field Effect Transistors," *IEEE Trans. Nanotechnology*, vol. 14, pp. 597-599, 2015b.
- Rajat Vishnoi and M. Jagadesh Kumar, "An Accurate Compact Analytical Model for the Drain Current of TFET from Subthreshold to Strong Inversion," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 478-484, 2015.
- S. Dash and G. P. Mishra, "A 2D Analytical Cylindrical Gate Tunnel FET (CG-TFET) Model: Impact of Shortest Tunneling Distance," *Adv. Nat. Sci.: Nanosci. Nanotechnology*, vol. 6, 035005:1-10, 2015a.

- S. Dash and G. P. Mishra, "A New Analytical Threshold Voltage Model of Cylindrical Gate Tunnel FET (CG-TFET)," *Superlattices and Microstructures*, vol. 86, pp. 211-220, 2015b.
- Sunil Kumar and Balwinder Raj, "Compact channel potential analytical modeling of DG-TFET based on Evanescent-mode approach," *Journal Comput. Electron*, vol. 14, pp. 820-827, 2015.
- P. Jain, V. Prabhat, and B. Ghosh, "Dual metal-double gate tunnel field effect transistor with mono/hetro dielectric gate material," *J. Comput Electron*, vol. 14, pp. 537–542, Mar. 2015.
- P. Pandey, R. Vishnoi, and M. Kumar, "A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling," *J. Comput Electron*, vol. 14, pp. 280–287, 2015.
- Hao Lu, David Esseni, and Alan Seabaugh, "Universal analytic model for tunnel FET circuit simulation," *Solid-State Electronics*, vol. 108, pp. 110-117, 2015.
- Yuan Taur, Jianzhi Wu, and Jie Min, "An Analytic Model for Heterojunction Tunnel FETs With Exponential Barrier," *IEEE Trans. Electron Devices*, vol. 108, pp. 110-117, 2015.
- Wanjie Xu, Hei Wonga, and Hiroshi Iwai, "Analytical model of drain current of cylindrical surrounding gate p-n-i-n TFET," *Solid-State Electronics*, vol. 111, pp. 171-179, 2015.
- K. Hemanjaneyulu and M. Shrivastava, "Fin Enabled Area Scaled Tunnel FET," *IEEE Trans. Electron Devices*, vol. 62, pp. 3184-3191, Oct. 2015.
- Jianzhi Wu, Jie Min, and Yuan Taur, "Short-Channel Effects in Tunnel FETs," *IEEE Trans. Electron Devices*, vol. 62, pp. 3019-3024, Sep. 2015.
- S. Chander and S. Baishya, "A two-dimensional gate threshold voltage model for a heterojunction SOI-Tunnel FET with oxide/source overlap," *IEEE Electron Device Letters*, vol. 36, no. 7, pp. 714-716, July 2015.
- P. Wang, YiQi Zhuang, Cong Li, Zhi Jiang, and YuQi Liu, "Drain current model for double-gate tunnel field-effect transistor with hetero-gate-dielectric and source-pocket," *Microelectronics Reliability*, vol. 59, pp. 30-36, Feb. 2016.
- S. Dash, Biswajit Jena, and Guru Prasad Mishra, "A new analytical drain current model of cylindrical gate silicon tunnel FET with source  $\delta$ -doping," *Superlattices and Microstructures*, vol. 97, pp. 231-241, June 2016.

- H. Reza Tajik Khaveh and S. Mohammadi, "Potential and Drain Current Modeling of Gate-All-Around Tunnel FETs Considering the Junctions Depletion Regions and the Channel Mobile Charge Carriers," *IEEE Trans. Electron Devices*, vol. 63, pp. 5021-5029, Dec. 2016.
- A. Mishra, R. Narang, M. Saxena, and M. Gupta, "Impact of interfacial fixed charges on the electrical characteristics of pocket-doped double-gate Tunnel FET," *IEEE Trans. Devices Materials Reliability*, vol. 16, no. 2, pp. 117-122, June 2016.
- D. S. Yadav, D. Sharma, B. Ram Raad, and Varun Bajaj, "Impactful study of dual work function, underlap and hetero gate dielectric on TFET with different drain doping profile for high frequency performance estimation and optimization," *Superlattices and Microstructures*, vol. 96, pp. 36-46, Aug. 2016.
- A. Pal and A. K. Dutta, "Analytical drain current modeling of double-gate Tunnel FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3213-3221, Aug. 2016.
- W. Y. Choi and H. K. Lee, "Demonstration of hetero-gate-dielectric tunneling field-effect transistors (HG TFETs)," *Nano Convergence*, vol. 3, no. 1, pp. 1-15, 2016.
- J. U. Mehta, W. A. Borders, H. Liu, R. Pandey, S. Datta, and L. Lunardi, "III-V tunnel FET model with closed-form analytical solution," *IEEE Trans. Electron Devices*, vol. 63, no. 5, pp. 2163-2168, May 2016.
- S. Chander and S. Baishya, "Two-dimensional model of a heterojunction silicon-on insulator tunnel field effect transistor," *Superlattices and Microstructures*, vol. 90, pp. 176-183, 2016.
- P. Dutta, K. Koley, Arka Dutta, and C. Kumar Sarkar, "An Analytical BTBT Current Model of Symmetric/Asymmetric 4T Tunnel Double Gate FETs With Ambipolar Characteristic," *IEEE Trans. Electron Devices*, vol. 63, pp. 2700-2706, July 2016.
- S. Marjani, Seyed Ebrahim Hosseini, and Rahim Faez, "A 3-D analytical modeling of tri-gate tunneling field-effect transistors," *J Comput Electron*, vol. 15, pp. 820-830, June 2016.
- Navjeet Bagga and Subir Kumar Sarkar, "An Analytical Model for Tunnel Barrier Modulation in Triple Metal Double Gate TFET," *IEEE Trans. Electron Devices*, vol. 62, pp. 2136-2142, July 2016.

- V. Prabhat and A. K. Dutta, "Analytical Surface Potential and Drain Current Models of Dual-Metal-Gate Double-Gate Tunnel-FETs, *IEEE Trans. Electron Devices*, vol. 63, pp. 2190-2196, May 2016.
- S. Ahish, D. Sharma, Y. B. Nithin Kumar, and M. H. Vasantha, "Performance Enhancement of Novel InAs/Si Hetero Double-Gate TFET Using Gaussian Doping," *IEEE Trans. Electron Devices*, vol. 63, pp. 288-295, Jan. 2016.
- Y. Dong, L. Zhang, X. Li, X. Lin, and M. Chan, "A compact model for double-gate heterojunction tunnel FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4506–4513, Nov. 2016.
- S. Sarkhel, Navjeet Bagga, and S. Kumar Sarkar, "Compact 2-D modeling and drain current performance analysis of a work function engineered double gate tunnel field effect transistor," *J Comput. Electron*, vol. 15, pp. 104-114, 2016.
- S. Dash, G. Shankar Sahoo, and G. Prasad Mishra, "Subthreshold swing minimization of cylindrical tunnel FET using binary metal alloy gate," *Superlattices and Microstructures*, vol. 91, pp. 105-111, Jan. 2016.
- D. B. Abdi and M J Kumar, "Suppressing Amplipolar Conduction using Dual-Material in Tunnel-FETs Having Heavily Doped Drain," *Int. J. of Electronics and Communication Engineering*, vol. 10, no.5, pp. 594-598, 2016.
- S. Ahish, Dheeraj Sharma, M.H. Vasantha, Y.B.N. Kumar, "Device and circuit level performance analysis of novel InAs/Si heterojunction double gate tunnel field effect transistor," *Superlattices and Microstructures*, vol. 94, pp. 119-130, 2016.
- Arnab Pal and A. K. Dutta, "Analytical drain current modeling of double-gate Tunnel FETs," *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3213–3221, Aug. 2016.
- Jaya Madan and Rishu Chaujar, "Numerical simulation of N<sup>+</sup> source pocket PIN-GAA-Tunnel FET: Impact of interface trap charges and temperature," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1482–1488, April 2017.
- S. Safa, S. L. Noor, and Md. Z. R. Khan, "Physics-based generalized threshold voltage model of multiple material gate tunneling FET structure," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1449-1454, April 2017.
- S. Mohammadi and H. R.T. Khaveh, "An analytical model for double-gate Tunnel FETs considering the junctions depletion regions and the channel mobile charge carriers," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1276–1284, Mar. 2017.

- P. Jain, C. Yadav, A. Agarwal and Y. S. Chauhan, "Surface potential based modeling of charge, current, and capacitances in DG Tunnel FET including mobile channel charge and ambipolar behaviour," *Solid-State Electronics*, vol. 134, pp. 74-81, June 2017.
- Y. Guan, Z. Li, W. Zhang, and Y. Zhang, "An accurate analytical current model of double-gate heterojunction Tunnel FET," *IEEE Trans. Electron Devices*, vol. 64, no.3, pp. 938-944, Mar. 2017.
- Upasana, Rakhi Narang, Manoj Saxena, Mridula Gupta, "Drain Current Model for Double Gate (DG) p-n-i-n TFET: Accumulation to Inversion Region of Operation," *Superlattices and Microstructures*, vol. 104, pp. 78-92, 2017.
- Bin Lu, Hongliang Lu, Yuming Zhang, Yimen Zhang, Xiaoran Cui, Chengji Jin, Chen Liu, "Improved analytical model of surface potential with modified boundary conditions for double gate tunnel FETs," *Microelectronics Reliability*, vol. 79, pp. 231-238, 2017.
- D. Gracia, D. Nirmal, A. Nisha Justeena, "Investigation of Ge based double gate dual metal tunnel FET novel architecture using various hetero dielectric materials," *Superlattices and Microstructures*, vol. 109, pp. 154-160, 2017.
- P. Xu, H. Lou, Lining Zhang, Z. Yu, and Xinnan Lin, "Compact Model for Double-Gate Tunnel FETs With Gate-Drain Underlap," *IEEE Trans. Electron Devices*, vol. 64, pp. 5242-5248, Dec. 2017.
- Nupur Navlakha and Abhinav Kranti, "Insights into operation of planar tri-gate tunnel field effect transistor for dynamic memory application," *Journal of Applied Physics*, vol. 122, pp. 044502-1-9, May 2017.
- W. Xu, H. Wong, H. Iwai, Jun Liu, and Pei Qin, "Analytical modeling on the drain current characteristics of gate-all-around TFET with the incorporation of short-channel effects," *Solid-State Electronics*, vol. 138, pp. 24-29, July 2017.

IR1: <http://pubs.rsc.org/en/content/articlehtml/2015/NR/C4NR01600A>

IR2: [http://www.slideshare.net/varun\\_bansal90/power-7535521](http://www.slideshare.net/varun_bansal90/power-7535521)